

March 2007

HI-8588

ARINC 429 Line Receiver

DESCRIPTION

The HI-8588 is an ARINC 429 bus interface receiver and is available in a SO 8 pin package. The technology is analog/digital CMOS. The circuitry requires only a 5 volt supply.

The ARINC bus can be connected directly to the chip. The typical 10 volt differential signal is translated and input to a window comparator and latch. The comparator levels are just below the standard 6.5 volt minimum ARINC data threshold and just above the standard 2.5 volt maximum ARINC null threshold.

The TESTA and TESTB inputs bypass the analog for testing purposes. Also if TESTA and TESTB are both taken high, the analog powers down and the digital outputs tristate allowing wire-or possibilities.

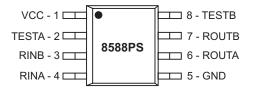
Please refer to the HI-8588-10 for applications where an external resistance in series with the ARINC inputs is required for lightning protection or when the digital outputs need to be a logic zero rather than open circuit when TESTA and TESTB are both high.

See Holt Application Note AN-300 for more information on lightning protection.

FEATURES

- Direct ARINC 429 line receiver interface in a small outline package
- Receiver input hystersis at least 2 volts
- Test inputs that bypass analog input and can power down and tri-state outputs
- Plastic and ceramic package options surface mount and DIP
- Mil processing available

PIN CONFIGURATION



8 - PIN PLASTIC NARROW BODY SOIC

SUPPLY VOLTAGES

VCC = 5.0V ± 5%

FUNCTION TABLE

RECEIVER

RINA	RINB	TESTA	TESTA TESTB		ROUTB	
-1.25V to 1.25V	-1.25V to 1.25V	0	0	0	0	
-3.25V to -6.5V	3.25V to 6.5V	0	0	0	1	
3.25V to 6.5V	-3.25V to -6.5V	0	0	1	0	
Х	Х	0	1	0	1	
Х	Х	1	0	1	0	
Х	Х	1	1	HI-Z	HI-Z	

PIN DESCRIPTION TABLE

PIN	SYMBOL	FUNCTION	DESCRIPTION
1	VCC	SUPPLY	5 VOLT SUPPLY
2	TESTA	LOGIC INPUT	CMOS
3	RINB	ARINC INPUT	RECEIVER B INPUT
4	RINA	ARINC INPUT	RECEIVER A INPUT
5	GND	POWER	GROUND
6	ROUTA	LOGIC OUTPUT	RECEIVER CMOS OUTPUT A
7	ROUTB	LOGIC OUTPUT	RECEIVER CMOS OUTPUT B
8	TESTB	LOGIC INPUT	CMOS

FUNCTIONAL DESCRIPTION

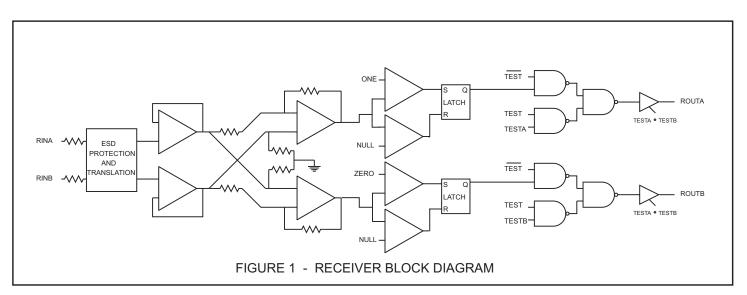
RECEIVER

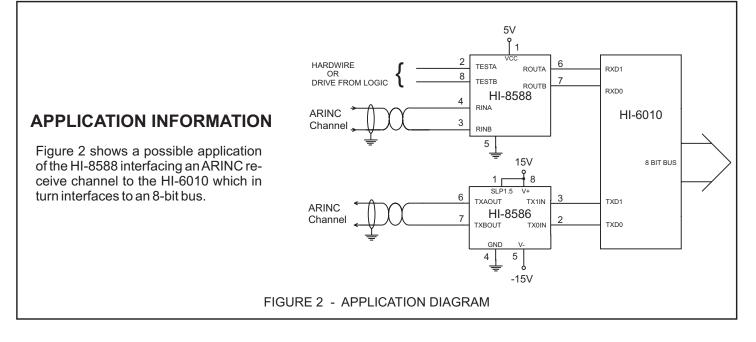
Figure 1 shows the general architecture of the ARINC 429 receiver. The receiver operates off the VCC supply only. The inputs RINA and RINB each have series resistors, typically 35K ohms. They connect to level translators whose resistance to Ground is typically 10K ohms. Therefore, any series resistance added to the inputs will affect the voltage translation.

After level translation, the inputs are buffered and become inputs to a differential amplifier. The amplitude of the differential signal is compared to levels derived from a divider between VCC and Ground. The nominal settings correspond to a One/Zero amplitude of 6.0V and a Null amplitude of 3.3V.

The status of the ARINC receiver input is latched. A Null input resets the latches and a One or Zero input sets the latches.

The logic at the output is controlled by the test signal which is generated by the logical OR of the TESTA and TESTB pins. If TESTA and TESTB are both One, then the receiver is powered down and the output pins float. The powerdown does not disconnect the internal resistors at the ARINC input.





HOLT INTEGRATED CIRCUITS 2

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to Ground

Supply voltages VCC7V
ARINC input - pins 3 & 4 Voltage at either pin+29V to -29V
DC current per input pin ±10mA
Power dissipation at 25°C plastic DIP0.7W ceramic DIP0.5W
Solder Temperature275°C for 10 sec
Storage Temperature65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltages VCC.....5V ± 5%

Industrial Screening......-40°C to +85°C Hi-Temp Screening......-55°C to +125°C Military Screening......-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC ELECTRICAL CHARACTERISTICS

OPERATING TEMPERATURE RANGE, VCC = 5.0V UNLESS OTHERWISE STATED

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	ТҮР	MAX	UNITS
ARINC input voltage						
one or zero	V _{DIN}	differential voltage, pins 3 & 4	6.5	10	13	volts
null	V _{NIN}		-	-	2.5	volts
common mode	V _{COM}	with respect to Ground	-	-	5.0	volts
logic input voltage						
high	∨ _{IH}		3.5	-	-	volts
low	V IL		-	-	1.5	volts
ARINC input resistance						
RINA to RINB	RDIFF	supplies floating	30	75	-	Kohm
RINA or RINB to Gnd or VCC	R _{SUP}	11 11	19	40	-	Kohm
logic input current						
source	Гін	$V_{IN} = 0 V$	-	-	0.1	μA
sink	I IL	$V_{IN} = 5 V$	-	-	0.1	μA
logic output drive current						
one	ГОН	V _{OH} = 4.6V	-	-1.6	-0.8	mA
zero	I OL	$V_{OL} = 0.4V$	3.6	5.6	-	mA
Current drain						
operating	I CC1	pins 2, 8 = 0V; pins 3, 4 open	-	2.3	6.3	mA
powerdown	I CC2	pins 2, 8 = 5V; pins 3, 4 open	-	0.36	0.6	mA

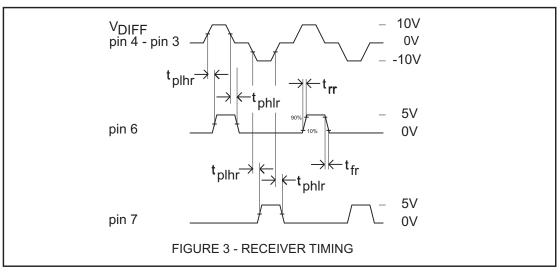
HI-8588

AC ELECTRICAL CHARACTERISTICS

OPERATING TEMPERATURE RANGE, VCC = 5.0V UNLESS OTHERWISE STATED

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	ТҮР	MAX	UNITS
Receiver propagation delay Output high to low Output low to high	t _{phlr} t _{plhr}	defined in Figure 3, C _L = 50pF	-	600 600	-	ns ns
Receiver output transition times Output high to low Output low to high	t fr t _{rr}		-	50 50	80 80	ns ns
Input capacitance (1) ARINC differential ARINC single ended to Ground Logic	C _{AD} C _{AS} C _{IN}		- - -	5 - -	10 10 10	pF pF pF

Notes: 1. Guaranteed but not tested



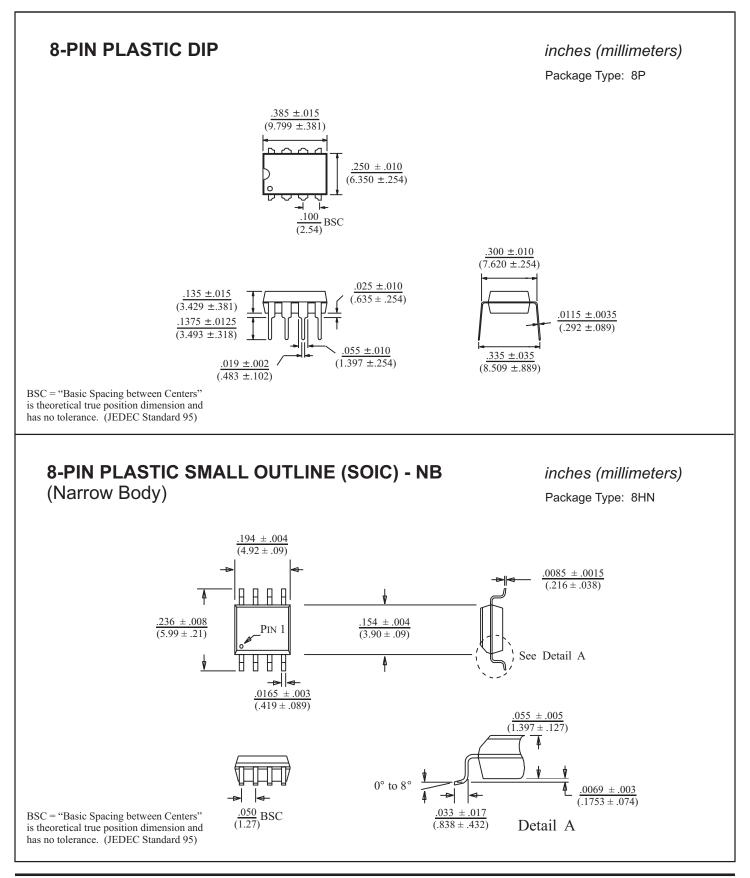
ORDERING INFORMATION

HI - 8588 x	ххх							
_	ΓΤΤ	PART NUMBER	LEAD FINISH					
		Blank	Tin / Lead (Sn / Pb) Solder100% Matte Tin (Pb-free, RoHS compliant)					
		F						
		PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN			
		I	-40°C TO +85°C	I	No			
		Т	-55°C TO +125°C					
		М	-55°C TO +125°C	-55°C TO +125°C M Yes				
		PART NUMBER	PACKAGE DESCRIPTION					
		PD	8 PIN PLASTIC DIP (8P) not available with "M" flow					
		PS	8 PIN PLASTIC NARROW BODY SOIC (8HN)					
		CR	8 PIN CERDIP (8D) not available Pb-free					

HOLT INTEGRATED CIRCUITS



HI-8588 PACKAGE DIMENSIONS



HOLT INTEGRATED CIRCUITS

HI-8588 PACKAGE DIMENSIONS

