

# **CMOS Static RAM**

## IDT61298SA/TTSA

#### Features

- 64K x 4 high-speed static RAM
- Fast Output Enable (OE) pin available for added system flexibility
- ٠ High speed (equal access and cycle times) - Commercial: 12/15 ns (max.)
- JEDEC standard pinout
- 300 mil 28-pin SOJ
- Produced with advanced CMOS technology
- Bidirectional data inputs and outputs
- Inputs/Outputs TTL-compatible
- Three-state outputs
- ٠ Military product compliant to MIL-STD-883, Class B

#### Description

The IDT61298SA is a 262,144-bit high-speed static RAM organized as 64K x 4. It is fabricated using IDT's high-performance, high-reliability

## Functional Block Diagram

CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective approach for memory intensive applications.

The IDT61298SA features two memory control functions: Chip Select  $(\overline{CS})$  and Output Enable  $(\overline{OE})$ . These two functions greatly enhance the IDT61298SA's overall flexibility in high-speed memory applications.

Access times as fast as 12ns are available. The IDT61298SA offers a reduced power standby mode, ISB1, which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability.

All inputs and outputs are TTL-compatible and the device operates from a single 5V supply. Fully static asynchronous circuitry, along with matching access and cycle times, favor the simplified system design approach.

The IDT61298SA is packaged in a 300 mil, 28-pin SOJ, providing improved board-level packing densities.



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#### CMOS Static RAM 256K (64K x 4-Bit)

#### **Commercial Temperature Range**

## Pin Configuration



#### **Pin Descriptions**

Name	Description		
Ao - A14 Addresses			
I/O0 - I/O7	Data Input/Output		
CS	Chip Select		
WE	Write Enable		
ŌĒ	Output Enable		
GND	Ground		
Vcc	Power		

2971 tbl 01

### Truth Table<sup>(1,2)</sup>

<u>C</u> S	ŌĒ	WE	I/O <b>Function</b>	
L	L	Н	DATAOUT Read Data	
L	Х	L	DATAN Write Data	
L	Н	Н	High-Z	Outputs Disabled
Н	Х	Х	High-Z Deselected - Standby	
VHC <sup>(3)</sup>	Х	Х	High-Z Deselected - Standby	

#### NOTES:

1.  $H = V_{IH}$ ,  $L = V_{IL}$ , x = Don't care.

2. VLC = 0.2V, VHC = VCC -0.2V.

3. Other inputs  $\geq$ VHC or  $\leq$ /LC.

Symbol	Rating	Com'l.	Unit
Vterm <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
Та	Operating Temperature	0 to +70	٥C
Tbias	Temperature Under Bias	-55 to +125	٥C
Tstg	Storage Temperature	-55 to +125	٥C
PT Power Dissipation		1.0	W
Ιουτ	DC Output Current	50	mA

### Absolute Maximum Ratings<sup>(1)</sup>

#### NOTES:

 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. VTERM must not exceed Vcc + 0.5V.

#### Capacitance

(TA = +25°C, f = 1.0MHz, SOJ Package)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
Cin	Input Capacitance	Vin = 3dV	5	pF
Соит	Output Capacitance	Vout = 3dV	7	pF
				2971 tbl 04

#### NOTE:

1. This parameter is determined by device characterization, but is not production tested.

2971 tbl 02

2971 tbl 03

**Commercial Temperature Range** 

#### Recommended Operating Temperature and Supply Voltage

Grade	Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

2971 tbl 05

# Recommended DC Operating Conditions

Symbol	Parameter	Min.	Тур.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
Vih	Input High Voltage	2.2		Vcc + 0.5V	V
Vil	Input Low Voltage	-0.5(1)		0.8	V

NOTE:

2971 tbl 06

2971 tbl 07

1. VIL (min.) = -1.5V for pulse width less than 10ns, once per cycle.

## DC Electrical Characteristics<sup>(1)</sup> (Vcc = $5V \pm 10\%$ , VLc = 0.2V, VHc = Vcc - 0.2V)

		61298SA12	61298SA15	
Symbol	Parameter	Com'l.	Com'l.	Unit
ICC	Dynamic Operating Current $\overline{CS} \le VIL$ , Outputs Open, Vcc = Max., f = fmax <sup>(2)</sup>	160	140	mA
ISB	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$ , Vcc = Max., Outputs Open, f = fmax <sup>(2)</sup>	50	45	mA
ISB1		20	20	mA

NOTES:

1. All values are maximum guaranteed values.

2. fMAX = 1/trc (all address inputs are cycling at fMAX); f = 0 means no address input lines are changing.

## AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2971 tbl 08





\*Includes scope and jig capacitances

#### **DC Electrical Characteristics** $(VCC = 5.0V \pm 10\%)$

			IDT61298SA			
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Lu	Input Leakage Current	Vcc = Max., VIN = GND to Vcc			5	μA
Ilo	Output Leakage Current	Vcc = Max., $\overline{CS}$ = VIH, Vout = GND to Vcc			5	μA
Vol	Output Low Voltage	Iol = 8mA, Vcc = Min. Iol = 10mA, Vcc = Min.			0.4 0.5	V
Vон	Output High Voltage	IOH = -4mA, Vcc = Min.	2.4	_	_	V

2971 tbl 09

# AC Electrical Characteristics ( $Vcc = 5.0V \pm 10\%$ )

		61298	ISA12	61298SA15		
Symbol	Parameter	Min.	Мах.	Min.	Max.	Unit
Read Cy	cle	-				
trc	Read Cycle Time	12		15		ns
taa	Address Access Time		12		15	ns
tacs	Chip Select Access Time	_	12		15	ns
talz(1)	Chip Select to Output in Low-Z	4	_	4	—	ns
tcHz <sup>(1)</sup>	Chip Deselect to Output in High-Z	_	6		7	ns
toe	Output Enable to Output Valid		6		7	ns
tolz <sup>(1)</sup>	Output Enable to Output in Low-Z	0	_	0		ns
tонz <sup>(1)</sup>	Output Disable to Output in High-Z		6		6	ns
toн	Output Hold from Address Change	3		3		ns
tpu <sup>(1)</sup>	Chip Select to Power-Up Time	0		0		ns
tpd <sup>(1)</sup>	Chip Deselect to Power-Down Time		12		15	ns
Write Cy	cle					
twc	Write Cycle Time	12	_	15		ns
tcw	Chip Select to End-of-Write	9		10		ns
taw	Address Valid to End-of-Write	9		10		ns
tas	Address Set-up Time	0	_	0	—	ns
twp	Write Pulse Width	9	_	10		ns
twr	Write Recovery Time		_	0		ns
tow	Data Valid to End-of-Write		_	7	—	ns
tDH	Data Hold Time			0	—	ns
twnz <sup>(1)</sup>	Write Enable to Output in High-Z	—	6		6	ns
tow <sup>(1)</sup>	Output Active from End-of-Write	4		4		ns
NOTE:						2971 tbl 10

1. This parameter is guaranteed with AC test load (Figure 2) by device characterization, but is not production tested.

#### IDT61298SA CMOS Static RAM 256K (64K x 4-Bit) **Commercial Temperature Range** Timing Waveform of Read Cycle No. 1<sup>(1)</sup> -tRC -ADDRESS ton tAA ŌĒ t OE tohz <sup>(5)</sup> tolz $^{(5)}$ CS t ACS t CHZ<sup>(5)</sup> t CLZ<sup>(5)</sup> DATAOUT DATA VALID

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Timing Waveform of Read Cycle No. 2<sup>(1,2,4)</sup>



## Timing Waveform of Read Cycle No. 3<sup>(1,3,4)</sup>



#### NOTES:

- 1.  $\overline{\text{WE}}$  is HIGH for Read cycle.
- 2. Device is continuously selected,  $\overline{\text{CS}}$  is LOW.
- 3. Address valid prior to or coincident with  $\overline{\text{CS}}$  transition LOW.
- 4.  $\overline{OE}$  is LOW.
- 5. Transition is measured  $\pm 200 \text{mV}$  from steady state.

# Timing Waveform of Write Cycle No. 1 (WE Controlled Timing)<sup>(1,2,4)</sup>



# Timing Waveform of Write Cycle No. 2 (CS Controlled Timing)<sup>(1,4)</sup>



#### NOTES:

- 1. A write occurs during the overlap of a LOW  $\overline{\text{CS}}$  and a LOW  $\overline{\text{WE}}$ .
- 2. OE is continuously HIGH. If OE is LOW during a WE controlled write cycle, the write pulse width must be the greater than or equal to twHz + tbw to allow the I/O drivers to turn off and data to be placed on the bus for the required tbw. If OE is HIGH during a WE controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the spectified twp.
- 3. During this period, I/O pins are in the output state so that the input signals must not be applied.
- 4. If the CS LOW transition occurs simultaneously with or after the WE LOW transition, the outputs remain in a high-impedance state.
- 5. Transition is measured ±200mV from steady state.



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## Datasheet Document History

11/22/99:		Updated to new format
	Pg. 6	Removed Note No. 1 Write Cycle No. 1 diagram, renumbered notes and footnotes
	Pg. 7	Added Datasheet Document History
08/09/00		Not recommended for new designs
02/01/01		Removed "Not recommended for new designs"
02/14/07	Pg. 7	Added TT generation die step to data sheet ordering information



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