5 VOLT BOOT BLOCK FLASH MEMORY

28F001BX (x8)

- **High-Integration Blocked Architecture**
  - **One 8 KB Boot Block w/Lock Out**
  - **Two 4 KB Parameter Blocks**
  - **One 112 KB Main Block**
- **Simplified Program and Erase**
  - **Automated Algorithms via On-Chip Write State Machine (WSM)**
- **SRAM-Compatible Write Interface**
- **Deep Power-Down Mode**
  - **0.05 µA I_{CC} Typical**
  - **0.8 µA I_{PP} Typical**
- **12.0 V ±5% V_{PP}**
- **High-Performance Read**
  - **120 ns, 150 ns Maximum Access Time**
  - **5.0 V ±10% V_{CC}**
- **Hardware Data Protection Feature**
  - **Erase/Write Lockout during Power Transitions**
- **Advanced Packaging, JEDEC Pinouts**
  - **32-Pin PDIP**
  - **32-Lead PLCC**
- **ETOX™ II Nonvolatile Flash Technology**
  - **EPROM-Compatible Process Base**
  - **High-Volume Manufacturing Experience**

The Intel® 28F001BX-B and 28F001BX-T combine the cost-effectiveness of Intel standard flash memory with features that simplify write and allow block erase. These devices aid the system designer by combining the functions of several components into one, making boot block flash an innovative alternative to EPROM and EEPROM or battery-backed static RAM. Many new and existing designs can take advantage of the 28F001BX's integration of blocked architecture, automated electrical reprogramming, and standard processor interface.

The 28F001BX-B and 28F001BX-T are 1,048,576 bit nonvolatile memories organized as 131,072 bytes of eight bits. They are offered in 32-pin plastic DIP and 32-lead PLCC packages. Pin assignment conform to JEDEC standards for byte-wide EPROMs. These devices use an integrated command port and state machine for simplified block erasure and byte reprogramming. The 28F001BX-T's block locations provide compatibility with microprocessors and microcontrollers that boot from high memory, such as Intel® MCS®-186 family, 80286, i386™, i486™, i860™ and 80960CA. With exactly the same memory segmentation, the 28F001BX-B memory map is tailored for microprocessors and microcontrollers that boot from low memory, such as Intel's MCS-51, MCS-196, 80960KX and 80960SX families. All other features are identical, and unless otherwise noted, the term 28F001BX can refer to either device throughout the remainder of this document.

The boot block section includes a reprogramming write lock out feature to guarantee data integrity. It is designed to contain secure code which will bring up the system minimally and download code to the other locations of the 28F001BX. Intel 28F001BX employs advanced CMOS circuitry for systems requiring high-performance access speeds, low-power consumption, and immunity to noise. Its access time provides zero wait-state performance for a wide range of microprocessors and microcontrollers. A deep power-down mode lowers power consumption to 0.25 µW typical through V_{CC}—crucial in laptop computer, hand-held instrumentation and other low-power applications. The RP# power control input also provides absolute data protection during system power-up or power loss.

Manufactured on Intel® ETOX™ process technology base, the 28F001BX builds on years of EPROM experience to yield the highest levels of quality, reliability, and cost-effectiveness.

Note: This document formerly known as *1-Mbit (128K x 8) Boot Block Flash Memory*.

December 1998

Order Number: 290406-009

INTEL CONFIDENTIAL
(until publication date)

Information in this document is provided in connection with Intel products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

The 28F001BX-T/28F001BX-B may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 5937
Denver, CO 8021-9808

or call 1-800-548-4725
or visit Intel's website at http://www.intel.com

 CG-041493

*Third-party brands and names are the property of their respective owners.

CONTENTS

PAGE

1.0 APPLICATIONS 5

2.0 PRINCIPLES OF OPERATION 10
2.1 Command Register and Write Automation . 11
2.2 Data Protection 11

3.0 BUS OPERATION 11
3.1 Read 12
3.2 Output Disable 12
3.3 Standby 12
3.4 Deep Power-Down 13
3.5 Intelligent Identifier Operation 13
3.5.1 Programming Equipment 13
3.5.2 In-System Programming 13
3.6 Write 13

4.0 COMMAND DEFINITIONS 13
4.1 Read Array Command 13
4.2 Intelligent Identifier Command for In-System Programming 14
4.3 Read Status Register Command 15
4.4 Clear Status Register Command 15
4.5 Erase Setup/Erase Confirm Commands 15
4.6 Erase Suspend/Erase Resume Commands 15
4.7 Program Setup/Program Commands 17

5.0 EXTENDED ERASE/PROGRAM CYCLING . 17

6.0 ON-CHIP PROGRAMMING ALGORITHM 17

PAGE

7.0 ON-CHIP ERASE ALGORITHM 17

8.0 BOOT BLOCK PROGRAM AND ERASE 18
8.1 In-System Operation 18
8.1.1 Programming Equipment 18

9.0 DESIGN CONSIDERATIONS 22
9.1 Power Supply Decoupling 22
9.2 V_{PP} Trace on Printed Circuit Boards 22
9.3 V_{CC}, V_{PP}, RP# Transitions and the Command/Status Registers 22
9.4 Power-Up/Down Protection 22
9.5 28F001BX Power Dissipation 23

10.0 ELECTRICAL SPECIFICATIONS 24
10.1 Absolute Maximum Ratings 24
10.2 Operating Conditions 24
10.3 Capacitance 24
10.4 DC Characteristics 25
10.5 AC Characteristics—Read-Only Operations 29
10.6 AC Characteristics—Write/Erase/Program Operations 31
10.6.1 PROM Programmer Specifications 32
10.7 Erase and Programming Performance 32
10.8 AC Characteristics—CE#-Controlled Write Operations 36
10.8.1 PROM Programmer Specifications 37

11.0 ORDERING INFORMATION 39

12.0 ADDITIONAL INFORMATION 39

REVISION HISTORY

Number	Description
-004	Removed **Preliminary** classification. Latched address A_{16} in Figure 5. Updated Boot Block Program and Erase section: "If boot block program or erase is attempted while RP# is at V_{IH}, **either the Program Status or Erase Status bit will be set to '1,' reflective of the operation being attempted and indicating boot block lock.**" Updated Figure 11, *28F001BX Erase Suspend/Resume Flowchart.* Added DC Characteristics typical current values. Combined V_{PP} Standby current and V_{PP} Read current into one V_{PP} Standby current spec with two test conditions (DC Characteristics table). Added maximum program/erase times to Erase and Programming Performance table. Added Figures 13–16. Added Extended Temperature proliferations.
-005	$\overline{PWD}$ changed to RP# for JEDEC standardization compatibility. Revised symbols, i.e.; $\overline{CE}$, $\overline{OE}$, etc. to CE#, OE#, etc.
-006	Added specifications for –90 and –70 product versions. Added V_{OH} CMOS Specification.
-007	Added reference to 28F001BN.
-008	Removed Extended Temperature products. Removed 70 ns and 90 ns speeds. Removed TSOP package. Updated *Erase Suspend/Resume Flowchart.* Updated *Ordering Information* table.
-009	Removed reference to 28F001BN. Changed I_{CCD} typical and maximum current values

1.0 APPLICATIONS

The Intel® 28F001BX Flash Boot Block memory augments the nonvolatility, in-system electrical erasure and reprogrammability of Intel's flash memory by offering four separately erasable blocks and integrating a state machine to control erase and program functions. The specialized blocking architecture and automated programming of the 28F001BX provide a full-function, non-volatile flash memory ideal for a wide range of applications, including PC boot/BIOS memory, minimum-chip embedded program memory and parametric data storage. The 28F001BX combines the safety of a hardware-protected 8-Kbyte boot block with the flexibility of three separately reprogrammable blocks (two 4-Kbyte parameter blocks and one 112-Kbyte code block) into one versatile, cost-effective flash memory. Additionally, reprogramming one block does not affect code stored in another block, ensuring data integrity.

The flexibility of flash memory reduces costs throughout the life cycle of a design. During the early stages of a system's life, flash memory reduces prototype development and testing time, allowing the system designer to modify in-system software electrically versus manual removal of components. During production, flash memory provides flexible firmware for just-in-time configuration, reducing system inventory and eliminating unnecessary handling and less reliable socketed connections. Late in the life cycle, when software updates or code "bugs" are often unpredictable and costly, flash memory reduces update costs by allowing the manufacturers to send floppy updates versus a technician. Alternatively, remote updates over a communication link are possible at speeds up to 9600 baud due to flash memory's fast programming time.

Reprogrammable environments, such as the personal computer, are ideal applications for the 28F001BX. The internal state machine provides SRAM-like timings for program and erasure, using the command and status registers. The blocking scheme allows BIOS update in the main and parameter blocks, while still providing recovery code in the boot block in the unlikely event a power failure occurs during an update, or where BIOS code is corrupted. Parameter blocks also provide convenient configuration storage, backing up SRAM and battery configurations. EISA systems, for example, can store hardware configurations in a flash parameter block, reducing system SRAM.

Laptop BIOS are becoming increasingly complex with the addition of power management software and extended system setup screens. BIOS code complexity increases the potential for code updates after the sale, but the compactness of laptop designs makes hardware updates very costly. Boot block flash memory provides an inexpensive update solution for laptops, while reducing laptop obsolescence. For portable PCs and hand-held equipment, the deep power-down mode dramatically lowers system power requirements during periods of slow operation or sleep modes.

The 28F001BX gives the embedded system designer several desired features. The internal state machine reduces the size of external code dedicated to the erase and program algorithms, as well as freeing the microcontroller or microprocessor to respond to other system requests during program and erasure. The four blocks allow logical segmentation of the entire embedded software: the 8-Kbyte block for the boot code, the 112-Kbyte block for the main program code and the two 4-Kbyte blocks for updatable parametric data storage, diagnostic messages and data, or extensions of either the boot code or program code. The boot block is hardware protected against unauthorized write or erase of its vital code in the field. Further, the power-down mode also locks out erase or write operations, providing absolute data protection during system power-up or power loss. This hardware protection provides obvious advantages for safety related applications such as transportation, military, and medical. The 28F001BX is well suited for minimum-chip embedded applications ranging from communications to automotive.

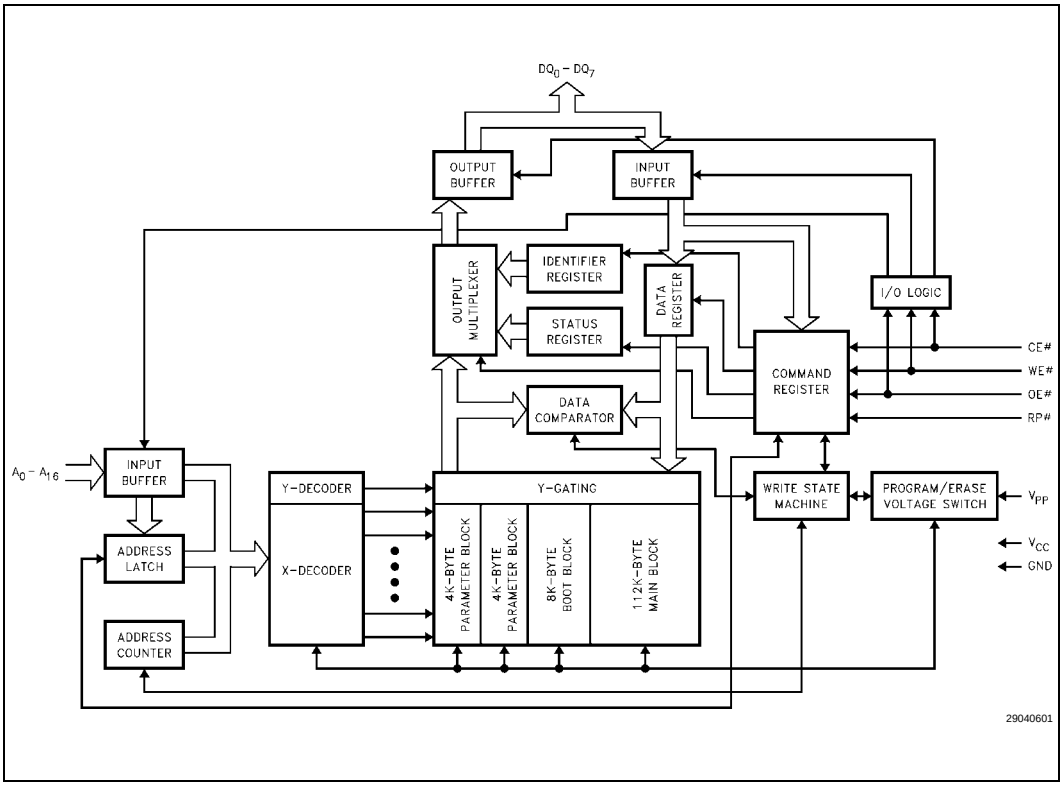


Figure 1. 28F001BX Block Diagram

Table 1. Lead Descriptions

Symbol	Type	Name and Function
A_0–A_{16}	INPUT	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle.
DQ_0–DQ_7	INPUT/ OUTPUT	**DATA INPUTS/OUTPUTS:** Inputs data and commands during memory write cycles; outputs data during memory, status register and identifier read cycles. The data pins are active high and float to tri-state off when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle.
CE#	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders and sense amplifiers. CE# is active low; CE# high deselects the memory device and reduces power consumption to standby levels.
RP#	INPUT	**POWERDOWN:** Puts the device in deep power-down mode. RP# is active low; RP# high gates normal operation. RP# = V_{HH} allows programming of the boot block. RP# also locks out erase or write operations when active low, providing data protection during power transitions. RP# active resets internal automation. Exit from deep power-down sets device to read array mode.
OE#	INPUT	**OUTPUT ENABLE:** Gates the device's outputs through the data buffers during a read cycle. OE# is active low. OE# = V_{HH} (pulsed) allows programming of the boot block.
WE#	INPUT	**WRITE ENABLE:** Controls writes to the command register and array blocks. WE# is active low. Addresses and data are latched on the rising edge of the WE# pulse.
V_{PP}		**ERASE/PROGRAM POWER SUPPLY** for erasing blocks of the array or programming bytes of each block. Note: With $V_{PP} < V_{PPL}$ max, memory contents cannot be altered.
V_{CC}		**DEVICE POWER SUPPLY:** (5 V ±10%)
GND		**GROUND**

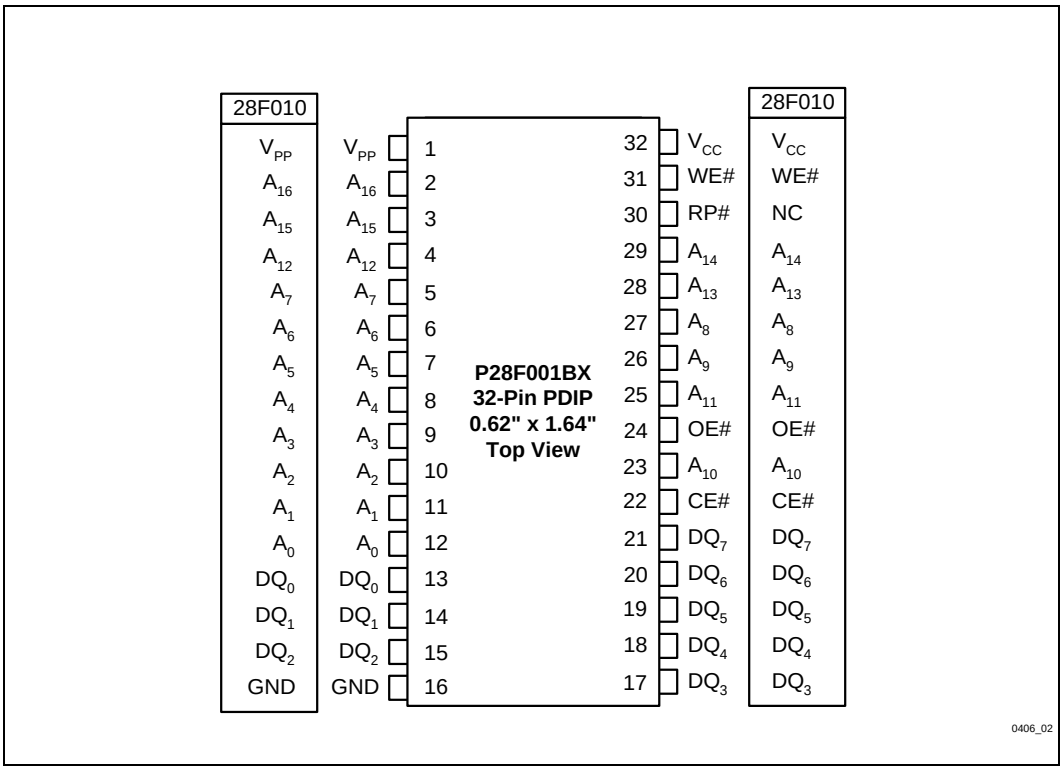


Figure 2. DIP Pin Configuration

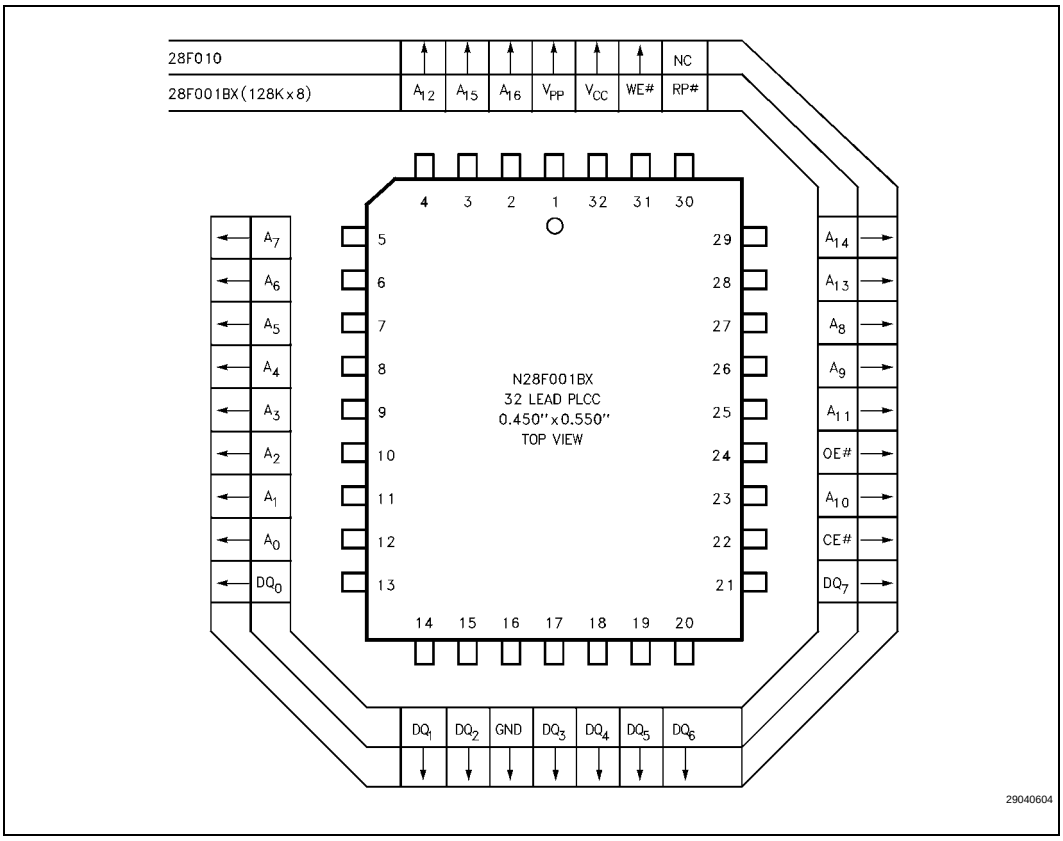


Figure 3. PLCC Lead Congfiguration

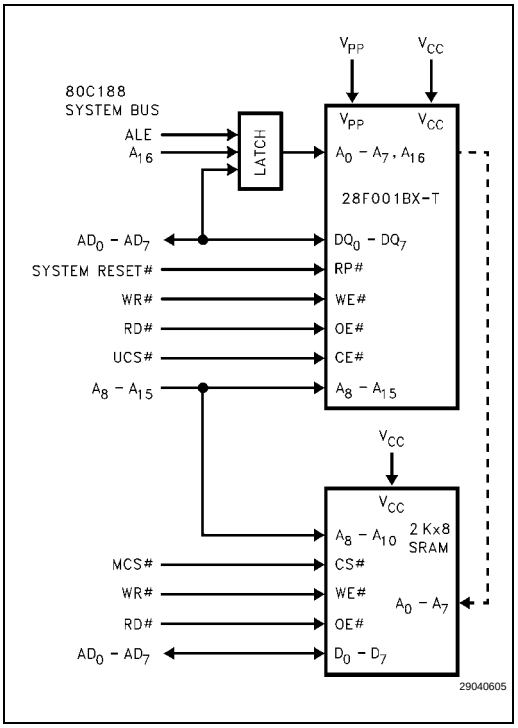


Figure 4. 28F001BX-T in a 80C188 System

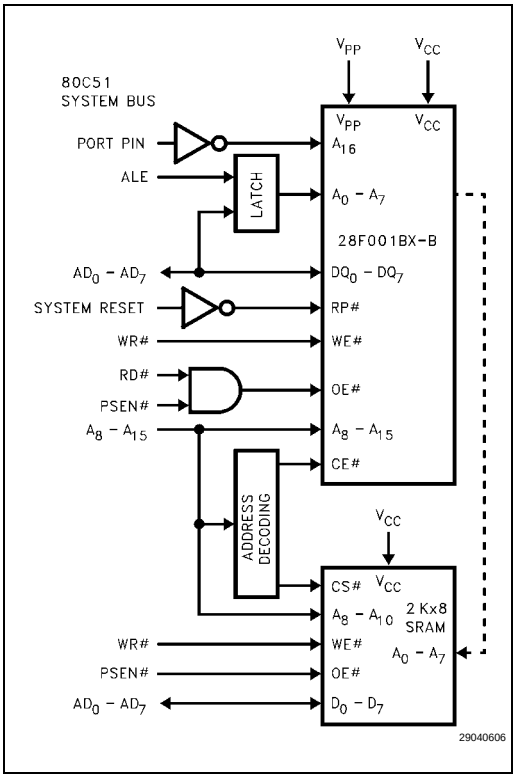


Figure 5. 28F001BX-B in a 80C51 System

2.0 PRINCIPLES OF OPERATION

The 28F001BX introduces on-chip write automation to manage write and erase functions. The write state machine allows for 100% TTL-level control inputs, fixed power supplies during erasure and programming, minimal processor overhead with RAM-like write timings, and maximum EPROM compatiblity.

After initial device power-up, or after return from deep power-down mode (see *Bus Operation*), the 28F001BX functions as a read-only memory. Manipulation of external memory-control pins yield standard EPROM read, standby, output disable or intelligent identifier operations. Both status register and intelligent identifiers can be accessed through the command register when $V_{PP} = V_{PPL}$.

This same subset of operations is also available when high voltage is applied to the V_{PP} pin. In addition, high voltage on V_{PP} enables successful erasure and programming of the device. All functions associated with altering memory contents—program, erase, status, and inteligent identifier—are accessed via the command register and verified through the status register.

Commands are written using standard microprocessor write timings. Register contents serve as input to the WSM, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for programming or erase operations. With the appropriate command written to the register, standard microprocessor read timings output array data, access the intelligent identifier codes, or output program and erase status for verification.

Interface software to initiate and poll progress of internal program and erase can be stored in any of the 28F001BX blocks. This code is copied to, and executed from, system RAM during actual flash memory update. After successful completion of program and/or erase, code execution out of the 28F001BX is again possible via the Read Array command. Erase suspend/resume capability allows system software to suspend block erase and read data/execute code from any other block.

2.1 Command Register and Write Automation

An on-chip state machine controls block erase and byte program, freeing the system processor for other tasks. After receiving the Erase Setup and Erase Confirm commands, the state machine controls block pre-conditioning and erase, returning progress via the status register. Programming is similarly controlled, after destination address and expected data are supplied. The program algorithm of past Intel Flash memories is now regulated by the state machine, including program pulse repetition where required and internal verification and margining of data.

2.2 Data Protection

Depending on the application, the system designer may choose to make the V_{PP} power supply switchable (available only when memory updates are required) or hardwired to V_{PPH}. When $V_{PP} = V_{PPL}$, memory contents cannot be altered. The 28F001BX command register architecture provides protection from unwanted program or erase operations even when high voltage is applied to V_{PP}. Additionally, all functions are disabled whenever V_{CC} is below the write lockout voltage V_{LKO}, or when RP# is at V_{IL}. The 28F001BX accommodates either design practice and encourages optimization of the processor-memory interface.

The two-step program/erase write sequence to the command register provides additional software write protection.

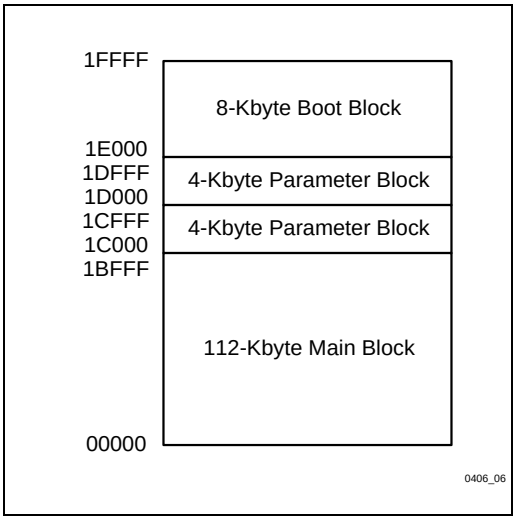


Figure 6. 28F001BX-T Memory Map

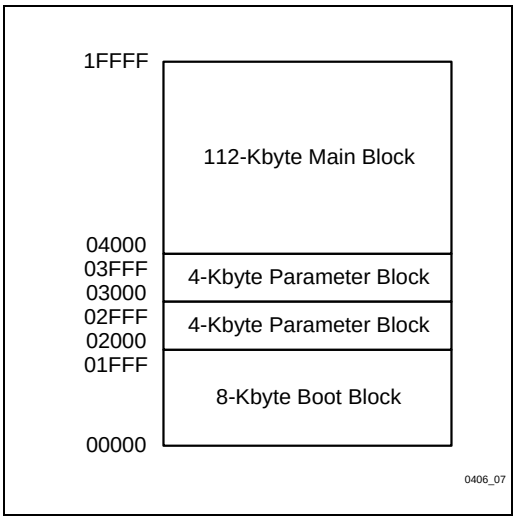


Figure 7. 28F001BX-B Memory Map

3.0 BUS OPERATION

Flash memory reads, erases and writes in-system via the local CPU. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

3.1 Read

The 28F001BX has three read modes. The memory can be read from any of its blocks, and information can be read from the intelligent identifier or the status register. V_{PP} can be at either V_{PPL} or V_{PPH}.

The first task is to write the appropriate Read Mode command to the command register (array, intelligent identifier, or status register). The 28F001BX automatically resets to read array mode upon initial device power-up or after exit from deep power-down. The 28F001BX has four control pins, two of which must be logically active to obtain data at the outputs. Chip Enable (CE#) is the device selection control, and when active enables the selected memory device. Output Enable (OE#) is the data input/output (DQ_0–DQ_7) direction control, and when active drives data from the selected memory onto the I/O bus. RP# and WE# must also be at V_{IH}. Figure 11 illustrates read bus cycle waveforms.

3.2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins (DQ_0–DQ_7) are placed in a high-impedance state.

3.3 Standby

CE# at a logic-high level (V_{IH}) places the 28F001BX in standby mode. Standby operation disables much of the 28F001BX's circuitry and substantially reduces device power consumption. The outputs (DQ_0–DQ_7) are placed in a high-impedance state independent of the status of OE#. If the 28F001BX is deselected during erase or program, the device will continue functioning and consuming normal active power until the operation is completed.

Table 2. 28F001BX Bus Operations

Mode	Notes	RP#	CE#	OE#	WE#	A_9	A_0	V_{PP}	DQ_{0-7}
Read	1, 2, 3	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	X	D_{OUT}
Output Disable	2	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	X	High Z
Standby	2	V_{IH}	V_{IH}	X	X	X	X	X	High Z
Deep Power Down	2	V_{IL}	X	X	X	X	X	X	High Z
Intelligent Identifier (Mfr)	2, 3, 4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IL}	X	89H
Intelligent Identifier (Device)	2, 3, 4, 5	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IH}	X	94H, 95H
Write	2, 6, 7, 8	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	X	D_{IN}

NOTES:

1. Refer to Section 10.4, *DC Characteristics*. When $V_{PP} = V_{PPL}$, memory contents can be read but not programmed or erased.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPL} or V_{PPH} for V_{PP}.
3. See *DC Characteristics*, for V_{PPL}, V_{PPH}, V_{HH} and V_{ID} voltages.
4. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3. A_1–A_8, A_{10}–$A_{16} = V_{IL}$.
5. Device ID = 94H for the 28F001BX-T and 95H for the 28F001BX-B.
6. Command writes involving block erase or byte program are successfully executed only when $V_{PP} = V_{PPH}$.
7. Refer to Table 3 for valid D_{IN} during a write operation.
8. Program or erase the boot block by holding RP# at V_{HH} or toggling OE# to V_{HH}. See AC waveforms for program/erase operations.

3.4 Deep Power-Down

The 28F001BX offers a 0.25 µW V_{CC} power-down feature, entered when RP# is at V_{IL}. During read modes, RP# low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. The 28F001BX requires time t_{PHQV} (see *AC Characteristics—Read-Only Operations*) after return from power-down until initial memory access outputs are valid. After this wakeup interval, normal operation is restored. The command register is reset to read array, and the status register is cleared to value 80H, upon return to normal operation.

During erase or program modes, RP# low will abort either operation. Memory contents of the block being altered are no longer valid as the data will be partially programmed or erased. Time t_{PHWL} after RP# goes to logic-high (V_{IH}) is required before another command can be written.

3.5 Intelligent Identifier Operation

The intelligent identifier operation outputs the manufacturer code, 89H; and the device code, 94H for the 28F001BX-T and 95H for the 28F001BX-B. Programming equipment or the system CPU can then automatically match the device with its proper erase and programming algorithms.

3.5.1 PROGRAMMING EQUIPMENT

CE# and OE# at a logic low level (V_{IL}), with A_9 at high voltage V_{ID} (see *DC Characteristics*) activates this operation. Data read from locations 00000H and 00001H represent the manufacturer's code and the device code respectively.

3.5.2 IN-SYSTEM PROGRAMMING

The manufacturer and device codes can also be read via the command register. Following a write of 90H to the command register, a read from address location 00000H outputs the manufacturer code (89H). A read from address 00001H outputs the device code (94H for the 28F001BX-T and 95H for the 28F001BX-B). It is not necessary to have high voltage applied to V_{PP} to read the intelligent identifiers from the command register.

3.6 Write

Writes to the command register allow read of device data and intelligent identifiers. They also control inspection and clearing of the status register. Additionally, when $V_{PP} = V_{PPH}$, the command register controls device erasure and programming. The contents of the register serve as input to the internal state machine.

The command register itself does not occupy an addressable memory location. The register is a latch used to store the command and address and data information needed to execute the command. Erase Setup and Erase Confirm commands require both appropriate command data and an address within the block to be erased. The Program Setup command requires both appropriate command data and the address of the location to be programmed, while the Program command consists of the data to be written and the address of the location to be programmed.

The command register is written by bringing WE# to a logic-low level (V_{IL}) while CE# is low. Addresses and data are latched on the rising edge of WE#. Standard microprocessor write timings are used.

Refer to *AC Characteristics—Write/Erase/Program Operations* and the *AC Waveform for Write Operations*, Figure 19, for specific timing parameters.

4.0 COMMAND DEFINITIONS

When V_{PPL} is applied to the V_{PP} pin, read operations from the status register, intelligent identifiers, or array blocks are enabled. Placing V_{PPH} on V_{PP} enables successful program and erase operations as well.

Device operations are selected by writing specific commands into the command register. Table 3 defines these 28F001BX commands.

4.1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the 28F001BX defaults to read array mode. This operation is also initiated by writing FFH into the command register.

Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered. Once the internal write state machine has started an erase or program operation, the device will not recognize the Read Array command, until the WSM has completed its operation. The Read Array command is functional when $V_{PP} = V_{PPL}$ or V_{PPH}.

4.2 Intelligent Identifier Command for In-System Programming

The 28F001BX contains an intelligent identifier operation to supplement traditional PROM-programming methodology. The operation is initiated by writing 90H into the command register. Following the command Write, a read cycle from address 00000H retrieves the manufacturer code of 89H. A read cycle from address 00001H returns the device code of 94H (28F001BX-T) or 95H (28F001BX-B). To terminate the operation, it is necessary to write another valid command into the register. Like the Read Array command, the Intelligent Identifier command is functional when $V_{PP} = V_{PPL}$ or V_{PPH}.

Table 3. 28F001BX Command Definitions

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Operation	Address	Data	Operation	Address	Data
Read Array/Reset	1	1	Write	X	FFH			
Intelligent Identifier	3	2, 3, 4	Write	X	90H	Read	IA	IID
Read Status Register	2	3	Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Erase Setup/Erase Confirm	2	2	Write	BA	20H	Write	BA	D0H
Erase Suspend/ Erase Resume	2		Write	X	B0H	Write	X	D0H
Program Setup/ Program	2	2, 3	Write	PA	40H	Write	PA	PD

NOTES:

1. Bus operations are defined in Table 2.
2. IA = Identifier Address: 00H for manufacturer code, 01H for device code.
   BA = Address within the block being erased.
   PA = Address of memory location to be programmed.
3. SRD = Data read from status register. See Table 4 for a description of the status register bits.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of WE#.
   IID = Data read from intelligent identifiers.
4. Following the Intelligent Identifier command, two read operations access manufacture and device codes.
5. Commands other than those shown above are reserved by Intel for future device implementations and should not be used.

4.3 Read Status Register Command

The 28F001BX contains a status register which may be read to determine when a program or erase operation is complete, and whether that operation completed successfully. The status register may be read at any time by writing the Read Status Register command (70H) to the command register. After writing this command, all subsequent read operations output data from the status register, until another valid command is written to the command register. The contents of the status register are latched on the falling edge of OE# or CE#, whichever occurs last in the read cycle. OE# or CE# must be toggled to V_{IH} before further reads to update the status register latch. The Read Status Register command functions when $V_{PP} = V_{PPL}$ or V_{PPH}.

4.4 Clear Status Register Command

The erase status and program status bits are set to "1" by the Write State Machine and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 4). By allowing system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several bytes or erasing multiple blocks in sequence). The status register may then be polled to determine if an error occurred during that series. This adds flexibility to the way the device may be used.

Additionally, the V_{PP} status bit (SR.3), when set to "1," **must** be reset by system software before further byte programs or block erases are attempted. To clear the status register, the Clear Status Register command (50H) is written to the command register. The Clear Status Register command is functional when $V_{PP} = V_{PPL}$ or V_{PPH}.

4.5 Erase Setup/Erase Confirm Commands

Erase is executed one block at a time, initiated by a two-cycle command sequence. An Erase Setup command (20H) is first written to the command register, followed by the Erase Confirm command (D0H). These commands require both appropriate command data and an address within the block to be erased. Block preconditioning, erase and verify are all handled internally by the Write State Machine, invisible to the system. After receiving the two-command erase sequence, the 28F001BX automatically outputs status register data when read (see Figure 9, *28F001BX Block Erase Flowchart*). The CPU can detect the completion of the erase event by checking the WSM status bit of the status register (SR.7).

When the status register indicates that erase is complete, the erase status bit should be checked. If erase error is detected, the status register should be cleared. The command register remains in read status register mode until further commands are issued to it.

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, block erasure can only occur when $V_{PP} = V_{PPH}$. In the absence of this high voltage, memory contents are protected against erasure. If block erase is attempted while $V_{PP} = V_{PPL}$, the V_{PP} status bit will be set to "1". Erase attempts while $V_{PPL} < V_{PP} < V_{PPH}$ produce spurious results and should not be attempted.

4.6 Erase Suspend/Erase Resume Commands

The Erase Suspend command allows erase sequence interruption in order to read data from another block of memory. Once the erase sequence is started, writing the Erase Suspend command (B0H) to the command register requests that the WSM suspend the erase sequence at a predetermined point in the erase algorithm. The 28F001BX continues to output status register data when read, after the Erase Suspend command is written to it. Polling the WSM status and erase suspend status bits will determine when the erase operation has been suspended (both will be set to "1s").

At this point, a Read Array command can be written to the command register to read data from blocks **other than that which is suspended**. The only other valid commands at this time are Read Status Register (70H) and Erase Resume (D0H), at which time the WSM will continue with the erase sequence. The erase suspend status and WSM status bits of the status register will be cleared. After the Erase Resume command is written to it, the 28F001BX automatically outputs status register data when read (see Figure 10, *28F001BX Erase Suspend/ Resume Flowchart*).

Table 4. 28F001BX Status Register Definitions

WSMS	ESS	ES	PS	VPPS	R	R	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy

NOTES:
The WSM status bit must first be checked to determine program or erase completion, before the program or erase status bits are checked for success.

SR.6 = ERASE SUSPEND STATUS
1 = Erase Suspended
0 = Erase in Progress/Completed

If the program **and** erase status bits are set to "1s" during an erase attempt, an improper command sequence was entered. Attempt the operation again.

SR.5 = ERASE STATUS
1 = Error in Block Erasure
0 = Successful Block Erase

If V_{PP} low status is detected, the status register must be cleared before another program or erase operation is attempted.

SR.4 = PROGRAM STATUS
1 = Error in Byte Program
0 = Successful Byte Program

The V_{PP} status bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates the V_{PP} level only after the Program or Erase command sequences have been entered and informs the system if V_{PP} has not been switched on. The V_{PP} status bit is not guaranteed to report accurate feedback between V_{PPL} and V_{PPH}.

SR.3 = V_{PP} STATUS
1 = V_{PP} Low Detect; Operation Abort
0 = V_{PP} OK

SR.2–SR.0 = RESERVED FOR FUTURE ENHANCEMENTS

These bits are reserved for future use and should be masked out when polling the status register.

4.7 Program Setup/Program Commands

Programming is executed by a two-write sequence. The Program Setup command (40H) is written to the command register, followed by a second write specifying the address and data (latched on the rising edge of WE#) to be programmed. The WSM then takes over, controlling the program and verify algorithms internally. After the two-command program sequence is written to it, the 28F001BX automatically outputs status register data when read (see Figure 8, *28F001BX Byte Programming Flowchart*). The CPU can detect the completion of the program event by analyzing the WSM status bit of the status register. Only the Read Status Register command is valid while programming is active.

When the status register indicates that programming is complete, the program status bit should be checked. If program error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully program to "0"s. The command register remains in read status register mode until further commands are issued to it. If byte program is attempted while $V_{PP} = V_{PPL}$, the V_{PP} status bit will be set to "1." Program attempts while $V_{PPL} < V_{PP} < V_{PPH}$ produce spurious results and should not be attempted.

5.0 EXTENDED ERASE/PROGRAM CYCLING

EEPROM cycling failures have always concerned users. The high electrical field required by thin oxide EEPROMs for tunneling can literally tear apart the oxide at defect regions. To combat this, some suppliers have implemented redundancy schemes, reducing cycling failures to insignificant levels. However, redundancy requires that cell size be doubled; an expensive solution.

Intel has designed extended cycling capability into its ETOX flash memory technology. Resulting improvements in cycling reliability come without increasing memory cell size or complexity. First, an advanced tunnel oxide increases the charge carrying ability ten-fold. Second, the oxide area per cell subjected to the tunneling electrical field is one-tenth that of common EEPROMs, minimizing the probability of oxide defects in the region. Finally, the peak electric field during erasure is approximately 2 Mv/cm lower than EEPROM. The lower electric field greatly reduces oxide stress and the probability of failure.

The 28F001BX-B and 28F001BX-T are capable of 100,000 program/erase cycles on each parameter block, main block and boot block.

6.0 ON-CHIP PROGRAMMING ALGORITHM

The 28F001BX integrates the Quick-Pulse programming algorithm of prior Intel Flash memory devices on-chip, using the command register, status register and WSM. On-chip integration dramatically simplifies system software and provides processor-like interface timings to the command and status registers. WSM operation, internal program verify and V_{PP} high voltage presence are monitored and reported via appropriate status register bits. Figure 8 shows a system software flowchart for device programming. The entire sequence is performed with V_{PP} at V_{PPH}. Program abort occurs when RP# transitions to V_{IL}, or V_{PP} drops to V_{PPL}. Although the WSM is halted, byte data is partially programmed at the location where programming was aborted. Block erasure or a repeat of byte programming will initialize this data to a known value.

7.0 ON-CHIP ERASE ALGORITHM

As above, the quick-erase algorithm of prior Intel Flash memory devices is now implemented internally, including all preconditioning of block data. WSM operation, erase success and V_{PP} high voltage presence are monitored and reported through the status register. Additionally, if a command other than Erase Confirm is written to the device after Erase Setup has been written, both the erase status and program status bits will be set to "1". When issuing the Erase Setup and Erase Confirm commands, they should be written to an address within the address range of the block to be erased. Figure 9 shows a system software flowchart for block erase.

Erase typically takes 1–4 seconds per block. The Erase Suspend/Erase Resume command sequence allows interrupt of this erase operation to read data**from a block other than that in which erase is being performed**. A system software flowchart is shown in Figure 10.

The entire sequence is performed with V_{PP} at V_{PPH}. Abort occurs when RP# transitions to V_{IL} or V_{PP} falls to V_{PPL}, while erase is in progress. Block data is partially erased by this operation, and a repeat of erase is required to obtain a fully erased block.

8.0 BOOT BLOCK PROGRAM AND ERASE

The boot block is intended to contain secure code which will minimally bring up a system and control programming and erase of other blocks of the device, if needed. Therefore, additional "lockout" protection is provided to guarantee data integrity. Boot block program and erase operations are enabled through high voltage V_{HH} on either RP# or OE#, and the normal Program and Erase command sequences are used. Reference the AC waveforms for program/erase.

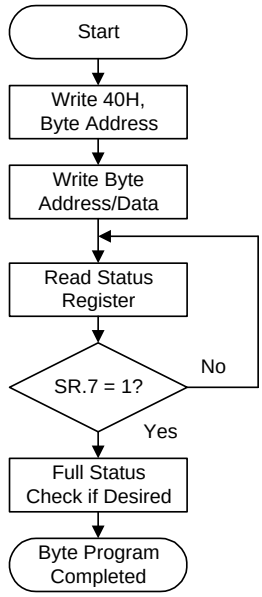
If boot block program or erase is attempted while RP# is at V_{IH}, either the program status or erase status bit will be set to "1", reflective of the operation being attempted and indicating boot block lock. Program/erase attempts while V_{IH} < RP# < V_{HH} produce spurious results and should not be attempted.

8.1 In-System Operation

For on-board programming, the RP# pin is the most convenient means of altering the boot block. Before issuing Program or Erase Confirm commands, RP# must transition to V_{HH}. Hold RP# at this high voltage throughout the program or erase interval (until after status register confirmation of successful completion). At this time, it can return to V_{IH} or V_{IL}.

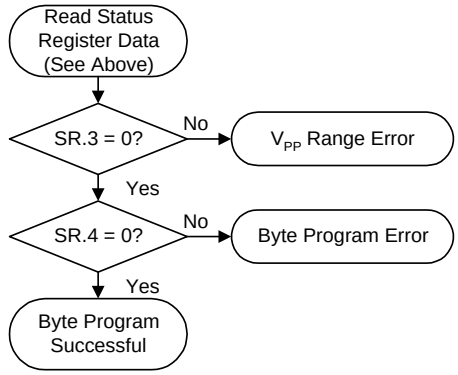
8.1.1 PROGRAMMING EQUIPMENT

For PROM programming equipment that cannot bring RP# to high voltage, OE# provides an alternate boot block access mechanism. OE# must transition to V_{HH} a minimum of 480 ns before the initial Program/Erase Setup command and held at V_{HH} at least 480 ns after Program or Erase Confirm commands are issued to the device. After this interval, OE# can return to normal TTL levels.



Bus Operation	Command	Comments
Write	Program Setup	Data = 40H Addr = Byte to Be Programmed
Write	Program	Data = Data to Be Programmed Addr = Byte to Be Programmed
Read		Status Register Data Toggle OE# or CE# to Update Status Register
Standby		Check SR.7 1 = Ready 0 = Busy
Repeat for subsequent bytes. Full status check can be done after each byte, or after a sequence of bytes. Write FFH after the last byte programming operation to reset the device to read array mode.		

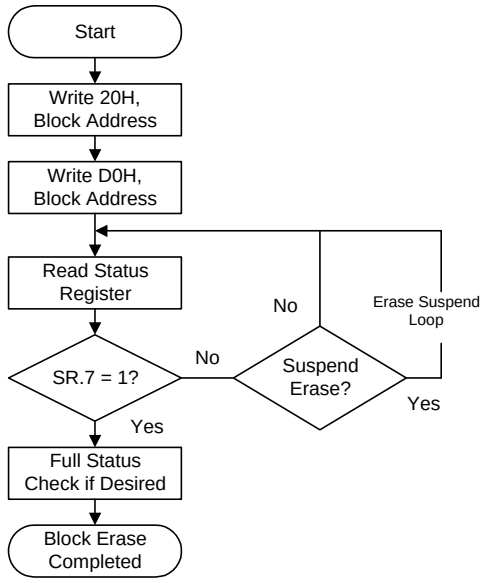
FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4 1 = Byte Program Error
SR.3 **must** be cleared, if set during a program attempt, before further attempts are allowed by the write state machine. SR.4 is only cleared by the Clear Status Register command in cases where multiple locations are programmed before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

0406_08

Figure 8. 28F001BX Byte Programming Flowchart



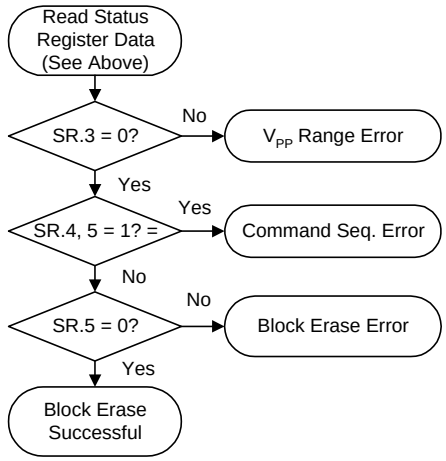
Bus Operation	Command	Comments
Write	Erase Setup	Data = 20H Addr = Within Block to Be Erased
Write	Erase	Data = D0H Addr = Within Block to Be Erased
Read		Status Register Data Toggle OE# or CE# to Update Status Register
Standby		Check SR.7 1 = Ready 0 = Busy

Repeat for subsequent blocks.

Full status check can be done after each block, or after a sequence of blocks.

Write FFH after the last block erase operation to reset the device to read array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error

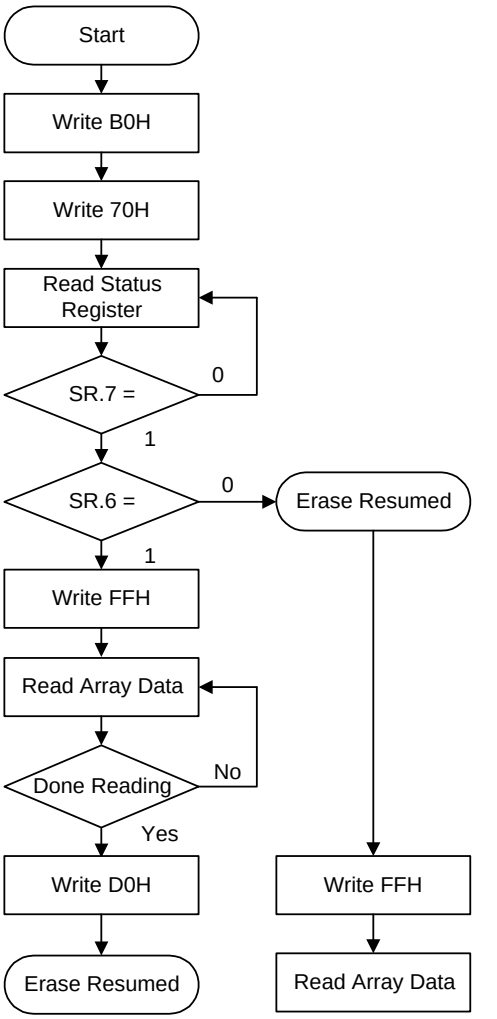
SR.3 **must** be cleared, if set during an erase attempt, before further attempts are allowed by the write state machine.

SR.5 is only cleared by the Clear Status Register command in cases where multiple blocks are erased before full status is checked.

If an error is detected, clear the status register before attempting retry or other error recovery.

0406_09

Figure 9. 28F001BX Block Erase Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H Addr = X
Write	Read Status	Data = 70H Addr = X
Read		Status Register Data Toggle OE# or CE# to Update Status Register Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Erase Suspended 0 = Erase Completed
Write	Read Array	Data = FFH Addr = X
Read		Read array data from block other than the one being programmed
Write	Erase Resume	Data = D0H Addr = X

Figure 10. 28F001BX Erase Suspend/Resume Flowchart

9.0 DESIGN CONSIDERATIONS

Flash memories are often used in larger memory arrays. Intel provides three control inputs to accommodate multiple memory connections. Three-line control provides for:

a) lowest possible memory power dissipation

b) complete assurance that data bus contention will not occur

To efficiently use these control inputs, an address decoder should enable CE#, while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. RP# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

9.1 Power Supply Decoupling

Flash memory power switching characteristics require careful device coupling. System designers are interested in three supply current issues; standby current levels (I_{SB}), active current levels (I_{CC}) and transient peaks producted by falling and rising edges of CE#. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between its V_{CC} and GND, and between its V_{PP} and GND. These high frequency, low inherent-inductance capacitors should be placed as close as possible to the device. Additionally, for every eight devices, a 4.7 µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

9.2 V_{PP} Trace on Printed Circuit Boards

Programming flash memories, while they reside in the target system, requires that the printed circuit board designer pay attention to the V_{PP} power supply trace. The V_{PP} pin supplies the memory cell current for programming. Use similar trace widths and layout considerations given to the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

9.3 V_{CC}, V_{PP}, RP# Transitions and the Command/Status Registers

Programming and erase completion are not guaranteed if V_{PP} drops below V_{PPH}. If the V_{PP} status bit of the status register (SR.3) is set to "1", a Clear Status Register command **must** be issued before further program/erase attempts are allowed by the WSM. Otherwise, the program (SR.4) or erase (SR.5) status bits of the status register will be set to "1" if error is detected. RP# transitions to V_{IL} during program and erase also abort the operations. Data is partially altered in either case, and the command sequence must be repeated after normal operation is restored. Device power-off, or RP# transitions to V_{IL}, clear the status register to initial value 80H.

The command register latches commands as issued by system software and is not altered by V_{PP} or CE# transitions or WSM actions. Its state upon power-up, after exit from deep power-down or after V_{CC} transitions below V_{LKO}, is FFH, or read array mode.

After program or erase is complete, even after V_{PP} transitions down to V_{PPL}, the command register must be reset to read array mode via the Read Array command if access to the memory array is desired.

9.4 Power-Up/Down Protection

The 28F001BX is designed to offer protection against accidental erasure or programming during power transitions. Upon power-up, the 28F001BX is indifferent as to which power supply, V_{PP} or V_{CC}, powers up first. Power supply sequencing is not required. Internal circuitry in the 28F001BX ensures that the command register is reset to read array mode on power-up.

A system designer must guard against spurious writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both WE# and CE# must be low for a command write, driving either to V_{IH} will inhibit writes. The command register architecture provides an added level of protection since alteration of memory contents only occurs after successful completion of the two-step command sequences.

Finally, the device is disabled, until RP# is brought to V_{IH}, regardless of the state of its control inputs. This provides an additional level of protection.

9.5 28F001BX Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash nonvolatility increases usable battery life because the 28F001BX does not consume any power to retain code or data when the system is off.

In addition, the 28F001BX's deep power-down mode ensures extremely low power dissipation even when system power is applied. For example, laptop and other PC applications, after copying BIOS to DRAM, can lower RP# to V_{IL}, producing negligible power consumption. If access to the boot code is again needed, as in case of a system RESET#, the part can again be accessed, following the t_{PHAV} wakeup cycle required after RP# is first raised back to V_{IH}. The first address presented to the device while in power-down requires time t_{PHAV}, after RP# transitions high, before outputs are valid. Further accesses follow normal timing. See *AC Characteristics—Read-Only Operations* and Figure 11 for more information.

10.0 ELECTRICAL SPECIFICATIONS

NOTICE: This is a production datasheet. The specifications are subject to change without notice.

10.1 Absolute Maximum Ratings*

Operating Temperature
During Read ..... 0 °C to 70 °C(1)
During Erase/Program ..... 0 °C to 70 °C(1)

Operating Temperature
During Read ..... –40 °C to +85 °C(2)
During Erase/Program ..... –40 °C to +85 °C(2)

Temperature under Bias ..... –10 °C to 80 °C (1)

Temperature under Bias ..... –20 °C to +90 °C (2)

Storage Temperature .....–65 °C to 125 °C

Voltage on Any Pin
(except A_9, RP#, OE#, V_{CC} and V_{PP})
with Respect to GND ..... –2.0 V to 7.0 V(3)

Voltage on A_9, RP#, and OE#
with Respect to GND .....–2.0 V to 13.5 V(3, 4)

V_{PP} Program Voltage
with Respect to GND
During Erase/Program .....–2.0 V to 14.0 V(3, 4)

V_{CC} Supply Voltage
with Respect to GND ..... –2.0 V to 7.0 V(3)

Output Short Circuit Current .....100 mA(5)

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. Operating temperature is for extended temperature product defined by this specification.
3. Minimum DC voltage is –0.5 V on input/output pins. During transitions, this level may undershoot to –2.0 V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} +0.5 V which, during transitions, may overshoot to V_{CC} + 2.0 V for periods <20 ns.
4. Maximum DC voltage on A_9 or V_{PP} may overshoot to +14.0 V for periods <20 ns.
5. Output shorted for no more than one second. No more than one output shorted at a time.

10.2 Operating Conditions

Symbol	Parameter	Min	Max	Unit
T_A	Operating Temperature(1)	0	70	°C
T_A	Operating Temperature(2)	–40	85	°C
V_{CC}	Supply Voltage	4.50	5.50	V

10.3 Capacitance(1)

T_A = 25 °C, F = 1 MHz

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Input Capacitance	8	pF	V_{IN} = 0 V
C_{OUT}	Output Capacitance	12	pF	V_{OUT} = 0 V

NOTE:

1. Sampled, not 100% tested.

10.4 DC Characteristics

V_{CC} = 5.0 V ±10%, T_A = 0 °C to +70 °C

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Conditions
I_{IL}	Input Load Current	1			±1.0	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current		1		±10	µA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current			1.2	2.0	mA	$V_{CC} = V_{CC}$ Max CE# = RP# = V_{IH}
				30	100	µA	$V_{CC} = V_{CC}$ Max CE# = RP# = V_{CC} ±0.2 V
I_{CCD}	V_{CC} Deep Power-Down Current	1		1.0	4.0	µA	RP# = GND ±0.2 V
I_{CCR}	V_{CC} Read Current	1		13	30	mA	$V_{CC} = V_{CC}$ Max, CE# = V_{IL} f = 8 MHz, I_{OUT} = 0 mA
I_{CCP}	V_{CC} Programming Current	1		5	20	mA	Programming in Progress
I_{CCE}	V_{CC} Erase Current	1		6	20	mA	Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	1, 2		5	10	mA	Erase Suspended CE# = V_{IH}
I_{PPS}	V_{PP} Standby Current	1		±1	±10	µA	$V_{PP} \leq V_{CC}$
				90	200	µA	$V_{PP} > V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1		0.80	1.0	µA	RP# = GND ±0.2 V
I_{PPP}	V_{PP} Programming Current	1		6	30	mA	$V_{PP} = V_{PPH}$ Programming in Progress
I_{PPE}	V_{PP} Erase Current	1		6	30	mA	$V_{PP} = V_{PPH}$ Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1		90	300	µA	$V_{PP} = V_{PPH}$ Erase Suspended
I_{ID}	A_9 Intelligent Identifier Current	1		90	500	µA	$A_9 = V_{ID}$
V_{IL}	Input Low Voltage		–0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	$V_{CC} = V_{CC}$ Min I_{OL} = 5.8 mA
V_{OH}	Output High Voltage		2.4			V	$V_{CC} = V_{CC}$ Min I_{OH} = 2.5 mA
V_{ID}	A_9 Intelligent Identifier Voltage		11.5		13.0	V	

10.4 DC Characteristics (Continued)

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Conditions
V_{PPL}	V_{PP} during Normal Operations	3	0.0		6.5	V	
V_{PPH}	V_{PP} during Prog/Erase Operations		11.4	12.0	12.6	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.5			V	
V_{HH}	RP#, OE# Unlock Voltage		11.4		12.6	V	Boot Block Prog/Erase

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0 V, V_{PP} = 12.0 V, T_A = 25 °C. These currents are valid for all product versions (packages and speeds).
2. I_{CCES} is specified with the device deselected. If the 28F001BX is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Erase/programs are inhibited when V_{PP} = V_{PPL} and not guaranteed in the range between V_{PPH} and V_{PPL}.

10.4 DC Characteristics (Continued)

V_{CC} = 5.0 V ±10%, T_A = –40 °C to +85 °C

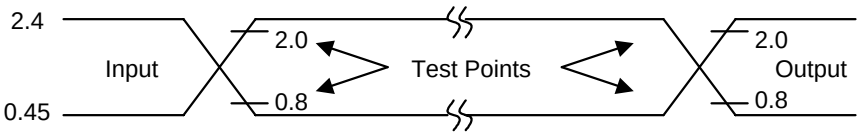
Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Conditions
I_{IL}	Input Load Current	1			±1.0	µA	V_{CC} = V_{CC} Max V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current	1			±10	µA	V_{CC} = V_{CC} Max V_{OUT} = V_{CC} or GND
I_{CCS}	V_{CC} Standby Current			1.2	2.0	mA	V_{CC} = V_{CC} Max CE# = RP# = V_{IH}
				30	150	µA	V_{CC} = V_{CC} Max CE# = RP# = V_{CC} ±0.2 V
I_{CCD}	V_{CC} Deep Power-Down Current	1		0.05	2.0	µA	RP# = GND ±0.2 V
I_{CCR}	V_{CC} Read Current	1		13	35	mA	V_{CC} = V_{CC} Max, CE# = V_{IL} f = 8 MHz, I_{OUT} = 0 mA
I_{CCP}	V_{CC} Programming Current	1		5	20	mA	Programming in Progress
I_{CCE}	V_{CC} Erase Current	1		6	20	mA	Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	1, 2		5	10	mA	Erase Suspended CE# = V_{IH}
I_{PPS}	V_{PP} Standby Current	1		±1	±15	µA	$V_{PP} \leq V_{CC}$
				90	400	µA	$V_{PP} > V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1		0.80	1.0	µA	RP# = GND ±0.2 V
I_{PPP}	V_{PP} Programming Current	1		6	30	µA	V_{PP} = V_{PP} Programming in Progress

10.4 DC Characteristics (Continued)

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Conditions
I_{PPE}	V_{PP} Erase Current	1		6	30	mA	$V_{PP} = V_{PPH}$ Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1		90	400	µA	$V_{PP} = V_{PPH}$ Erase Suspended
I_{ID}	A_9 Intelligent Identifier Current	1		90	500	µA	$A_9 = V_{ID}$
V_{IL}	Input Low Voltage		–0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	$V_{CC} = V_{CC}$ Min I_{OL} = 5.8 mA
V_{OH1}	Output High Voltage (TTL)		2.4			V	$V_{CC} = V_{CC}$ Min I_{OH} = 2.5 mA
V_{OH2}	Output High Voltage (CMOS)		0.85 V_{CC}			V	$V_{CC} = V_{CC}$ Min I_{OH} = –2.5 µA
			V_{CC} –0.4				$V_{CC} = V_{CC}$ Min I_{OH} = –100 µA
V_{ID}	A_9 Intelligent Identifier Voltage		11.5		13.0	V	
V_{PPL}	V_{PP} during Normal Operations	3	0.0		6.5	V	
V_{PPH}	V_{PP} during Prog/Erase Operations		11.4	12.0	12.6	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.5			V	
V_{HH}	RP#, OE# Unlock Voltage		11.4		12.6	V	Boot Block Prog/Erase

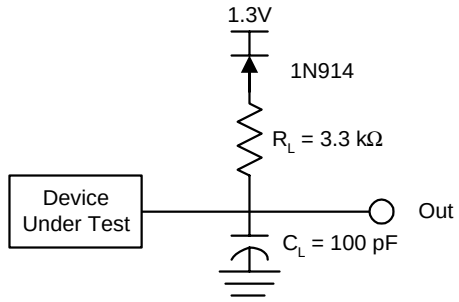
NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0 V, V_{PP} = 12.0 V, T_A = 25 °C. These currents are valid for all product versions (packages and speeds).
2. I_{CCES} is specified with the device deselected. If the 28F001BX is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Erase/programs are inhibited when $V_{PP} = V_{PPL}$ and not guaranteed in the range between V_{PPH} and V_{PPL}.



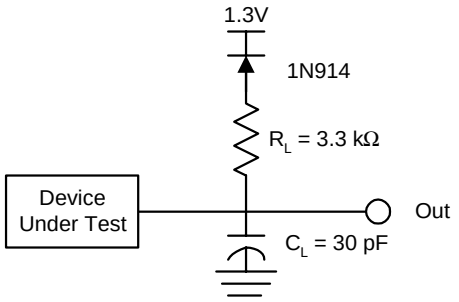
AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a Logic "1" and V_{OL} (0.45 V_{TTL}) for a Logic "0." Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) <10 ns.

Figure 11. AC Input/Output Reference Waveform



NOTE:
C_L Includes Jig Capacitance

Figure 12. Standard Test Configuration AC Testing Load Circuit



NOTE:
C_L Includes Jig Capacitance

Figure 13. High Speed Test Configuration AC Testing Load Circuit

10.5 AC Characteristics—Read-Only Operations[1]

Version[2]a		V_{CC} ±10%		–120		–150		
Symbol		**Parameter**	**Notes**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{AVAV}	t_{RC}	Read Cycle Time		120		150		ns
t_{AVQV}	t_{ACC}	Address to Output Delay			120		150	ns
t_{ELQV}	t_{CE}	CE# to Output Delay	2		120		150	ns
t_{PHQV}	t_{PWH}	RP# High to Output Delay			600		600	ns
t_{GLQV}	t_{OE}	OE# to Output Delay	2		50		55	ns
t_{ELQX}	t_{LZ}	CE# to Output Low Z	3	0		0		ns
t_{EHQZ}	t_{HZ}	CE# High to Output High Z	3		55		55	ns
t_{GLQX}	t_{OLZ}	OE# to Output Low Z	3	0		0		ns
t_{GHQZ}	t_{DF}	OE# High to Output High Z	3		30		30	ns
	t_{OH}	Output Hold from Addresses, CE# or OE# Change, Whichever is First	3	0		0		ns

NOTES:

1. See Figure 11, *AC Input/Output Reference Waveform*.
2. OE# may be delayed up to t_{CE}–t_{OE} after the falling edge of CE# without impact on t_{CE}.
3. Sampled, not 100% tested.

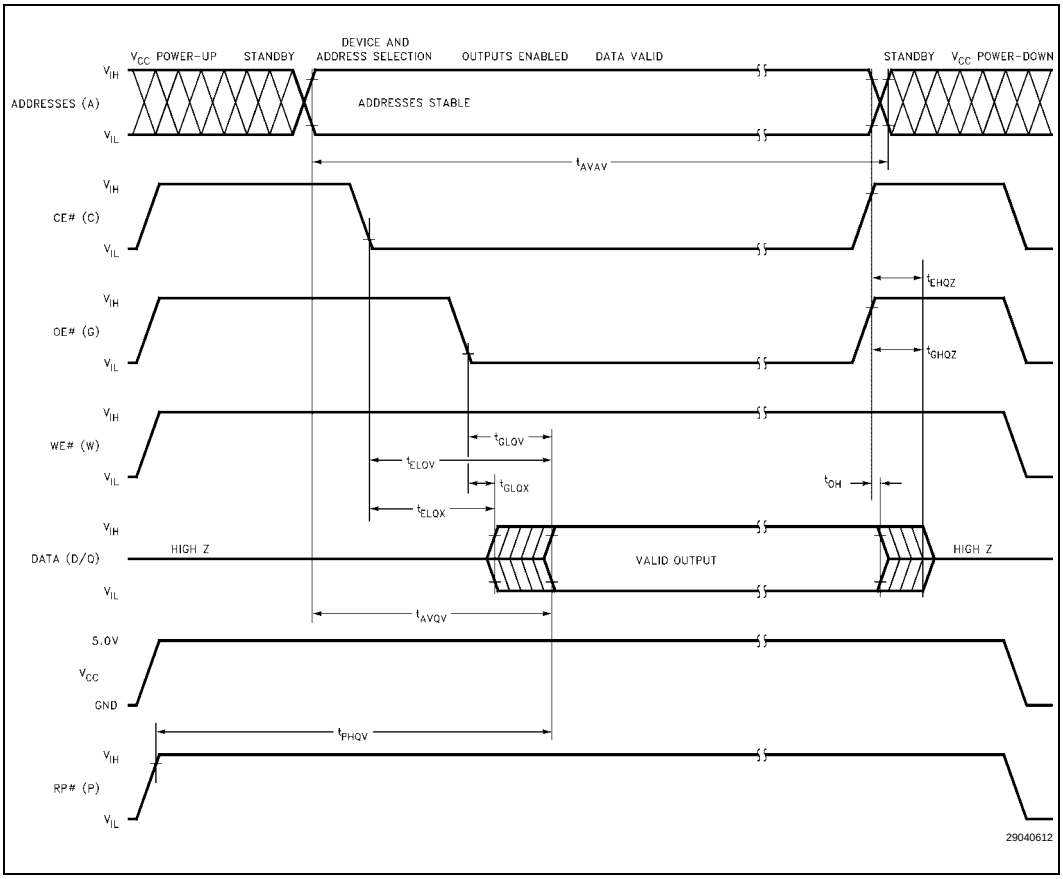


Figure 14. AC Waveform for Read Operations

10.6 AC Characteristics—Write/Erase/Program Operations[1, 9]

Versions		V_{CC} ±10%[10]		–120		–150		
Symbol		Parameter	Notes	Min	Max	Min	Max	Unit
t_{AVAV}	t_{WC}	Write Cycle Time		120		150		ns
t_{PHWL}	t_{PS}	RP# High Recovery to WE# Going Low	2	480		480		ns
t_{ELWL}	t_{CS}	CE# Setup to WE# Going Low		10		10		ns
t_{WLWH}	t_{WP}	WE# Pulse Width		50		50		ns
t_{PHHWH}	t_{PHS}	RP# V_{HH} Setup to WE# Going High	2	100		100		ns
t_{VPWH}	t_{VPS}	V_{PP} Setup to WE# Going High	2	100		100		ns
t_{AVWH}	t_{AS}	Address Setup to WE# Going High	3	50		50		ns
t_{DVWH}	t_{DS}	Data Setup to WE# Going High	4	50		50<		ns
t_{WHDX}	t_{DH}	Data Hold from WE# High		10		10		ns
t_{WHAX}	t_{AH}	Address Hold from WE# High		10		10		ns
t_{WHEH}	t_{CH}	CE# Hold from WE# High		10		10		ns
t_{WHWL}	t_{WPH}	WE# Pulse Width High		50		50		ns
t_{WHQV1}		Duration of Programming Operation	5, 6, 7	15		15		µs
t_{WHQV2}		Duration of Erase Operation (Boot)	5, 6, 7	1.3		1.3		sec
t_{WHQV3}		Duration of Erase Operation (Parameter)	5, 6, 7	1.3		1.3		sec
t_{WHQV4}		Duration of Erase Operation (Main)	5, 6, 7	3.0		3.0		sec
t_{WHGL}		Write Recovery before Read		0		0		µs
t_{QVVL}	t_{VPH}	V_{PP} Hold from Valid SRD	2, 6	0		0		ns
t_{QVPH}	t_{PHH}	RP# V_{HH} Hold from Valid SRD	2, 7	0		0		ns
t_{PHBR}		Boot-Block Relock Delay	2		100		100	ns

NOTES:

1. Read timing characteristics during erase and program operations are the same as during read-only operations. Refer to Section 10.5, *AC Characteristics—Read-Only Operations*.
2. Sampled, not 100% tested.
3. Refer to Table 3 for valid A_{IN} for byte programming or block erasure.
4. Refer to Table 3 for valid D_{IN} for byte programming or block erasure.
5. The on-chip WSM incorporates all program and erase system functions and overhead of standard Intel Flash memory, including byte program and verify (programming) and block precondition, precondition verify, erase and erase verify (erasing).
6. Program and erase durations are measured to completion (SR.7 = 1). V_{PP} should be held at V_{PPH} until determination of program/erase success (SR.3/4/5 = 0).
7. For boot block programming and erasure, RP# should be held at V_{HH} until determination of program/erase success (SR.3/4/5 = 0).
8. Alternate boot block access method.
9. See *Standard Test Configuration*.

10.6.1 PROM PROGRAMMER SPECIFICATIONS

Versions		V_{CC} ±10%		–120		–150		
Symbol		**Parameter**	**Notes**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{GHHWL}		OE# V_{HH} Setup to WE# Going Low	1, 2	480		480		ns
t_{WHGH}	t_{PHH}	OE# V_{HH} Hold from WE# High	1, 2	480		480		ns

NOTES:

1. Sampled, not 100% tested.
2. Alternate boot block access method.

10.7 Erase and Programming Performance

Parameter	Notes	–120			–150			Unit
		Min	Typ(1)	Max	Min	Typ(1)	Max	
Boot Block Erase Time	2		2.10	14.9		2.10	14.9	Sec
Boot Block Program Time	2		0.15	0.52		0.15	0.52	Sec
Parameter Block Erase Time	2		2.10	14.6		2.10	14.6	Sec
Parameter Block Program Time	2		0.07	0.26		0.07	0.26	Sec
Main Block Erase Time	2		3.80	20.9		3.80<	20.9	Sec
Main Block Program Time	2		2.10	7.34		2.10	7.34	Sec
Chip Erase Time	2		10.10	65		10.10	65	Sec
Chip Program Time	2		2.39	8.38		2.39	8.38	Sec

NOTES:

1. 25 °C, 12.0 V_{PP}.
2. Excludes System-Level Overhead.

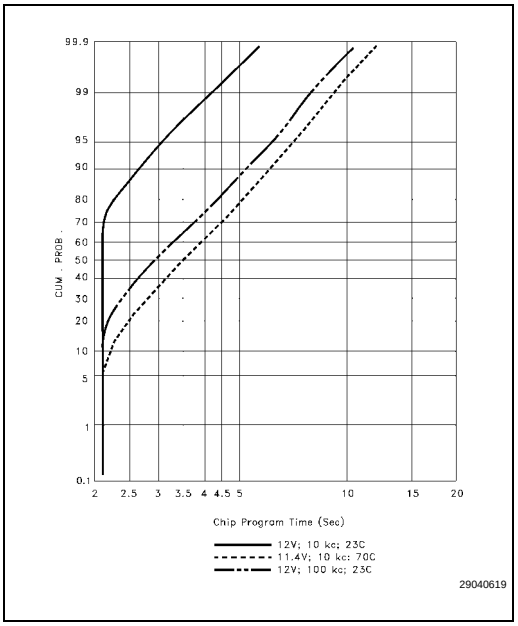


Figure 15. 28F001BX Typical Programming Capability

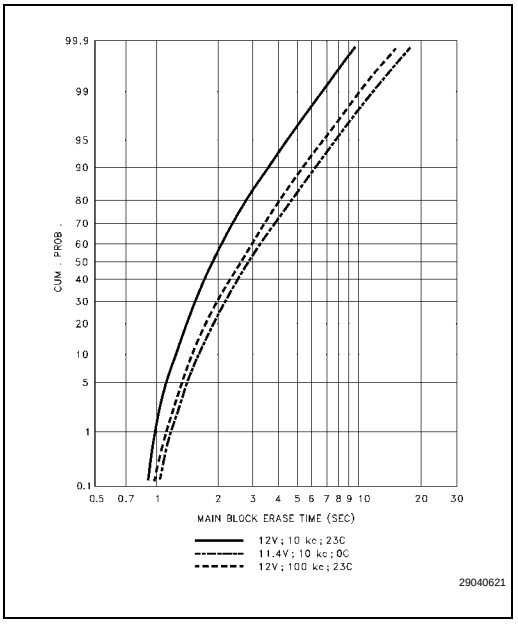


Figure 17. 28F001BX Typical Erase Capability

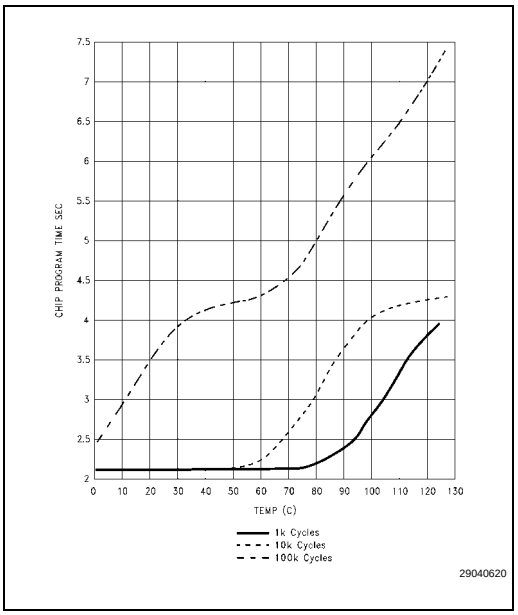


Figure 16. 28F001BX Typical Programming Time at 12 V

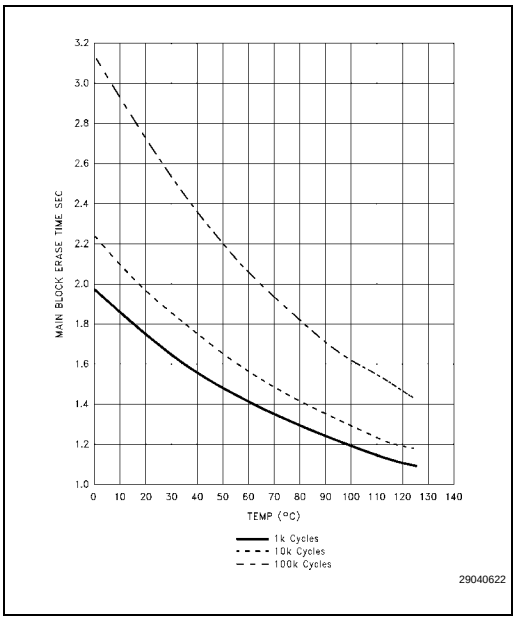


Figure 18. 28F001BX Typical Erase Time at 12 V

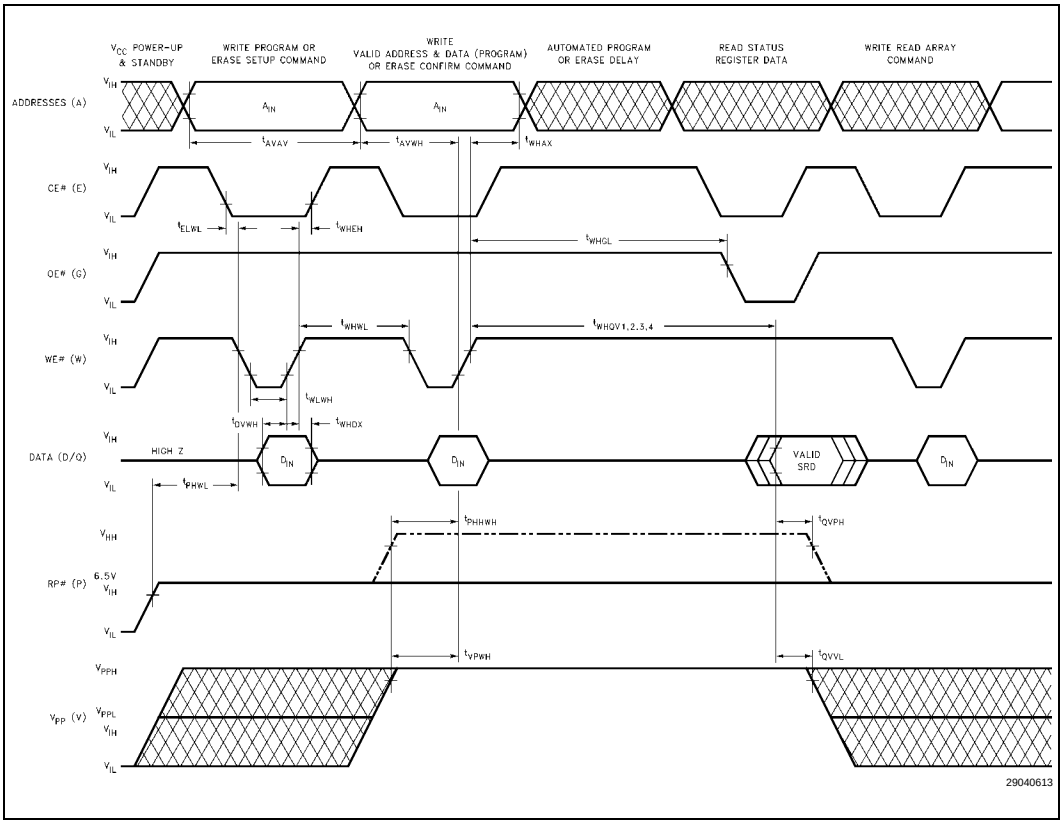


Figure 19. AC Waveform for Write Operations

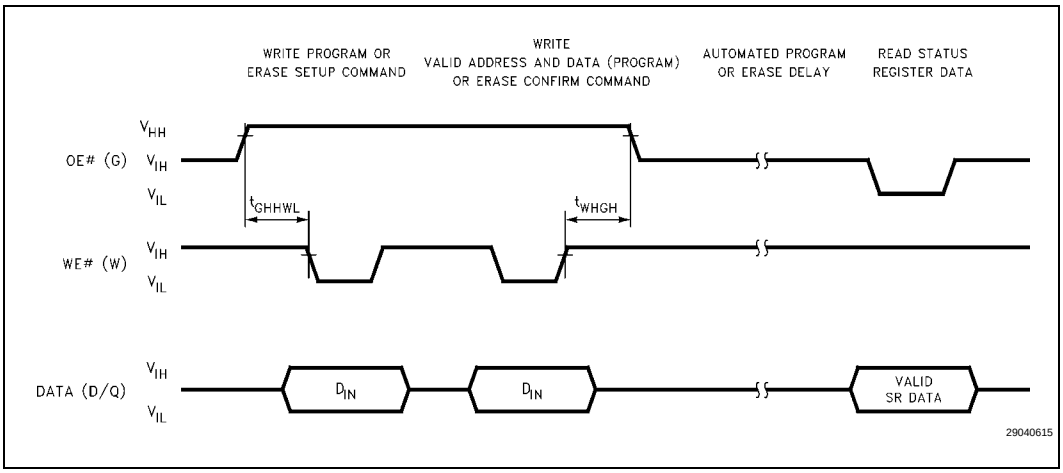


Figure 20. Alternate Boot Block Access Method Using OE#

10.8 AC Characteristics—CE#-Controlled Write Operations(1)

Versions		V_{CC} ±10%	–120			–150		
Symbol		Parameter	Notes	Min	Max	Min	Max	Unit
t_{AVAV}	t_{WC}	Write Cycle Time		120		150		ns
t_{PHEL}	t_{PS}	RP# High Recovery to CE# Going Low	2	480		480		ns
t_{WLEL}	t_{WS}	WE# Setup to CE# Going Low		0		0		ns
t_{ELEH}	t_{CP}	CE# Pulse Width		70		70		ns
t_{PHHEH}	t_{PHS}	RP# V_{HH} Setup to CE# Going High	2	100		100		ns
t_{VPEH}	t_{VPS}	V_{PP} Setup to CE# Going High	2	100		100		ns
t_{AVEH}	t_{AS}	Address Setup to CE# Going High	3	50		50		ns
t_{DVEH}	t_{DS}	Data Setup to CE# Going High	4	50		50		ns
t_{EHDX}	t_{DH}	Data Hold from CE# High		10		10		ns
t_{EHAX}	t_{AH}	Address Hold from CE# High		15		15		ns
t_{EHWH}	t_{WH}	WE# Hold from CE# High		0		0		ns
t_{EHEL}	t_{EPH}	CE# Pulse Width High		25		25		ns
t_{EHQV1}		Duration of Programming Operation	5, 6	15		15		µs
t_{EHQV2}		Duration of Erase Operation (Boot)	5, 6	1.3		1.3		sec
t_{EHQV3}		Duration of Erase Operation (Parameter)	5, 6	1.3		1.3		sec
t_{EHQV4}		Duration of Erase Operation (Main)	5, 6	3.0		3.0		sec
t_{EHGL}		Write Recovery before Read		0		0		µs
t_{QVVL}	t_{VPH}	V_{PP} Hold from Valid SRD	2, 5	0		0		ns
t_{QVPH}	t_{PHH}	RP# V_{HH} Hold from Valid SRD	2, 6	0		0		ns
t_{PHBR}		Boot-Block Relock Delay	2		100		100	ns

NOTES:

1. Chip-enable controlled writes: write operations are driven by the valid combination of CE# and WE#. In systems where CE# defines the write pulse width (within a longer WE# timing waveform), all set-up, hold and inactive WE# times should be measured relative to the CE# waveform.
2. Sampled, not 100% tested.
3. Refer to Table 3 for valid A_{IN} for byte programming or block erasure.
4. Refer to Table 3 for valid D_{IN} for byte programming or block erasure.
5. Program and erase durations are measured to completion (SR.7 = 1). V_{PP} should be held at V_{PPH} until determination of program/erase success (SR.3/4/5 = 0).
6. For boot block programming and erasure, RP# should be held at V_{HH} until determination of program/erase success (SR.3/4/5 = 0).
7. Alternate boot block access method.

10.8.1 PROM PROGRAMMER SPECIFICATIONS

Versions		V_{CC} ±10%	–120		–150		
Symbol	**Parameter**	**Notes**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{GHHEL}	OE# V_{HH} Setup to CE# Going Low	1, 2	480		480		ns
t_{EHGH}	OE# V_{HH} Hold from CE# High	1, 2	480		480		ns

NOTES:

1. Sampled, not 100% tested.
2. Alternate boot block access method.

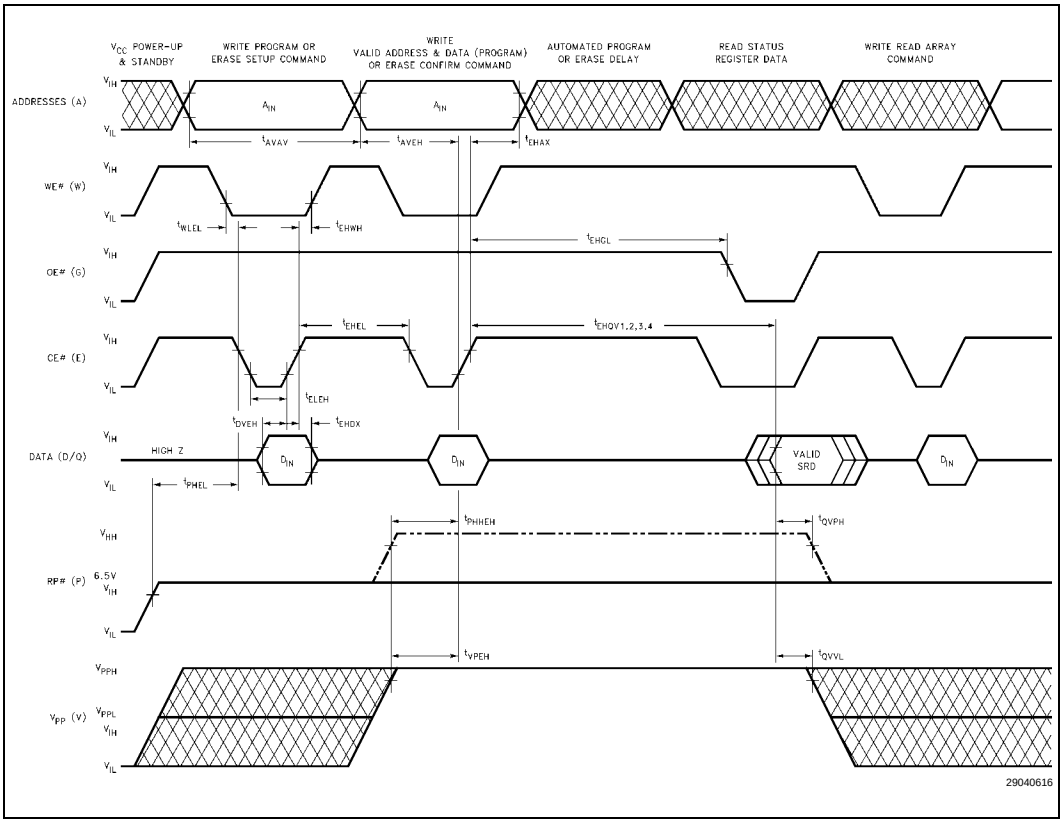
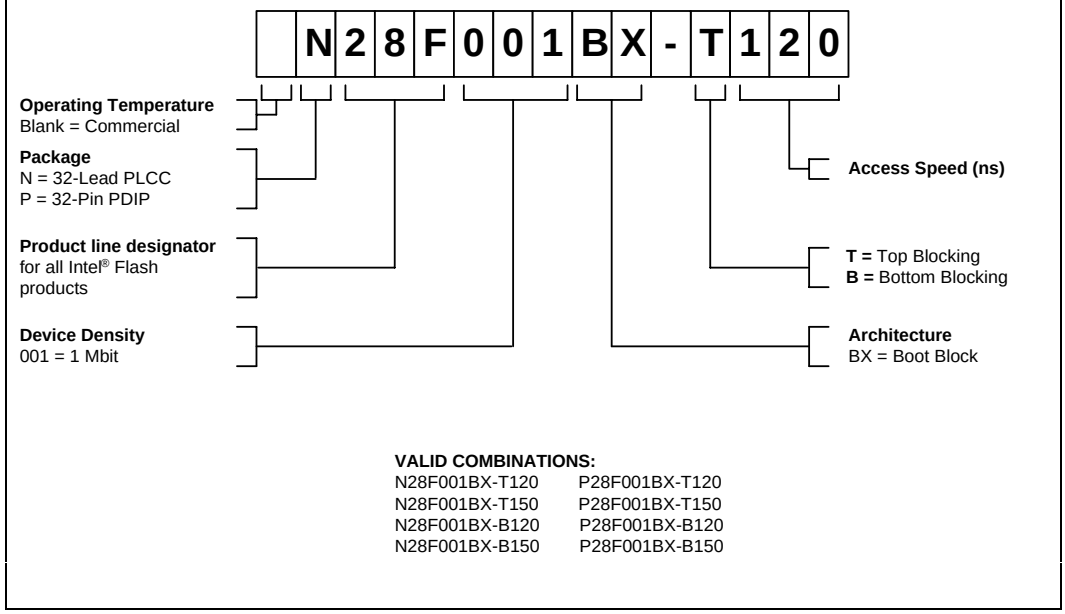


Figure 21. Alternate AC Waveform for Write Operations

11.0 ORDERING INFORMATION



12.0 ADDITIONAL INFORMATION(1,2)

Order Number	Document
Note 3	*AP-316 Using Flash Memory for In-System Reprogrammable Nonvolatile Storage*
Note 3	*AP-608 Implementing a Plug and Play BIOS Using Intel's Boot Block Flash Memory*
Note 3	*AP-623 Multi-Site Layout Planning Using Intel's Boot Block Flash Memory*

NOTE:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com for technical documentation and tools.
3. These documents can be located at the Intel World Wide Web support site, http://www.intel.com/support/flash/memory