W86L387D

Winbond Host Interface
Memory Stick™ Bridge

Table of Contents-

1. GENERAL DESCRIPTION

The W86L387D is a Memory Stick™ host interface bridge used between host microprocessor and Memory Stick™. The data width of host microprocessor can be 8-bit or 16-bit. W86L387D can support synchronous or asynchronous type of host interface. It also supports DMA or Interrupt type of transfer mode to improve data transfer performance between host microprocessor and Memory Stick™. W86L387D is fit for most of IA devices, such as PDA, Cellular Phone, DSC, and MP3 player.

2. FEATURES

- Compliant with Sony Memory Stick™ spec. Version 1.3
- Support two types of host microprocessor interface access--synchronous and asynchronous mode
- DMA and Interrupt transfer mode supported
- Host microprocessor data bus can be 8-bit or 16-bit
- Built-in crystal driver circuit, support external oscillator or crystal clock input
- Extra 8 programmable GPIO supported
- Wide range of clock input up to 20Mhz
- 3.3V opereation
- 48-pin LQFP package

Ordering Information

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W86L387D	48-PIN LQFP	Commercial, 0°C to +70°C

3. PIN CONFIGURATION

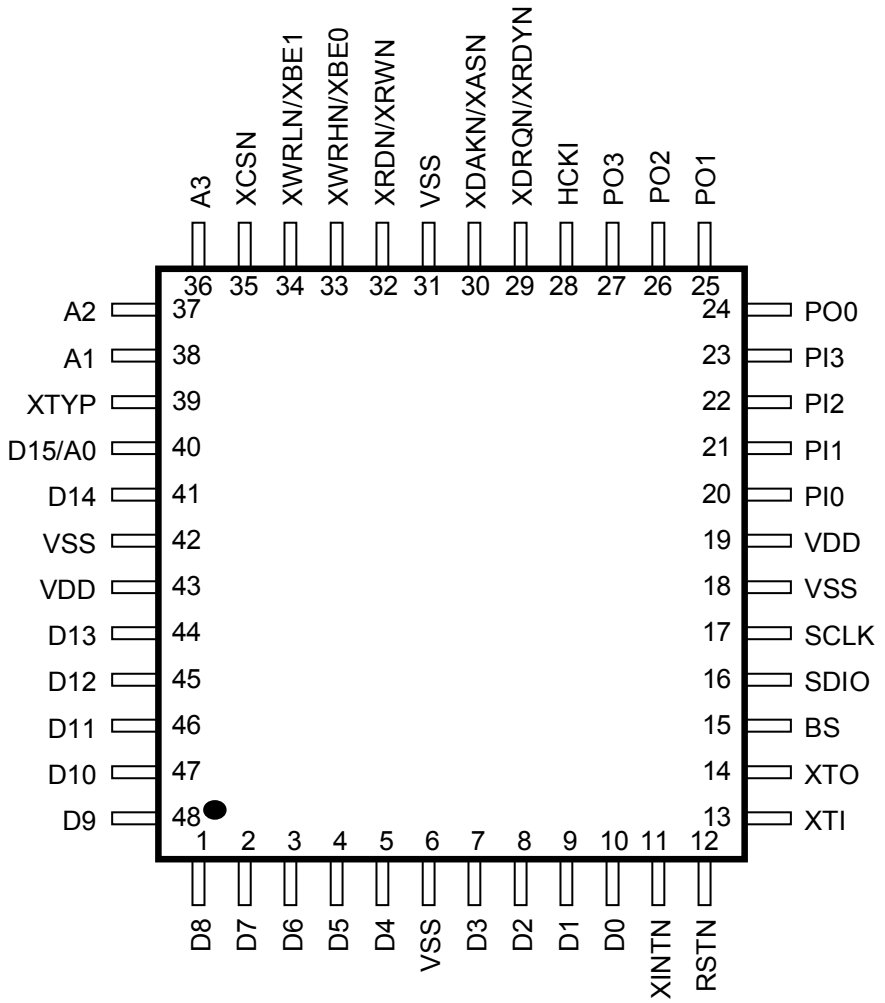


Fig.3-1 W86L387D Pin Assignment.

4. PIN DESCRIPTIONS

PIN	NAME	TYPE	DESCRIPTION
MS Interface:			
15	BS	DO	Serial protocol bus state signal for Memory stick.
16	SDIO	DO/DI	Serial protocol data signal for Memory stick.
17	SCLK	DO	Clock output signal for Memory stick.
Crystal Driver:			
13	XTI	DI	From 3.58MHz to 20MHz Clock driver input signal, can be used as external clock input.
14	XTO	DO	Clock driver output signal.
Host Interface:			
28	HCKI	DI	Host clock input. Only used in Type2.
35	XCSN	DI	Chip select input pin, active low.
36:38	A[3:1]	DI	Address input pins.
40	D15/A0	DI/DO	Data bus D15 pin, D[15:8] is the high byte of the data bus, D15 also used as A0 when 8-bit Host data size. In 8-bit mode, internal register high byte (D15:8) will accessed at data bus [7:0] when A0 = 1, low byte (D7:0) will accessed at data bus [7:0] when A0 = 0.
41	D14	DI/DO	Data bus D14 pin.
44:48	D[13:9]	DI/DO	Data bus [13:9] pins.
1:5	D[8:4]	DI/DO	Data bus [8:4] pins, D[7:0] is the low byte of the data bus.
7:10	D[3:0]	DI/DO	Data bus [3:0] pins.
33	XWRHN/ XBE0	DI	Type 1: High byte (D15 to D8) write control pin, active low. Type 2: High byte (D15 to D8) data valid pin, active low.
34	XWRLN/ XBE1	DI	Type 1: Low byte (D7 to D0) write control pin, active low. Type 2: Low byte (D7 to D0) data valid pin, active low.

Pin Descriptions, continued

PIN	NAME	TYPE	DESCRIPTION
32	XRDN/ XRWN	DI	Type 1: Read control pin, active low. Type 2: Read write control pin, 1: read 0: write
11	XINTN	DO	Interrupt request pin, active low.
30	XDAKN/ XASN	4.1.1.1. DI	Type 1: DMA transfer acknowledge pin, active low. Type 2: Bus access cycle start pin, active low.
29	XDRQN/ XRDYN	DO	Type 1: DMA transfer request pin, active low. Type 2: Bus cycle complete pin, active low.
39	XTYP	DI	Host interface type 2 select pin, 0 : type 1 mode. 1 : type 2 mode.
GP I/O Port:			
23:20	PI[3:0]	DI	4-bit parallel port input signal.
27:24	PO[3:0]	DO	4-bit parallel port output signal.
Other:			
12	RSTN	DI	Reset input, hardware reset input, active low.
Power:			
19,43	VDD x2	DP	Power supply 3.3V (2 pins).
6,18, 31,42	VSS x4	DP	Ground (4 pins).

Type: DP is Power, DI is Digital Input, DO is Digital Output.

5. BLOCK DIAGRAM

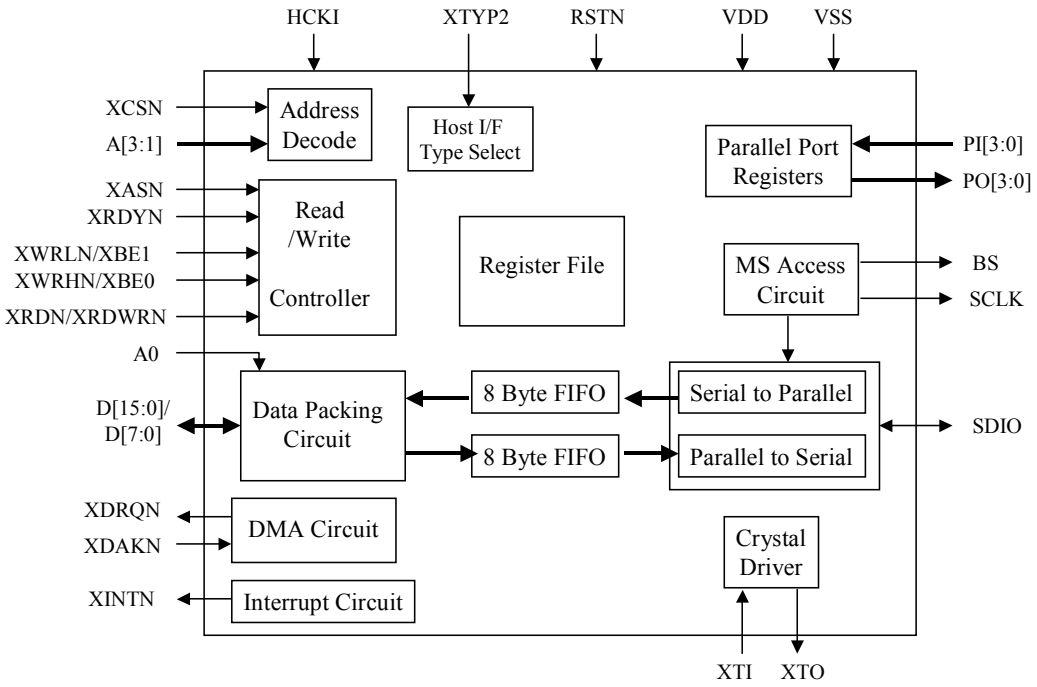


Fig. 5-1 Block Diagram of W86L387D

6. REGISTERS

6.1 Register Map

The register in the W86L387D is consisted of command, status, control, received/transmit data buffer, interrupt, DMA and parallel port registers and READY register in Host interface type 2, these registers are listed as follows:

ADDR	REGISTER NAME	CONTENT (NOTE 2)															
A[3:1]	(NOTE 1)	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
000	Command Reg. (R/W)	PID code				Data size											
		0	0	0	0	-	-	0	0	0	0	0	0	0	0	0	0
001	Status Reg. (RO)	Status								-	-	-	-	-	-	-	-
		0	0	-	-	1	0	1	0								
001	Control Reg. (R/W)	-	-	-	-	-	-	-	-	Control							
										0	0	0	0	0	1	0	1
010	Receive Data Buffer (R/O)	Receive data buffer															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010	Transmit Data Buffer (WO)	Transmit data buffer															
		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
011	Interrupt Status Reg. (RO)	Interrupt status								-	-	-	-	-	-	-	-
		1	0	0	0	-	-	0	0								
011	Interrupt Control Reg. (R/W)	-	-	-	-	-	-	-	-	Interrupt control							
										0	0	0	-	-	-	-	-
100	Parallel Port Data Reg. ([15:12]RO, [11:8]R/W)	PI[3:0]				PO[3:0]				-	-	-	-	-	-	-	-
		X	X	X	X	X	X	X	X								
100	Parallel Port Control Reg. (R/W)	-	-	-	-	-	-	-	-	PIEN[3:0]				POEN[3:0]			
										0	0	0	0	0	0	0	0
101	Ready Control Reg. (R/W)	F	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		0															
111	Data Size Reg. (R/W)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	8-bit
										0	0	0	0	0	0	0	0

Note 1: R/W means the register can be read and write.

RO means the register is read only.

WO means the register is write only.

Note 2: The data bit in the content is the initial value during hardware reset.

0: the bit value is 0.

1: the bit value is 1.

X: the bit value is unknown.

-: Undefined bit in the register and the value will read 0.

6.2 Register Description

Command Register A[3:1] = 000, Read/Write:

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PID code				Data size											
0	0	0	0	-	-	0	0	0	0	0	0	0	0	0	0

PID code is the packet ID also is the transfer protocol command (TPC) code of the MS bus when the transfer protocol is started. This command must write when RDY bit in interrupt status register is high and serial interface is enabled (SIEN bit in the control register is high).

The data size of the MS transfer protocol depends on the TPC code and may be up to 512 bytes, the 16-bit CRC code is generated automatically and not included in the data size. The direction of data transfer is also determined from extraction of the TPC code.

The command will not started until the high low byte of the register has been written.

Status Register A[3:1] = 001, Read only:

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INT	DRQ	-	-	RBE	RBF	TBE	TBF								
0	0	-	-	1	0	1	0	-	-	-	-	-	-	-	-

INT (Interrupt): This bit = 1 when the interrupt pin (XINTN) becomes active (low).

DRQ (DMA request): This bit = 1 when DMA request input (DRQN) becomes active (low).

RBE (Receive buffer empty): This bit = 1 when receive buffer is empty, the receive buffer will set to empty during reset.

RBF (Receive buffer full): This bit = 1 when receive buffer is full.

TBE (Transmit buffer empty): This bit = 1 when transmit buffer is empty, the transmit buffer will set to empty during reset.

TBF (Transmit buffer full): This bit = 1 when transmit buffer is full.

Control Register A[3:1] = 001, Read/Write:

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
								RST	PWD	SIEN	DAKEN	NO_CRC	BSY_CNT		
								0	0	0	0	0	1	0	1

RST (Reset): This bit = 1 is software reset and is used to reset the internal logic and receive and transmit data buffer, the content of other registers are not affected.

PWD (Power down): This bit = 1 is used to power down the internal logic and crystal driver. Set this bit to low will enabled the W86L387D when the W86L387D is in power down state. But the W86L387D will never enabled if Host interface type 2 is configured and the Host I/F clock (HCKI) input is disabled.

SIEN (Serial interface enable): The MS bus interface is enabled when this bit is high.

DAKEN (DMA acknowledge enable): This bit is used to set the DMA request and acknowledge mode. When this bit is low, the XDRQN will active once by accessing receive/transmit data buffer register and not influenced by any state of XDAKN signal. When this bit is high, the XDRQN will kept in low (active) state continuously and the XDAKN is used to count the data access cycle. The XDRQN will return to high when the last data access cycle has completely. The DAKEN must set at low if the Host interface type 2 is configured.

NO_CRC (No CRC): The CRC code in the MS interface will not generated and checked when this bit is set high. This mode should not use in normal operation condition.

BSY_CNT (Busy count): These bits set the time out value when the MS interface is accessing. The time out value is 4 times this value of CLK period, the initial value is 20 cycles of CLK (default value is 5). The time out error will not detected when the value set to 0.

Receive Data Buffer Register A[3:1] = 010, Read only:

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive data buffer															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Receive Data Buffer Register A[3:0] = 0100, Read only, 8-bit data size:

								BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
								Receive data buffer							
								0	0	0	0	0	0	0	0

When the extraction of the TPC code is READ_PAGE_DATA or READ_REG or GET_INT, the data received from the SDIO pin and is recorded in receive data buffer, the RBE and RBF bits in the status register will reflect the buffer status and XDRQN will active. The received data can be read out by reading this register repeatedly until receive buffer is empty. Only high byte data (bit[15:8]) is valid if the last data is one byte only.

The data is located at bit[7:0] and address bit 0 must set 0 when read the receive data buffer register with 8-bit data size of Host CPU.

Transmit Data Buffer Register A[3:1] = 010, Write only:

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit data buffer															
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Transmit Data Buffer Register A[3:0] = 0100, Write only, 8-bit data size:

								BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
								Transmit data buffer							
								X	X	X	X	X	X	X	X

When the extraction of the TPC code is WRITE_PAGE_DATA or WRITE_REG or SET_R/W_REG_ADDRESS or SET_CMD. The data stored in the transmit data buffer will transmitted to the SDIO pin, the TBE and TBF bits in the status register will reflect the transmit buffer status and XDRQN will active when the buffer is not full and the data size is not enough. The transmit data must be written to this register repeatedly until the data size specified in the command register is enough. Only high byte data (bit[15:8]) is valid if the last data is one byte only.

The data is located at bit[7:0] and address bit 0 must set 0 when write the transmit data buffer register with 8-bit data size of Host CPU.

Interrupt Status Register A[3:1] = 011, Read only:

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RDY	SIF	DREQ	PIN	-	-	CRC	TOE	-	-	-	-	-	-	-	-
0	0	0	0	-	-	0	0								

RDY (Ready): This bit = 1 when the MS transfer protocol ended and the serial interface is in ready state, this bit always reflect the serial interface status and never cleared when read the interrupt status register.

SIF (Serial interface interrupt IN): This bit = 1 when serial interface received interrupt IN from the MS card.

DREQ (DMA request interrupt IN): This bit = 1 when the data transfer is requested.

PIN (Parallel Input interrupt IN): This bit = 1 when the parallel input port change state.

CRC (CRC error interrupt): This bit = 1 when the received data with CRC error checked. This bit will be disabled when NO_CRC bit is set in the control register.

TOE (Time out error interrupt): This bit is used to notify an abnormal operation of card accessing when the count value of the BSY transmitted from the card is more than the time out value setted by the BSY_CNT in the control register. The BS signal will remain at low when TOE activated and RDY become high.

The XINTN goes low when any bit of interrupt status register becomes high, the XINTN signal will return to high and the interrupt status register will cleared when read the interrupt status register but the RDY bit will not cleared.

Interrupt Control Register A[3:1] = 011, Read/Write:

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
-	-	-	-	-	-	-	-	INT	DREQ	PIN	-	-	-	-	-
								0	0	0	-	-	-	-	-

INT (Interrupt enable): XINTN output pin is enabled when this bit is high.

DREQ (DMA request interrupt enable): The XINTN will active (low) when this bit = 1 and DMA request is active.

PIN (Parallel input interrupt enable): This bit = 1 to enable the parallel input interrupt.

Parallel Port Data Register A[3:1] = 100, Bit[15:12]Read only, Bit[11:8] Read/Write:

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PIN3	PIN2	PIN1	PIN0	PO3	PO2	PO1	PO0	-	-	-	-	-	-	-	-
X	X	X	X	X	X	X	X								

PIN[3:0]: is the read data from parallel input port [3:0] pins, the parallel input are sampled every 16 cycles of the system clock. The read bit is high when the input pin is low.

PO[3:0]: is the data output to the PO[3:0] pins, write 1 in the register will output high on the related PO pin.

Parallel Port Control Register A[3:1] = 100, Read/Write:

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
-	-	-	-	-	-	-	-	PIEN3	PIEN2	PIEN1	PIEN0	POEN3	POEN2	POEN1	POEN0
								0	0	0	0	0	0	0	0

PIEN[3:0] (Parallel input enable): The bit = 1 is used to enable the related parallel input pin of PI[3:0].

POEN[3:0] (Parallel output enable): The bit = 1 is used to enable the related parallel output pin of PO[3:0].

READY Control Register A[3:1] = 101, Read/Write:

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Fast	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0	-	-	-	-	-	-	-								

This register is effective only when Host interface access type 2 is selected. The access cycle is 2-cycle when Fast bit is set high, otherwise the access cycle is 3-cycle.

Data Size Register A[3:1] = 111, Read/Write:

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	8-bit
								0	0	0	0	0	0	0	0

This data size register is used to set the Host data size, default is 16-bit data size, write 1 to bit 0 will set the data size to 8-bit, bit [7:1] must write 0.

7. FUNCTIONAL DESCRIPTION

7.1 Host Interface

The Host interface type may be type 1 or type 2 and the data size of the data bus may be 16-bit or 8-bit.

Host Interface Type 1:

The Host interface type 1 is selected when XTYP pin is low. The data size of the CPU data bus may be 16-bit or 8-bit. Figure 7-1 shows the timing of 16-bit CPU read and write in type 1, figure 7-2 and 7-3 show the timing of CPU 8-bit data bus read and write in type 1.

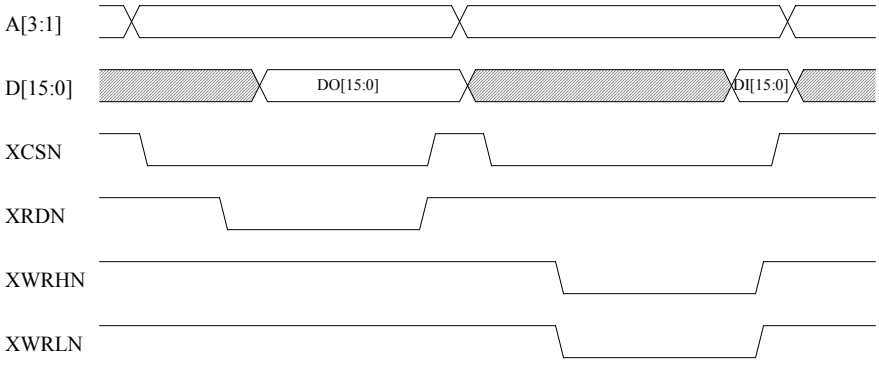


Fig. 7-1 16-bit Read and Write Access in Host I/F Type 1.

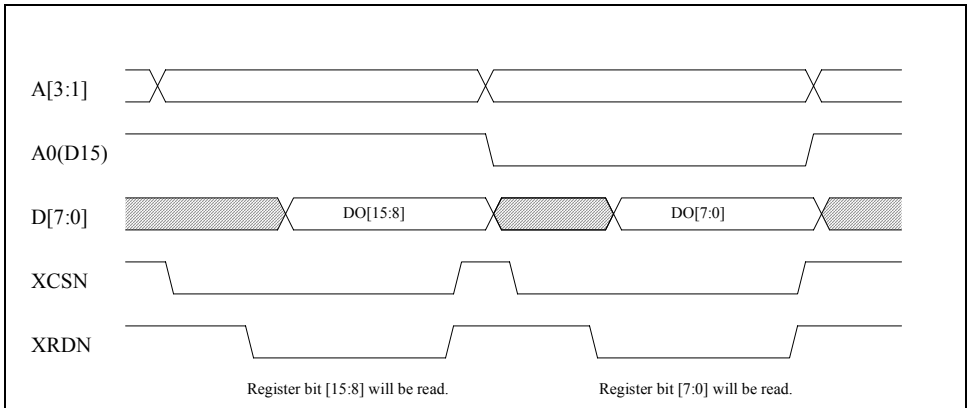


Fig. 7-2 CPU 8-bit Data Bus Read Access in Host I/F Type 1.

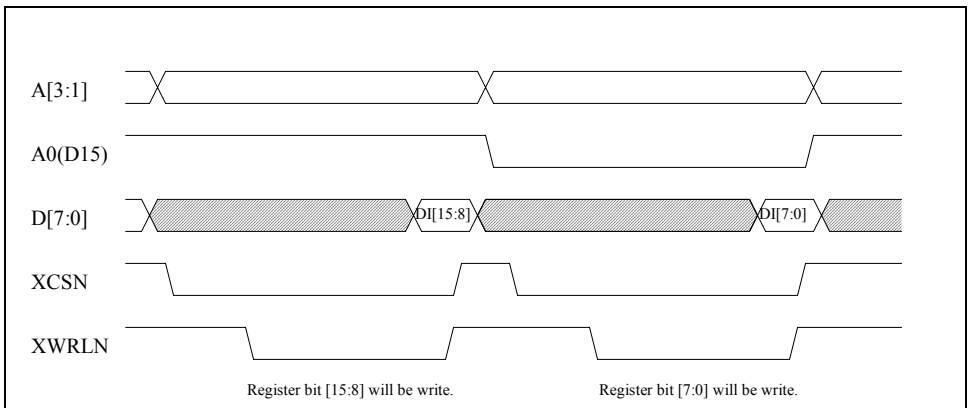


Fig. 7-3 CPU 8-bit Data Bus Write Access in Host I/F Type 1.

The data is located at bit [7:0] when the data size of Host CPU is 8-bit, the address bit 0 (A0) = 1 is to access the register data bit [15:8], A0 = 0 to access data bit [7:0].

Host Interface Type 2:

The Host interface type 2 is selected when XTYP pin is high. The data size of the CPU data bus may be 16-bit or 8-bit and the access cycle may be in 3-cycle or 3-cycle. Figure 7-4 shows the timing of 16-bit CPU read write in type 2 and the access cycle is 3-cycle access, figure 7-5 shows the timing of 16-bit CPU read write in type 2 and the access cycle is 2-cycle access.

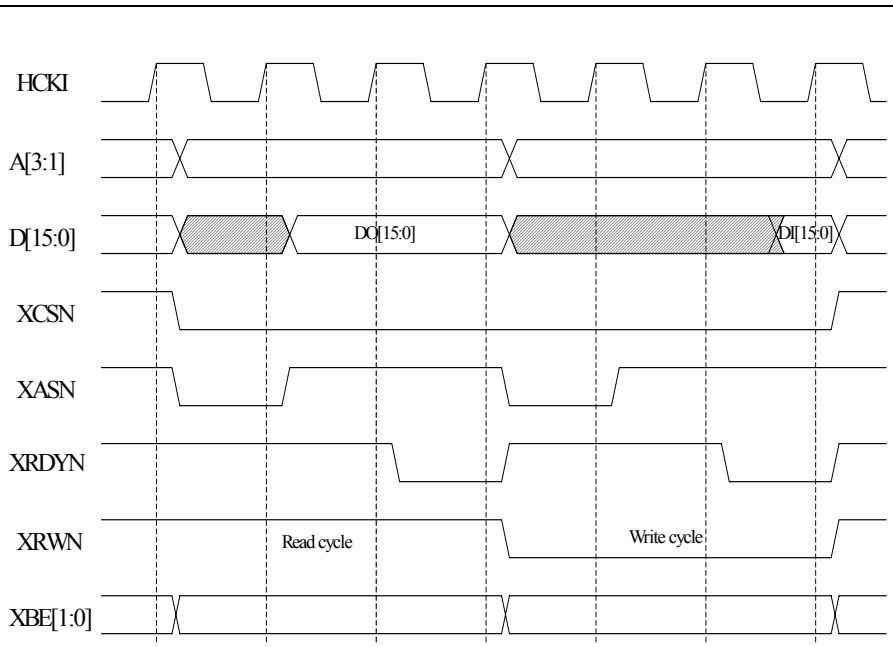


Fig. 7-4 16-bit Read and Write Access in Host I/F Type 2, 3-Cycle Access.

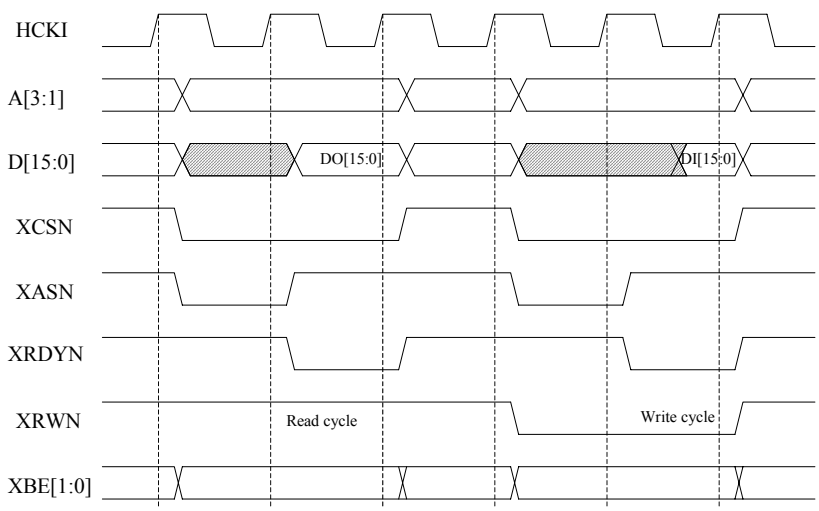


Fig. 7-5 16-bit Read and Write Access in Host I/F Type 2, 2-Cycle Access.

7.2 DMA Access

DMA request XDRQN is used to notify the Host that the Host should write data to the transmit data buffer or read data from the receive data buffer in data write to the card or data read from the card.

During data transmit to the card, the XDRQN will active if the data write command has been transfer to the card and the transmit data buffer have not enough data to transmit to the card. The XDRQN will not active if the transmit data buffer have enough data to transmit to the card.

During data receive from the card, the XDRQN will active if the data read command has been transfer to the card and the data have been received in the receive data buffer. The XDRQN will not active if the data read command has been executed completely and the receive data buffer is read out.

There are two types of DMA acknowledge waveform, the first type is configured if DAKEN = low, XDAKN is ignore and XDRQN will inactive after each access receive or transmit data buffer, the XDRQN will re-active after four clock later. Figure 7-6 shows the waveform of DMA access receive data buffer in DAKN = low. The second type is configured if DAKEN = high, XDAKN is used to count the transfer count of the data buffer, XDRQN will hold at active state until the data has been transferred completely. Figure 7-7 is the waveform of DMA access transmit data buffer in DAKN = high.

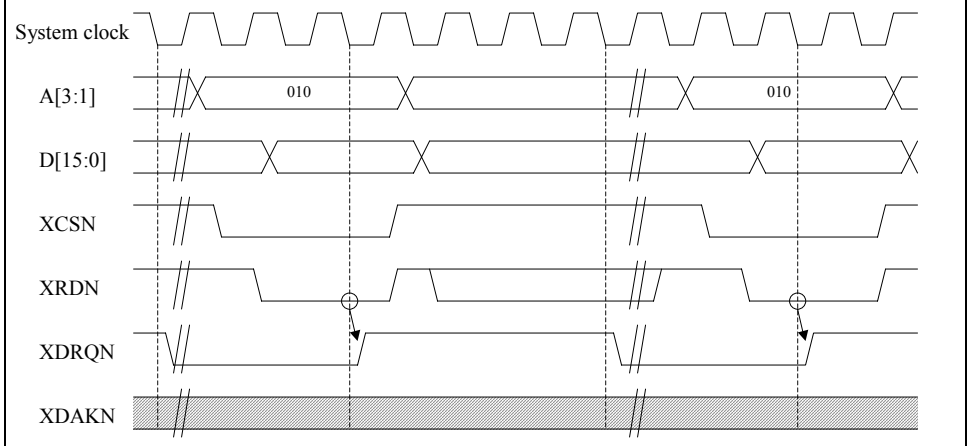


Fig. 7-6 DMA Access Receive Data Buffer (DAKEN = low).

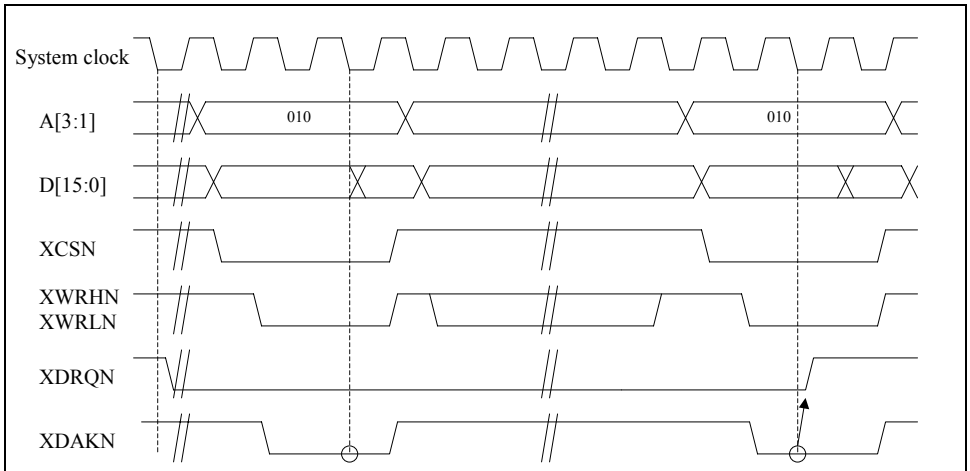


Fig. 7-7 DMA Access Transmit Data Buffer (DAKEN = high).

8. HOST ACCESS PROCEDURE

8.1 System Initialization Procedure:

STEP	HOST ACCEPT AND ACTION COMMAND		W86L387D ACTION		MS CARD ACTION
1.	Set up CPU data size and type access cycle.	>	Execute.		
2.	Read card insert signal of MS.		card insert not sensed by W86L387D.	<	No MS card.
3.	Write PWD = high on the control register if card insert signal = high.	>	Power down.		
4.	Wait until card insert signal = low.			<	Card insert.
5.	Re-check card insert signal is in low.				
6.	Write PWD = low on the control register.	>	Power up.		
7.	Write software reset.	>	Reset internal logic circuit.		
8.	Read status register.	>	Execute.		
9.	Chip error if status <> 0AH.				
10.	Program PIO port if necessary.	>	Execute.		
11.	Program PIO interrupt enable register if necessary.	>	Execute.		
12.	Set up DAKEN and BSY_CNT on the control register.	>	Execute.		
13.	Enable DREQ and INT interrupt.	>	Execute.		
14.	Wait for TPC command.				

8.2 READ_REG (Read MS Register) of TPC Commands:

STEP	HOST ACCEPT AND ACTION COMMAND		W86L387D ACTION		MS CARD ACTION
1.	Read status register.	>	Execute.		
2.	Read interrupt status register if status <> 0AH.	>	Execute.		
3.	Enable SIE bit of control register.	>	Execute.		
4.	Write 401FH in the command register.	>	Activate read 31 bytes of MS register.	>	Accept read MS register command.
5.	Wait for DMA request.				
6.	Read receive data buffer if DMA request.	<	Receive read data from card and output data to the Host.	<	Card output read data.
7.	Wait for DMA request.		Receive read data from card.	<	Card output read data.
	If Host busy.		Stop MS SCLK if receive data buffer is full.		
8.	Go to step 6 if data length not enough.				
9.	Read status register and check receive data buffer.	>	Execute.		
10.	Read interrupt status register if status <> 0AH.	>	Execute.		
11.	Disable SIE bit of control register if needed.	>	Execute.		
12.	Wait for TPC command.				

8.3 WRITE_REG (Write MS Register) of TPC Commands:

STEP	HOST ACCEPT AND ACTION COMMAND		W86L387D ACTION		MS CARD ACTION
1.	Read status register.	>	Execute.		
2.	Read interrupt status register if status <> 0AH.	>	Execute.		
3.	Enable SIE bit of control register.	>	Execute.		
4.	Write 8 bytes of register data to the transmit data buffer.	>	Accept write data and store in transmit data buffer.		
5.	Write B00FH in the command register.	>	Activate write 15 bytes of MS register.	>	Accept write MS register command.
6.	Wait for DMA request.		Output write data to the MS bus.	>	Card accept write data.
7.	Write data to the transmit data buffer if DMA request.	>	Accept write data and output to the MS bus.	>	Card accept write data.
8.	Wait for DMA request.		Output write data to the MS bus.	<	Card accept write data.
	If Host busy.		Stop MS SCLK if transmit data buffer is empty.		
9.	Go to step 7 if data length not enough.				
10.	Read status register and check transmit data buffer.	>	Execute.		
11.	Read interrupt status register if status <> 0AH.	>	Execute.		
12.	Disable SIE bit of control register if needed.	>	Execute.		
13.	Wait for TPC command.				

8.4 SET_CMD (Set Command to the Flash Controller of MS card) of TPC Commands:

STEP	HOST ACCEPT AND ACTION COMMAND		W86L387D ACTION		MS CARD ACTION
1.	Read status register.	>	Execute.		
2.	Read interrupt status register if status <> 0AH.	>	Execute.		
3.	Enable SIE bit of control register.	>	Execute.		
4.	Write 1 byte of command code to the transmit data buffer.	>	Accept command code and store in transmit data buffer.		
5.	Write E001H in the command register.	>	Activate 1 byte of set command to the MS bus.	>	Accept the command.
6.	Wait until interrupt.	<	Reflect SIF interrupt.	<	Card execute completely and activate interrupt.
7.	Read interrupt status register and check is SIF interrupt.	>	Execute.		
8	Read status register and check transmit data buffer.	>	Execute.		
9	Read interrupt status register if status <> 0AH.	>	Execute.		
10.	Disable SIE bit of control register if needed.	>	Execute.		
11.	Wait for TPC command.				

8.5 READ_PAGE_DATA (Read Page Data from the MS Card) of TPC Commands:

STEP	HOST ACCEPT AND ACTION COMMAND		W86L387D ACTION		MS CARD ACTION
1.	Read status register.	>	Execute.		
2.	Read interrupt status register if status <> 0AH.	>	Execute.		
3.	Enable SIE bit of control register.	>	Execute.		
4.	Write 2200H in the command register.	>	Activate read 512 bytes of MS page data.	>	Accept read MS page data command.
5.	Wait for DMA request.				
6.	Read receive data buffer if DMA request.	<	Receive read data from card and output data to the Host.	<	Card output read data.
7.	Wait for DMA request.		Receive read data from card.	<	Card output read data.
	If Host busy.		Stop MS SCLK if receive data buffer is full.		
8.	Go to step 6 if data length not enough.				
9.	Read status register and check receive data buffer.	>	Execute.		
10.	Read interrupt status register if status <> 0AH.	>	Execute.		
11.	Disable SIE bit of control register if needed.	>	Execute.		
12.	Wait for TPC command.				

8.6 WRITE_PAGE_DATA (Write Page Data from the MS Card) of TPC Commands:

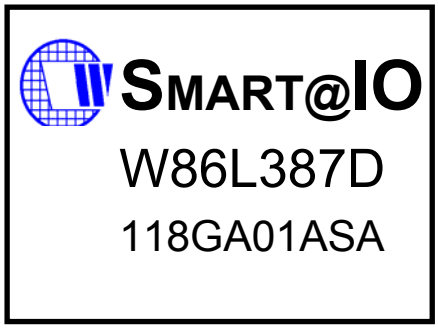
STEP	HOST ACCEPT AND ACTION COMMAND		W86L387D ACTION		MS CARD ACTION
1.	Read status register.	>	Execute.		
2.	Read interrupt status register if status <> 0AH.	>	Execute.		
3.	Enable SIE bit of control register.	>	Execute.		
4.	Write 8 bytes of page data to the transmit data buffer.	>	Accept write data and store in transmit data buffer.		
5.	Write D200H in the command register.	>	Activate write 512 bytes of MS page data.	>	Accept write MS page data command.
6.	Wait for DMA request.		Output write data to the MS bus.	>	Card accept write data.
7.	Write data to the transmit data buffer if DMA request.	>	Accept write data and output to the MS bus.	>	Card accept write data.
8.	Wait for DMA request.		Output write data to the MS bus.	<	Card accept write data.
	If Host busy.		Stop MS SCLK if transmit data buffer is empty.		
9.	Go to step 7 if data length not enough.				
10.	Read status register and check transmit data buffer.	>	Execute.		
11.	Read interrupt status register if status <> 0AH.	>	Execute.		
12.	Disable SIE bit of control register if needed.	>	Execute.		
13.	Wait for TPC command.				

8.7 PIN[3:0] Access Sequential:

STEP	HOST ACCEPT AND ACTION COMMAND		W86L387D ACTION		PIN[3:0] ACTION
1.	Write parallel port control to enable the related PIEN input.	>	Execute.		
2.	Write interrupt register to enable the PIN interrupt.	>	Execute.		
3.	Read parallel port data register, PIN[3:0] = low	<	Reflect logic state PIN[3:0] pins.	<	PIN[3:0] = high.
4.	Wait for interrupt input.				PIN[3:0] = high.
5.	Read interrupt status register and check is PIN interrupt.	<	Reflect the active (low) input pin and generate interrupt.	<	Any one of PIN[3:0] is low.
6.	Read parallel port data register, PIN = high.	<	Execute.		
7.	Read parallel port data register, PIN = low.	<	Reflect the inactive (high) input pin	<	PIN[3:0] = high.
8.	Read interrupt status register, PIN interrupt = high.	>	PIN interrupt will be cleared after this action.		
9.	Read status register, INT bit = low.	>	Execute.		
10.	Wait for TPC command.				

9. HOW TO READ THE TOP MARKING

The top marking of W86L387D



1st line: Winbond logo and SMART@IO Mark

2nd line: Part number of W86L387D

3rd line: Tracking code 118 G A 01A SA

118: packages made in '01, week 18

G: assembly house ID; A means ASE, O means OSE, G means GR

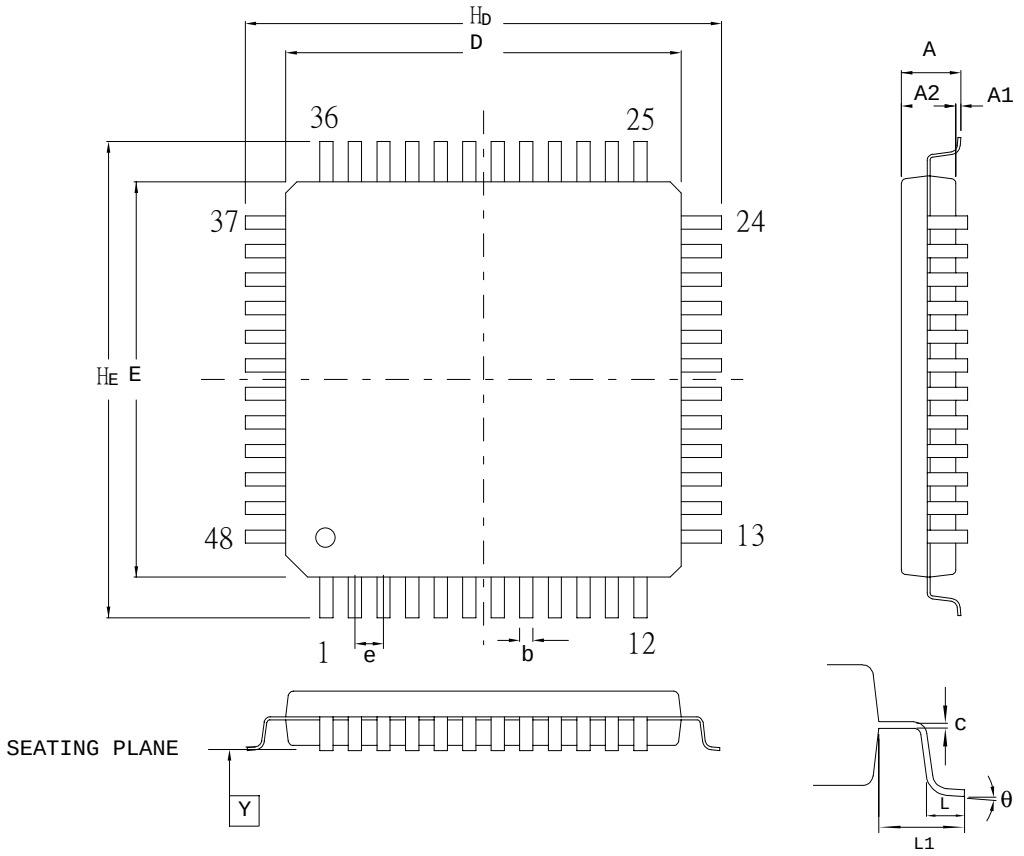
A: IC revision; A means version A, B means version B

01A: for internal use

SA: for internal use

10. PACKAGE DIMENSIONS

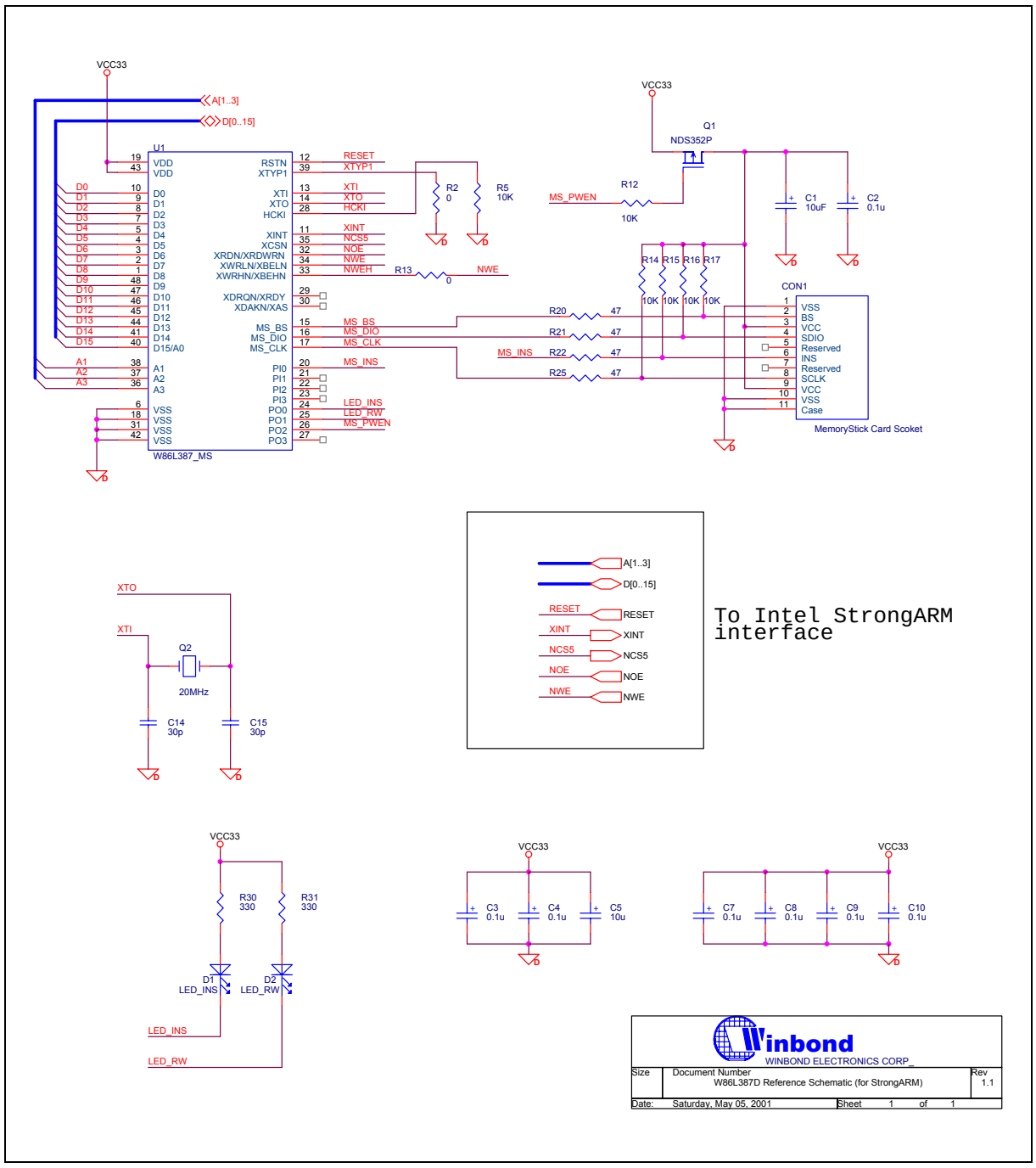
48-LQFP(7x7x1.4mm footprint 2.0mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7 °	0°	—	7 °

11. REFERENCE SCHEMATIC



12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	May 13, 2005	26	ADD Important Notice

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

Please note that all data and specifications are subject to change without notice. All the trademarks of products and companies mentioned in this data sheet belong to their respective owners.

Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
http://www.winbond.com.tw/

Taipei Office
9F, No.480, Rueiguang Rd.,
Neihu District, Taipei, 114,
Taiwan, R.O.C.
TEL: 886-2-8177-7168
FAX: 886-2-8751-3579

Winbond Electronics Corporation America
2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441798

Winbond Electronics Corporation Japan
7F Daini-ueno BLDG, 3-7-18
Shinyokohama Kohoku-ku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Winbond Electronics (Shanghai) Ltd.
27F, 2299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62365998

Winbond Electronics (H.K.) Ltd.
Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064