## Features

- **Single Voltage Operation**
  - **5V Read**
  - **5V Reprogramming**
- **Fast Read Access Time - 45 ns**
- **Internal Program Control and Timer**
- **8K Bytes Boot Block With Lockout**
- **Fast Erase Cycle Time - 10 seconds**
- **Byte-By-Byte Programming - 10 µs/Byte**
- **Hardware Data Protection**
- **$\overline{\text{DATA}}$ Polling For End Of Program Detection**
- **Low Power Dissipation**
  - **30 mA Active Current**
  - **100 µA CMOS Standby Current**
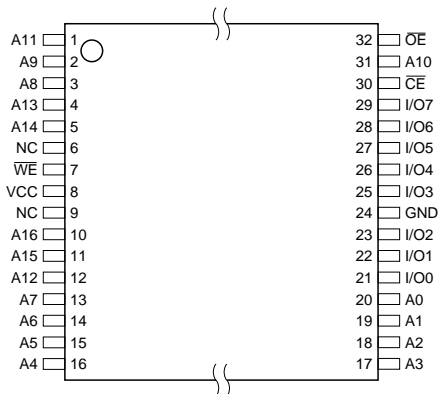- **Typical 10,000 Write Cycles**

## Description

The AT49F010/HF010 are 5-volt only in-system programmable and erasable Flash Memories. Their 1 megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the devices offer access times to 45 ns (HF version) with a power dissipation of just 165 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 100 µA. *(continued)*
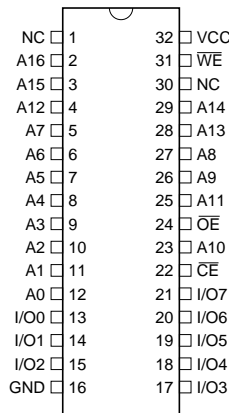
## 1-Megabit (128K x 8) 5-volt Only Flash Memory

## AT49F010
## AT49HF010

## Pin Configurations

| Pin Name | Function |
| --- | --- |
| A0 - A16 | Addresses |
| $\overline{\text{CE}}$ | Chip Enable |
| $\overline{\text{OE}}$ | Output Enable |
| $\overline{\text{WE}}$ | Write Enable |
| I/O0 - I/O7 | Data Inputs/Outputs |
| NC | No Connect |

### TSOP Top View
**Type 1**

| | | |
| --- | --- | --- |
| A11 | 1 | 32 $\overline{\text{OE}}$ |
| A9 | 2 | 31 A10 |
| A8 | 3 | 30 $\overline{\text{CE}}$ |
| A13 | 4 | 29 I/O7 |
| A14 | 5 | 28 I/O6 |
| NC | 6 | 27 I/O5 |
| $\overline{\text{WE}}$ | 7 | 26 I/O4 |
| VCC | 8 | 25 I/O3 |
| NC | 9 | 24 GND |
| A16 | 10 | 23 I/O2 |
| A15 | 11 | 22 I/O1 |
| A12 | 12 | 21 I/O0 |
| A7 | 13 | 20 A0 |
| A6 | 14 | 19 A1 |
| A5 | 15 | 18 A2 |
| A4 | 16 | 17 A3 |

### DIP Top View

| | | |
| --- | --- | --- |
| NC | 1 | 32 VCC |
| A16 | 2 | 31 $\overline{\text{WE}}$ |
| A15 | 3 | 30 NC |
| A12 | 4 | 29 A14 |
| A7 | 5 | 28 A13 |
| A6 | 6 | 27 A8 |
| A5 | 7 | 26 A9 |
| A4 | 8 | 25 A11 |
| A3 | 9 | 24 $\overline{\text{OE}}$ |
| A2 | 10 | 23 A10 |
| A1 | 11 | 22 $\overline{\text{CE}}$ |
| A0 | 12 | 21 I/O7 |
| I/O0 | 13 | 20 I/O6 |
| I/O1 | 14 | 19 I/O5 |
| I/O2 | 15 | 18 I/O4 |
| GND | 16 | 17 I/O3 |

### PLCC Top View

Top row (pins 4,3,2,1,32,31,30): A12, A15, A16, NC, VCC, $\overline{\text{WE}}$, NC

| | | |
| --- | --- | --- |
| A7 | 5 | 29 A14 |
| A6 | 6 | 28 A13 |
| A5 | 7 | 27 A8 |
| A4 | 8 | 26 A9 |
| A3 | 9 | 25 A11 |
| A2 | 10 | 24 $\overline{\text{OE}}$ |
| A1 | 11 | 23 A10 |
| A0 | 12 | 22 $\overline{\text{CE}}$ |
| I/O0 | 13 | 21 I/O7 |

Bottom row (pins 14,15,16,17,18,19,20): I/O1, I/O2, GND, I/O3, I/O4, I/O5, I/O6

**1**

To allow for simple in-system reprogrammability, the AT49F010/HF010 does not require high input voltages for programming. Five-volt-only commands determine the read and programming operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT49F010/HF010 is performed by erasing the entire 1 megabit of memory and then programming on a byte by byte basis. The byte programming time is a fast 50 μs. The end of a program cycle can be optionally detected by the $\overline{DATA}$ polling feature. Once the end of a byte program cycle has been detected, a new access for a read or program can begin. The typical number of program and erase cycles is in excess of 10,000 cycles.

The optional 8K bytes boot block section includes a reprogramming write lock out feature to provide data integrity. The boot sector is designed to contain user secure code, and when the feature is enabled, the boot sector is permanently protected from being reprogrammed.

## Block Diagram
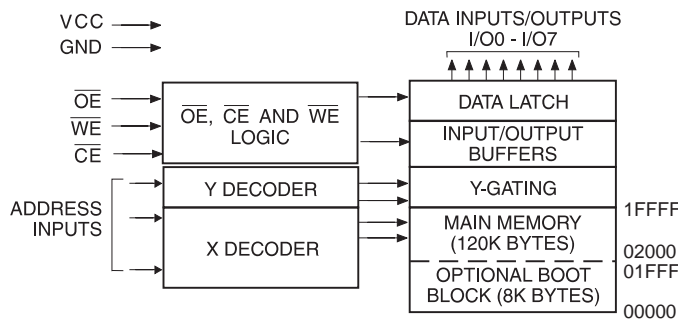


## Device Operation

**READ:** The AT49F010/HF010 is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

**ERASURE:** Before a byte can be reprogrammed, the 128K bytes memory array (or 120K bytes if the boot block featured is used) must be erased. The erased state of the memory bits is a logical "1". The entire device can be erased at one time by using a 6-byte software code. The chip erase code consists of 6-byte load commands to specific address locations with a specific data pattern (please refer to the Chip Erase Cycle Waveforms).

After the chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time needed to erase the whole chip is $t_{EC}$. If the boot block lockout feature has been enabled, the data in the boot sector will not be erased.

**BYTE PROGRAMMING:** Once the memory array is erased, the device is programmed (to a logical "0") on a byte-by-byte basis. Please note that a data "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s. Programming is accomplished via the internal device command register and is a 4 bus cycle operation (please refer to the Command Definitions table). The device will automatically generate the required internal program pulses.

The program cycle has addresses latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last, and the data latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Programming is completed after the specified $t_{BP}$ cycle time. The $\overline{DATA}$ polling feature may also be used to indicate the end of a program cycle.

**BOOT BLOCK PROGRAMMING LOCKOUT:** The device has one designated block that has a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. The size of the block is 8K bytes. This block, referred to as the boot block, can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; the boot block's usage as a write protected region is optional to the user. The address range of the boot block is 00000H to 01FFFH.

Once the feature is enabled, the data in the boot block can no longer be erased or programmed. Data in the main memory block can still be changed through the regular programming method. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. Please refer to the Command Definitions table.

**BOOT BLOCK LOCKOUT DETECTION:** A software method is available to determine if programming of the boot block section is locked out. When the device is in the software product identification mode (see Software Product Identification Entry and Exit sections) a read from address location 00002H will show if programming the boot block is locked out. If the data on I/O0 is low, the boot block can be programmed; if the data on I/O0 is high, the program lockout feature has been activated and the block cannot be programmed. The software product identification code should be used to return to standard operation.

**PRODUCT IDENTIFICATION:** The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

**DATA POLLING:** The AT49F010/HF010 features $\overline{\text{DATA}}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{\text{DATA}}$ polling may begin at any time during the program cycle.

**TOGGLE BIT:** In addition to $\overline{\text{DATA}}$ polling the AT49F010/HF010 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero.

Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

**HARDWARE DATA PROTECTION:** Hardware features protect against inadvertent programs to the AT49F010/HF010 in the following ways: (a) $V_{CC}$ sense—if $V_{CC}$ is below 3.8V (typical), the program function is inhibited; (b) Program inhibit—holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits program cycles; and (c) Noise filter—Pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a program cycle.

## Command Definition (in Hex)

| Command Sequence | Bus Cycles | 1st Bus Cycle | | 2nd Bus Cycle | | 3rd Bus Cycle | | 4th Bus Cycle | | 5th Bus Cycle | | 6th Bus Cycle | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Read | 1 | Addr | $D_{OUT}$ | | | | | | | | | | |
| Chip Erase | 6 | 5555 | AA | 2AAA | 55 | 5555 | 80 | 5555 | AA | 2AAA | 55 | 5555 | 10 |
| Byte Program | 4 | 5555 | AA | 2AAA | 55 | 5555 | A0 | Addr | $D_{IN}$ | | | | |
| Boot Block Lockout[1] | 6 | 5555 | AA | 2AAA | 55 | 5555 | 80 | 5555 | AA | 2AAA | 55 | 5555 | 40 |
| Product ID Entry | 3 | 5555 | AA | 2AAA | 55 | 5555 | 90 | | | | | | |
| Product ID Exit[2] | 3 | 5555 | AA | 2AAA | 55 | 5555 | F0 | | | | | | |
| Product ID Exit[2] | 1 | XXXX | F0 | | | | | | | | | | |

Notes:  1.  The 8K word boot sector has the address range 00000H to 01FFFH.

2.  Either one of the Product ID exit commands can be used.

## Absolute Maximum Ratings*

| |
|---|
| Temperature Under Bias ................................ -55°C to +125°C |
| Storage Temperature ..................................... -65°C to +150°C |
| All Input Voltages (including NC Pins) with Respect to Ground ...................................-0.6V to +6.25V |
| All Output Voltages with Respect to Ground .............................-0.6V to $V_{CC}$ + 0.6V |
| Voltage on $\overline{\text{OE}}$ with Respect to Ground ...................................-0.6V to +13.5V |

*NOTICE:    Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC and AC Operating Range

|  |  | AT49HF010-45 | AT49HF010-55 | AT49F010-70 | AT49F010-90 | AT49F010-12 |
|---|---|---|---|---|---|---|
| Operating Temperature (Case) | Com. | 0°C - 70°C | 0°C - 70°C | 0°C - 70°C | 0°C - 70°C | 0°C - 70°C |
|  | Ind. | -40°C - 85°C | -40°C - 85°C | -40°C - 85°C | -40°C - 85°C | -40°C - 85°C |
| $V_{CC}$ Power Supply |  | 5V ± 10% | 5V ± 10% | 5V ± 10% | 5V ± 10% | 5V ± 10% |

## Operating Modes

| Mode | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | Ai | I/O |
|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | Ai | $D_{OUT}$ |
| Program[2] | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | Ai | $D_{IN}$ |
| Standby/Write Inhibit | $V_{IH}$ | X[1] | X | X | High Z |
| Program Inhibit | X | X | $V_{IH}$ |  |  |
| Program Inhibit | X | $V_{IL}$ | X |  |  |
| Output Disable | X | $V_{IH}$ | X |  | High Z |
| Product Identification |  |  |  |  |  |
| Hardware | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | A1 - A16 = $V_{IL}$, A9 = $V_H$,[3] A0 = $V_{IL}$ | Manufacturer Code[4] |
|  |  |  |  | A1 - A16 = $V_{IL}$, A9 = $V_H$,[3] A0 = $V_{IH}$ | Device Code[4] |
| Software[5] |  |  |  | A0 = $V_{IL}$, A1 - A16 = $V_{IL}$ | Manufacturer Code[4] |
|  |  |  |  | A0 = $V_{IH}$, A1 - A16 = $V_{IL}$ | Device Code[4] |

Notes: 1. X can be $V_{IL}$ or $V_{IH}$.

2. Refer to AC Programming Waveforms.

3. $V_H$ = 12.0V ± 0.5V.

4. Manufacturer Code: 1FH, Device Code: 87H.

5. See details under Software Product Identification Entry/Exit.

## DC Characteristics

| Symbol | Parameter | Condition |  | Min | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN}$ = 0V to $V_{CC}$ |  |  | 10 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{I/O}$ = 0V to $V_{CC}$ |  |  | 10 | µA |
| $I_{SB1}$ | $V_{CC}$ Standby Current CMOS | $\overline{CE}$ = $V_{CC}$ - 0.3V to $V_{CC}$ | Com. |  | 100 | µA |
|  |  |  | Ind. |  | 300 | µA |
| $I_{SB2}$ | $V_{CC}$ Standby Current TTL | $\overline{CE}$ = 2.0V to $V_{CC}$ |  |  | 3 | mA |
| $I_{CC}$[1] | $V_{CC}$ Active Current | f = 5 MHz; $I_{OUT}$ = 0 mA | Com. |  | 30 | mA |
|  |  |  | Ind. |  | 40 | mA |
| $V_{IL}$ | Input Low Voltage |  |  |  | 0.8 | V |
| $V_{IH}$ | Input High Voltage |  |  | 2.0 |  | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1 mA |  |  | 0.45 | V |
| $V_{OH1}$ | Output High Voltage | $I_{OH}$ = -400 µA |  | 2.4 |  | V |
| $V_{OH2}$ | Output High Voltage CMOS | $I_{OH}$ = -100 µA; $V_{CC}$ = 4.5V |  | 4.2 |  | V |

Note: 1. In the erase mode, $I_{CC}$ is 90 mA.

**AT49HF/F010**

## AC Read Characteristics

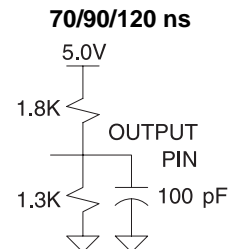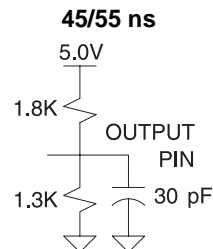| Symbol | Parameter | AT49HF010-45 Min | AT49HF010-45 Max | AT49HF010-55 Min | AT49HF010-55 Max | AT49F010-70 Min | AT49F010-70 Max | AT49F010-90 Min | AT49F010-90 Max | AT49F010-12 Min | AT49F010-12 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{ACC}$ | Address to Output Delay | | 45 | | 55 | | 70 | | 90 | | 120 | ns |
| $t_{CE}$[1] | $\overline{CE}$ to Output Delay | | 45 | | 55 | | 70 | | 90 | | 120 | ns |
| $t_{OE}$[2] | $\overline{OE}$ to Output Delay | | 25 | | 30 | | 35 | 0 | 40 | 0 | 50 | ns |
| $t_{DF}$[3][4] | $\overline{CE}$ or $\overline{OE}$ to Output Float | 0 | 25 | 0 | 25 | 0 | 25 | 0 | 25 | 0 | 30 | ns |
| $t_{OH}$ | Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first | 0 | | 0 | | 0 | | 0 | | 0 | | ns |

## AC Read Waveforms[1][2][3][4]
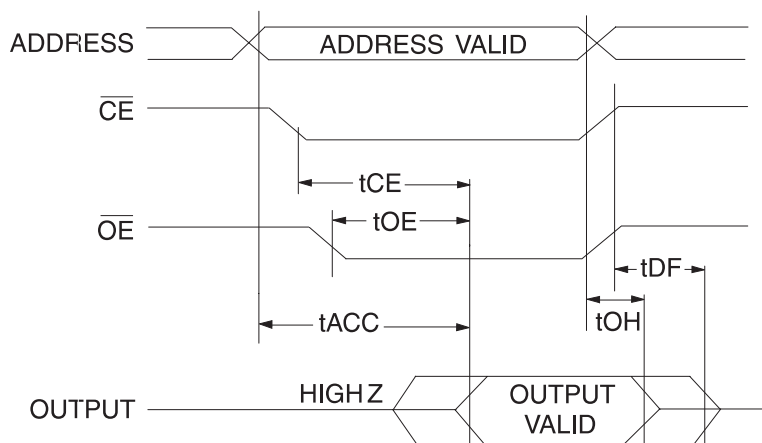


Notes:  1.  $\overline{CE}$ may be delayed up to $t_{ACC}$ - $t_{CE}$ after the address transition without impact on $t_{ACC}$.

2.  $\overline{OE}$ may be delayed up to $t_{CE}$ - $t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{CE}$ or by $t_{ACC}$ - $t_{OE}$ after an address change without impact on $t_{ACC}$.

3.  $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (CL = 5 pF).

4.  This parameter is characterized and is not 100% tested.

## Input Test Waveforms and Measurement Level



AC DRIVING LEVELS

3.0V

0.0V

1.5V

AC MEASUREMENT LEVEL

$t_R$, $t_F$ < 5 ns

## Output Test Load

**45/55 ns**

5.0V
1.8K
OUTPUT PIN
1.3K
30 pF

**70/90/120 ns**

5.0V
1.8K
OUTPUT PIN
1.3K
100 pF
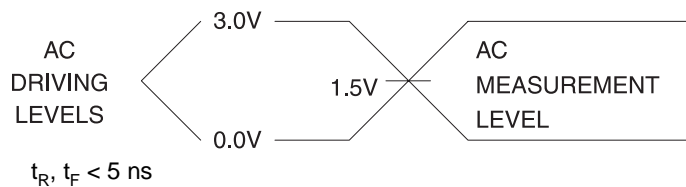
## Pin Capacitance

f = 1 MHz, T = 25°C[1]

| Symbol | Typ | Max | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | 4 | 6 | pF | $V_{IN}$ = 0V |
| $C_{OUT}$ | 8 | 12 | pF | $V_{OUT}$ = 0V |

Note:  1.  This parameter is characterized and is not 100% tested.

**5**

## AC Byte Load Characteristics

| Symbol | Parameter | Min | Max | Units |
|--------|-----------|-----|-----|-------|
| $t_{AS}$, $t_{OES}$ | Address, $\overline{OE}$ Set-up Time | 0 | | ns |
| $t_{AH}$ | Address Hold Time | 50 | | ns |
| $t_{CS}$ | Chip Select Set-up Time | 0 | | ns |
| $t_{CH}$ | Chip Select Hold Time | 0 | | ns |
| $t_{WP}$ | Write Pulse Width ($\overline{WE}$ or $\overline{CE}$) | 90 | | ns |
| $t_{DS}$ | Data Set-up Time | 50 | | ns |
| $t_{DH}$, $t_{OEH}$ | Data, $\overline{OE}$ Hold Time | 0 | | ns |
| $t_{WPH}$ | Write Pulse Width High | 90 | | ns |

## AC Byte Load Waveforms

### $\overline{WE}$ Controlled



### $\overline{CE}$ Controlled

## AT49HF/F010
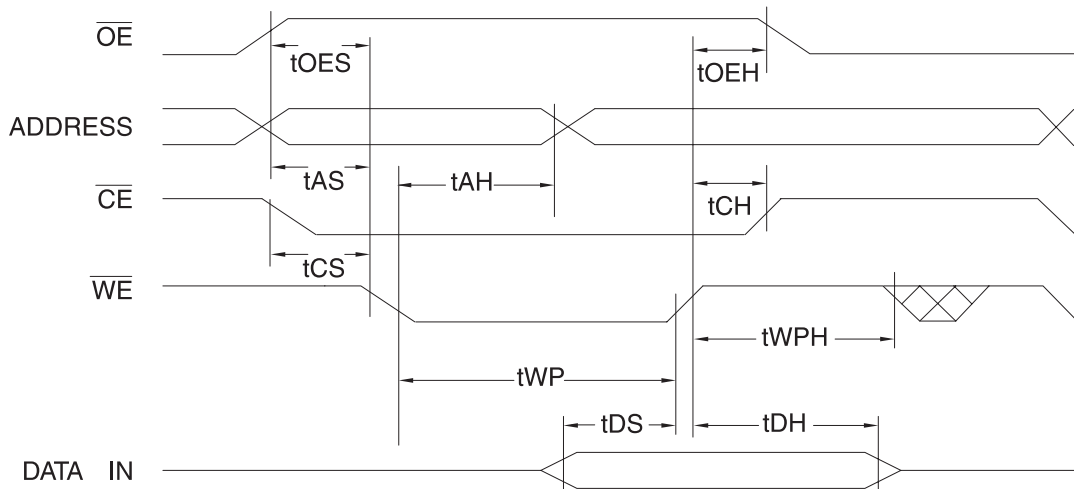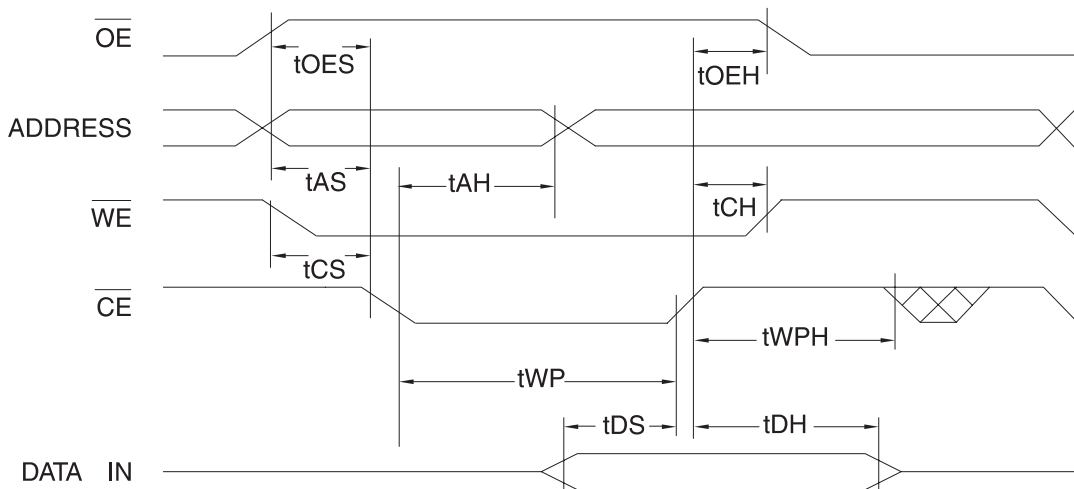
## Program Cycle Characteristics

| Symbol | Parameter | Min | Typ | Max | Units |
|--------|-----------|-----|-----|-----|-------|
| $t_{BP}$ | Byte Programming Time | | 10 | 50 | μs |
| $t_{AS}$ | Address Set-up Time | 0 | | | ns |
| $t_{AH}$ | Address Hold Time | 50 | | | ns |
| $t_{DS}$ | Data Set-up Time | 50 | | | ns |
| $t_{DH}$ | Data Hold Time | 0 | | | ns |
| $t_{WP}$ | Write Pulse Width | 90 | | | ns |
| $t_{WPH}$ | Write Pulse Width High | 90 | | | ns |
| $t_{EC}$ | Erase Cycle Time | | | 10 | seconds |

## Program Cycle Waveforms
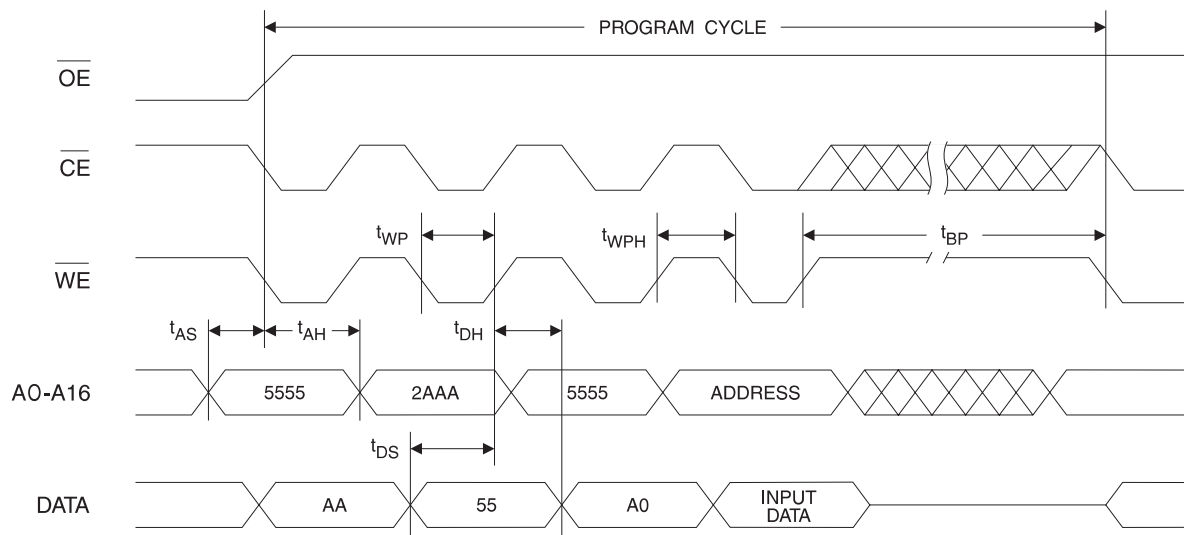


## Chip Erase Cycle Waveforms
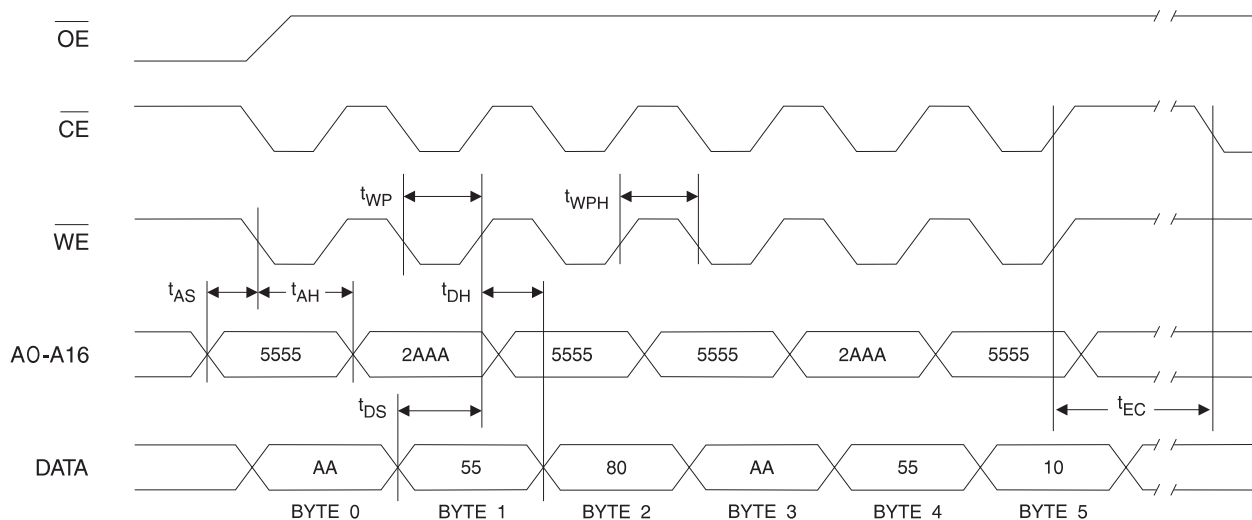


Note:    1.    $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
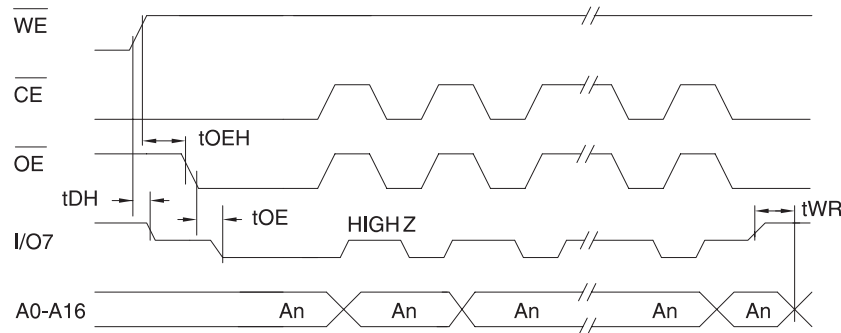
## $\overline{\text{Data}}$ Polling Characteristics[1]

| Symbol | Parameter | Min | Typ | Max | Units |
|--------|-----------|-----|-----|-----|-------|
| $t_{DH}$ | Data Hold Time | 10 | | | ns |
| $t_{OEH}$ | $\overline{\text{OE}}$ Hold Time | 10 | | | ns |
| $t_{OE}$ | $\overline{\text{OE}}$ to Output Delay[2] | | | | ns |
| $t_{WR}$ | Write Recovery Time | 0 | | | ns |

Notes:  1.  These parameters are characterized and not 100% tested.

2.  See $t_{OE}$ spec in AC Read Characteristics.

## $\overline{\text{Data}}$ Polling Waveforms



## Toggle Bit Characteristics[1]

| Symbol | Parameter | Min | Typ | Max | Units |
|--------|-----------|-----|-----|-----|-------|
| $t_{DH}$ | Data Hold Time | 10 | | | ns |
| $t_{OEH}$ | $\overline{\text{OE}}$ Hold Time | 10 | | | ns |
| $t_{OE}$ | $\overline{\text{OE}}$ to Output Delay[2] | | | | ns |
| $t_{OEHP}$ | $\overline{\text{OE}}$ High Pulse | 150 | | | ns |
| $t_{WR}$ | Write Recovery Time | 0 | | | ns |

Notes:  1.  These parameters are characterized and not 100% tested.

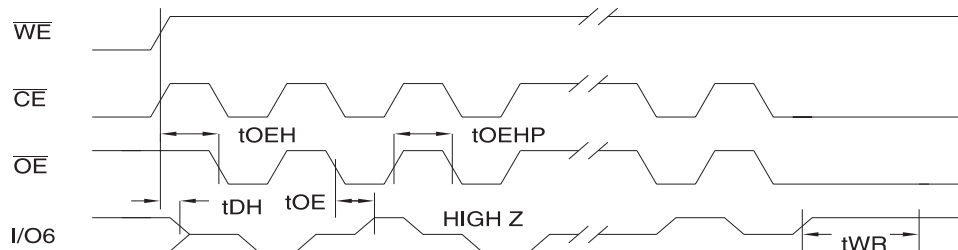2.  See $t_{OE}$ spec in AC Read Characteristics.

## Toggle Bit Waveforms[1][2][3]



Notes:  1.  Toggling either $\overline{\text{OE}}$ or $\overline{\text{CE}}$ or both $\overline{\text{OE}}$ and $\overline{\text{CE}}$ will operate toggle bit. The $t_{OEHP}$ specification must be met by the toggling input(s).

2.  Beginning and ending state of I/O6 will vary.

3.  Any address location may be used by the address should not vary.

## Software Product Identification Entry[1]

```
LOAD DATA AA
TO
ADDRESS 5555
```
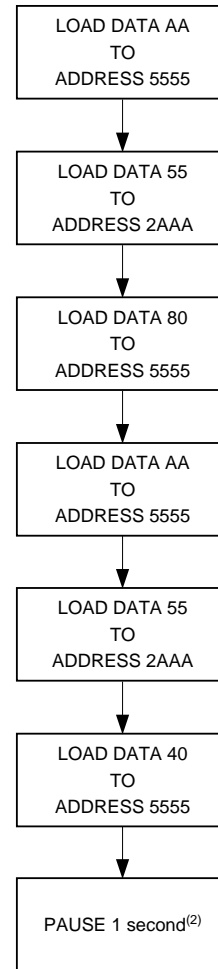↓
```
LOAD DATA 55
TO
ADDRESS 2AAA
```
↓
```
LOAD DATA 90
TO
ADDRESS 5555
```
↓
```
ENTER PRODUCT
IDENTIFICATION
MODE[2][3][5]
```

## Software Product Identification Exit[1]

```
LOAD DATA AA      OR      LOAD DATA F0
TO                        TO
ADDRESS 5555              ANY ADDRESS
```
↓                         ↓
```
LOAD DATA 55              EXIT PRODUCT
TO                        IDENTIFICATION
ADDRESS 2AAA              MODE[4]
```
↓
```
LOAD DATA F0
TO
ADDRESS 5555
```
↓
```
EXIT PRODUCT
IDENTIFICATION
MODE[4]
```
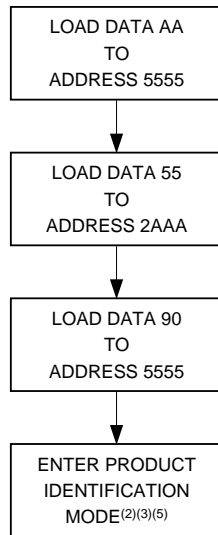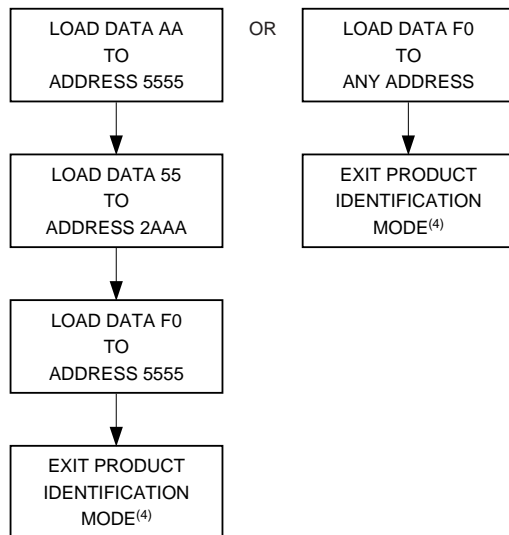
Notes for software product identification:

1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).

2. A1 - A16 = $V_{IL}$.
   Manufacturer Code is read for A0 = $V_{IL}$;
   Device Code is read for A0 = $V_{IH}$.

3. The device does not remain in identification mode if powered down.

4. The device returns to standard operation mode.

5. Manufacturer Code is 1FH. The Device Code is 17H.

## Boot Block Lockout Feature Enable Algorithm[1]

```
LOAD DATA AA
TO
ADDRESS 5555
```
↓
```
LOAD DATA 55
TO
ADDRESS 2AAA
```
↓
```
LOAD DATA 80
TO
ADDRESS 5555
```
↓
```
LOAD DATA AA
TO
ADDRESS 5555
```
↓
```
LOAD DATA 55
TO
ADDRESS 2AAA
```
↓
```
LOAD DATA 40
TO
ADDRESS 5555
```
↓
```
PAUSE 1 second[2]
```

Notes for boot block lockout feature enable:

1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).

2. Boot block lockout feature enabled.
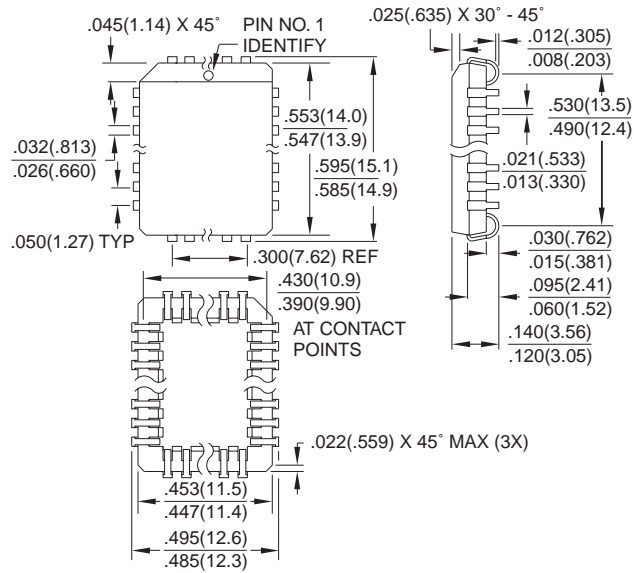
## Ordering Information[1]

| t$_{ACC}$ (ns) | I$_{CC}$ (mA) | | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| | Active | Standby | | | |
| 45 | 30 | 0.1 | AT49HF010-45JC<br>AT49HF010-45PC<br>AT49HF010-45TC | 32J<br>32P6<br>32T | Commercial<br>(0° to 70°C) |
| | 40 | 0.3 | AT49HF010-45JI<br>AT49HF010-45PI<br>AT49HF010-45TI | 32J<br>32P6<br>32T | Industrial<br>(-40° to 85°C) |
| 55 | 30 | 0.1 | AT49HF010-55JC<br>AT49HF010-55PC<br>AT49HF010-55TC | 32J<br>32P6<br>32T | Commercial<br>(0° to 70°C) |
| | 40 | 0.3 | AT49HF010-55JI<br>AT49HF010-55PI<br>AT49HF010-55TI | 32J<br>32P6<br>32T | Industrial<br>(-40° to 85°C) |
| 70 | 30 | 0.1 | AT49F010-70JC<br>AT49F010-70PC<br>AT49F010-70TC | 32J<br>32P6<br>32T | Commercial<br>(0° to 70°C) |
| | 40 | 0.3 | AT49F010-70JI<br>AT49F010-70PI<br>AT49F010-70TI | 32J<br>32P6<br>32T | Industrial<br>(-40° to 85°C) |
| 90 | 30 | 0.1 | AT49F010-90JC<br>AT49F010-90PC<br>AT49F010-90TC | 32J<br>32P6<br>32T | Commercial<br>(0° to 70°C) |
| | 40 | 0.3 | AT49F010-90JI<br>AT49F010-90PI<br>AT49F010-90TI | 32J<br>32P6<br>32T | Industrial<br>(-40° to 85°C) |
| 120 | 30 | 0.1 | AT49F010-12JC<br>AT49F010-12PC<br>AT49F010-12TC | 32J<br>32P6<br>32T | Commercial<br>(0° to 70°C) |
| | 40 | 0.3 | AT49F010-12JI<br>AT49F010-12PI<br>AT49F010-12TI | 32J<br>32P6<br>32T | Industrial<br>(-40° to 85°C) |

Note:   1.  The AT49F010/HF010 has an optional boot block feature. The part number shown in the Ordering Information table is for devices with the boot block in the lower address range (i.e., 00000H to 01FFFH). Users requiring the boot block to be in the higher address range should contact Atmel.
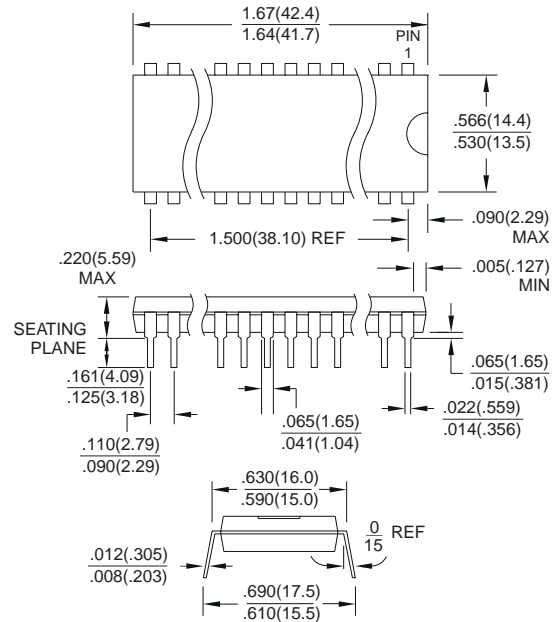
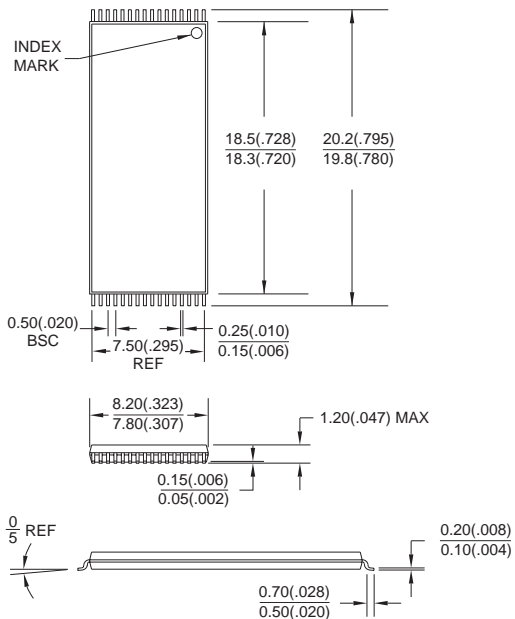| Package Type | |
|---|---|
| **32J** | 32-Lead, Plastic, J-Leaded Chip Carrier Package (PLCC) |
| **32P6** | 32-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP) |
| **32T** | 32-Lead, Thin Small Outline Package (TSOP) |

# Packaging Information

**32J**, 32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE MS-016 AE

.045(1.14) X 45°  PIN NO. 1 IDENTIFY
.025(.635) X 30° - 45°
.012(.305) / .008(.203)
.553(14.0) / .547(13.9)
.530(13.5) / .490(12.4)
.032(.813) / .026(.660)
.595(15.1) / .585(14.9)
.021(.533) / .013(.330)
.050(1.27) TYP
.300(7.62) REF
.030(.762) / .015(.381)
.430(10.9) / .390(9.90)
AT CONTACT POINTS
.095(2.41) / .060(1.52)
.140(3.56) / .120(3.05)
.022(.559) X 45° MAX (3X)
.453(11.5) / .447(11.4)
.495(12.6) / .485(12.3)

**32P6**, 32-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)

1.67(42.4) / 1.64(41.7)
PIN 1
.566(14.4) / .530(13.5)
1.500(38.10) REF
.090(2.29) MAX
.220(5.59) MAX
.005(.127) MIN
SEATING PLANE
.161(4.09) / .125(3.18)
.065(1.65) / .015(.381)
.065(1.65) / .041(1.04)
.022(.559) / .014(.356)
.110(2.79) / .090(2.29)
.630(16.0) / .590(15.0)
$\frac{0}{15}$ REF
.012(.305) / .008(.203)
.690(17.5) / .610(15.5)

**32T**, 32-Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*
JEDEC OUTLINE MO-142 BD

INDEX MARK
18.5(.728) / 18.3(.720)
20.2(.795) / 19.8(.780)
0.50(.020) BSC
7.50(.295) REF
0.25(.010) / 0.15(.006)
8.20(.323) / 7.80(.307)
1.20(.047) MAX
0.15(.006) / 0.05(.002)
$\frac{0}{5}$ REF
0.20(.008) / 0.10(.004)
0.70(.028) / 0.50(.020)

*Controlling dimension: millimeters

## Atmel Headquarters

### Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

### Europe
Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686677
FAX (44) 1276-686697

### Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road
Tsimshatsui East
Kowloon, Hong Kong
TEL (852) 27219778
FAX (852) 27221369

### Japan
Atmel Japan K.K.
Tonetsu Shinkawa Bldg., 9F
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

## Atmel Operations

### Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

### Atmel Rousset
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4 42 53 60 00
FAX (33) 4 42 53 60 01

### Fax-on-Demand
North America:
1-(800) 292-8635

International:
1-(408) 441-0732

### e-mail
literature@atmel.com

### Web Site
http://www.atmel.com

### BBS
1-(408) 436-4309

© **Atmel Corporation 1998.**

Atmel Corporation makes no warranty for the use of its products, other than those expressly contained in the Company's standard warranty which is detailed in Atmel's Terms and Conditions located on the Company's website. The Company assumes no responsibility for any errors which may appear in this document, reserves the right to change devices or specifications detailed herein at any time without notice, and does not make any commitment to update the information contained herein. No licenses to patents or other intellectual property of Atmel are granted by the Company in connection with the sale of Atmel products, expressly or by implication. Atmel's products are not authorized for use as critical components in life support devices or systems.

Marks bearing ® and/or ™ are registered trademarks and trademarks of Atmel Corporation.

Terms and product names in this document may be trademarks of others.

Printed on recycled paper.

0852B–10/98/xM