CY62167DV30

MoBL®

16-Mbit (1M x 16) Static RAM

Features

- **Very high speed: 45 ns**
- **Wide voltage range: 2.20V – 3.60V**
- **Ultra-low active power**
  - **Typical active current: 2 mA @ f = 1 MHz**
  - **Typical active current: 18.5 mA @ f = f_{max} (45 ns speed)**
- **Ultra-low standby power**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Packages offered in a 48-ball BGA and 48-pin TSOPI**

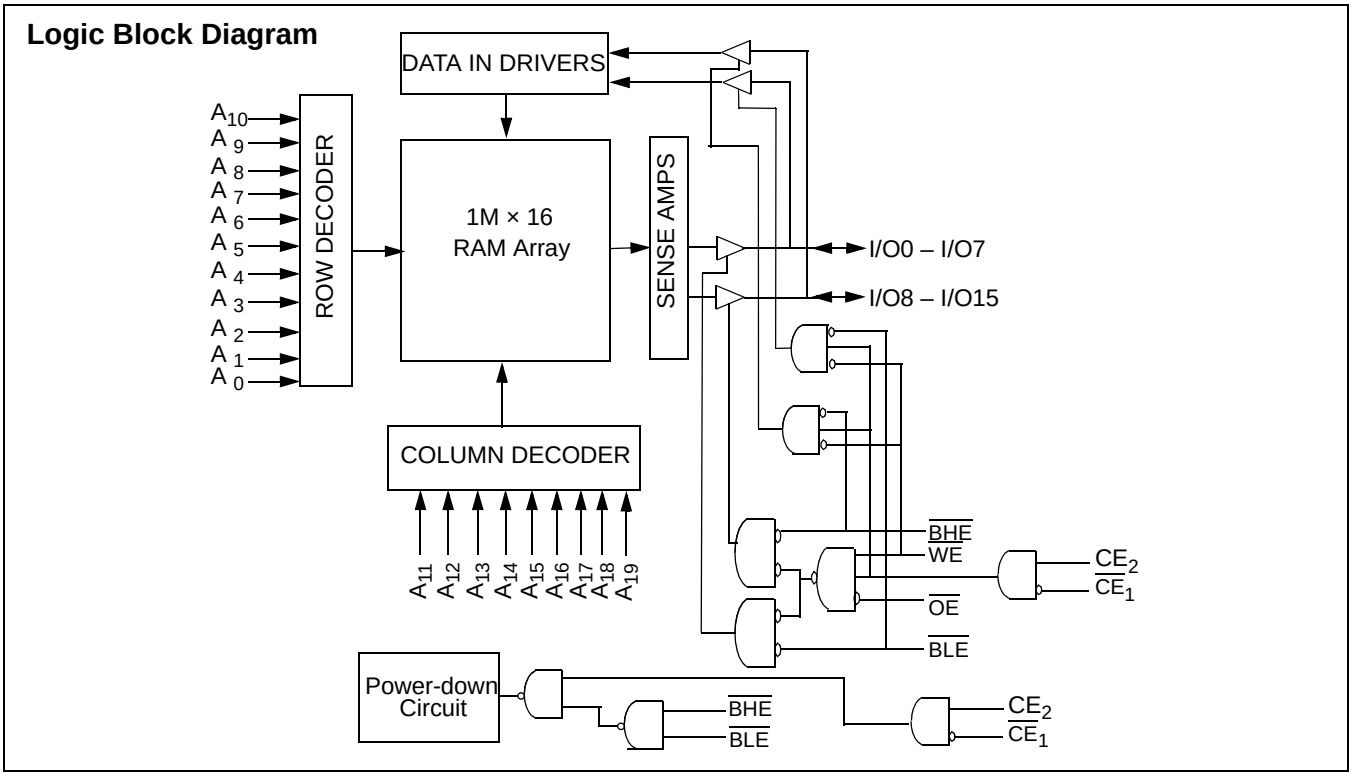
Functional Description[1]

The CY62167DV30 is a high-performance CMOS static RAM organized as 1M words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a Write operation ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{19}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{19}).

Reading from the device is accomplished by taking Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table at the back of this data sheet for a complete description of Read and Write modes.

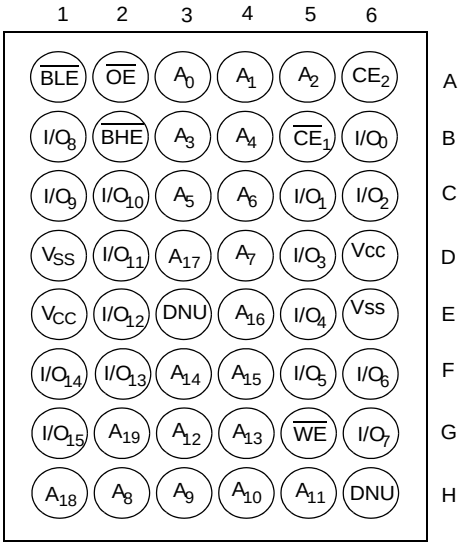
Logic Block Diagram



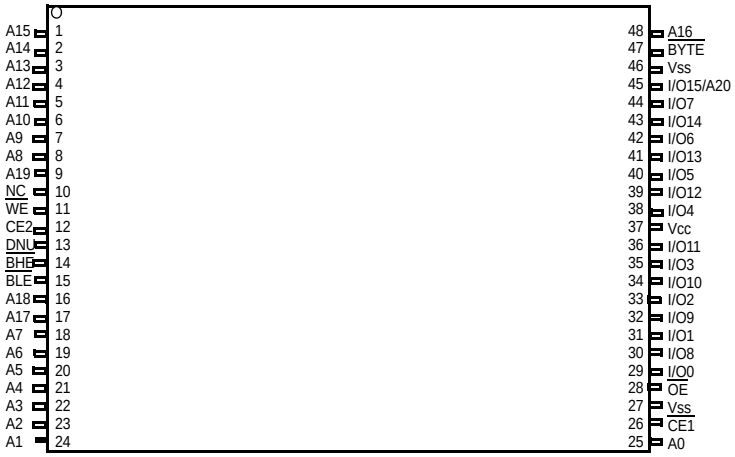
Note:
1. For best-practice recommendations, please refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com.

Pin Configuration[2, 3, 4, 5]

FBGA
Top View



48TSOPI (Forward)
Top View



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC}(mA)				Standby I_{SB2}(µA)	
					f = 1MHz		f = f_{max}			
	Min.	Typ.[6]	Max.		Typ.[6]	Max.	Typ.[6]	Max.	Typ.[6]	Max.
CY62167DV30L	2.20	3.0	3.60	45	2	4	18.5	37	2.5	30
				55			15	30		
				70			12	25		
CY62167DV30LL				45			18.5	37	2.5	22
				55			15	30		
				70			12	25		

Notes:
2. NC pins are not connected on the die.
3. DNU pins have to be left floating.
4. The BYTE pin in the 48-TSOPI package has to be tied HIGH to use the device as a 1M × 16 SRAM. The 48-TSOPI package can also be used as a 2M × 8 SRAM by tying the BYTE signal LOW. For 2M × 8 Functionality, please refer to the CY62168DV30 datasheet. In the 2M × 8 configuration, Pin 45 is A20.
5. Ball H6 for the FBGA package can be used to upgrade to a 32M density.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25°C$.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential .....–0.2V to V_{CC} + 0.3V

DC Voltage Applied to Outputs in High-Z State[7, 8].....–0.2V to V_{CC} + 0.3V

DC Input Voltage[7, 8] .....–0.2V to V_{CC} + 0.3V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[9]
CY62167DV30L	Industrial	–40°C to +85°C	2.20V to 3.60V
CY62167DV30LL			

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			CY62167DV30-45			CY62167DV30-55			CY62167DV30-70			Unit
					Min.	Typ.[6]	Max.	Min.	Typ.[6]	Max.	Min.	Typ.[6]	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	V_{CC} = 2.20V		2.0			2.0			2.0			V
		I_{OH} = –1.0 mA	V_{CC} = 2.70V		2.4			2.4			2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	V_{CC} = 2.20V				0.4			0.4			0.4	V
		I_{OL} = 2.1mA	V_{CC} = 2.70V				0.4			0.4			0.4	V
V_{IH}	Input HIGH Voltage	V_{CC} = 2.2V to 2.7V			1.8		V_{CC} +0.3V	1.8		V_{CC} +0.3V	1.8		V_{CC} +0.3V	V
		V_{CC}= 2.7V to 3.6V			2.2		V_{CC} +0.3V	2.2		V_{CC} +0.3V	2.2		V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage	V_{CC} = 2.2V to 2.7V			–0.3		0.6	–0.3		0.6	–0.3		0.6	V
		V_{CC}= 2.7V to 3.6V			–0.3		0.8	–0.3		0.8	–0.3		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}			–1		+1	–1		+1	–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			–1		+1	–1		+1	–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = V_{CCmax} I_{OUT} = 0 mA CMOS levels	f = f_{MAX} = $1/t_{RC}$			18.5	37		15	30		12	25	mA
			f = 1 MHz			2	4		2	4		2	4	mA
I_{SB1}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE_1}$ ≥ V_{CC} – 0.2V or CE_2 ≤ 0.2V V_{IN} ≥ V_{CC} – 0.2V, V_{IN} ≤ 0.2V) f = f_{MAX} (Address and Data Only), f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$, $\overline{BLE}$), V_{CC} = 3.60V		L		2.5	30		2.5	30		2.5	30	µA
				LL		2.5	22		2.5	22		2.5	22	
I_{SB2}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE_1}$ ≥ V_{CC} – 0.2V or CE_2 ≤ 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = 3.60V		L		2.5	30		2.5	30		2.5	30	µA
				LL		2.5	22		2.5	22		2.5	22	

Notes:
7. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
8. $V_{IH(Max)}$ = V_{CC} + 0.75V for pulse durations less than 20 ns.
9. Full Device AC operation requires linear V_{CC} ramp from 0 to $V_{CC(min.)}$ > = 500 µs.

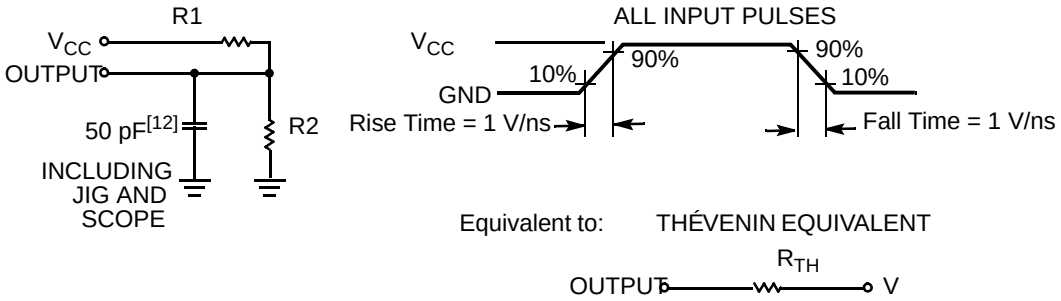
Capacitance[10, 11]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	8	pF
C_{OUT}	Output Capacitance		10	pF

Thermal Resistance

Parameter	Description	Test Conditions	BGA	TSOP I	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)[10]	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	55	60	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)[10]		16	4.3	°C/W

AC Test Loads and Waveforms[12]

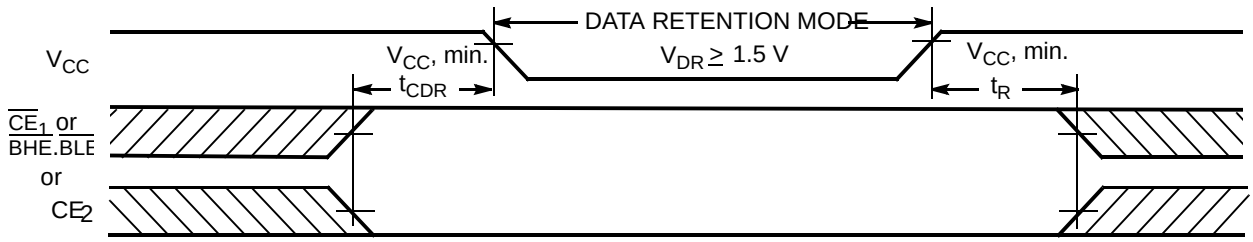


Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions		Min.	Typ.[6]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			1.5			V
I_{CCDR}	Data Retention Current	V_{CC}= 1.5V $\overline{CE_1} \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	L			15	µA
			LL			10	
t_{CDR}[10]	Chip Deselect to Data Retention Time			0			ns
t_R[13]	Operation Recovery Time			t_{RC}			ns

Data Retention Waveform[14]



Notes:
10. Tested initially and after any design or process changes that may affect these parameters.
11. This applies for all packages.
12. Test condition for the 45 ns part is a load capacitance of 30 pF
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.
14. BHE.BLE is the AND of both BHE and BLE. Chip can be deselected by either disabling the chip enable signals or by disabling both BHE and BLE.

Switching Characteristics Over the Operating Range[15]

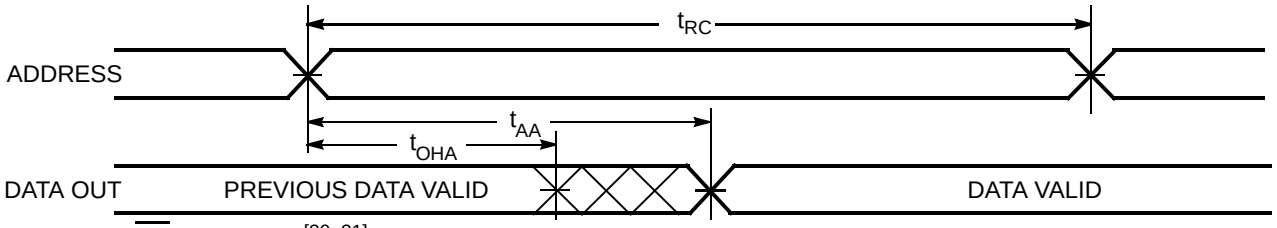
Parameter	Description	45 ns [12]		55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	45		55		70		ns
t_{AA}	Address to Data Valid		45		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		10		ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Data Valid		45		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[16]	5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[16, 17]		15		20		25	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[16]	10		10		10		ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z[16, 17]		20		20		25	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power-up	0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to Power-down		45		55		70	ns
t_{DBE}	BLE/BHE LOW to Data Valid		45		55		70	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low Z[16]	10		10		10		ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z[16, 17]		15		20		25	ns
Write Cycle[18]								
t_{WC}	Write Cycle Time	45		55		70		ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Write End	40		40		60		ns
t_{AW}	Address Set-Up to Write End	40		40		60		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	35		40		45		ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to Write End	40		40		60		ns
t_{SD}	Data Set-Up to Write End	25		25		30		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[16, 17]		15		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[16]	10		10		10		ns

Notes:

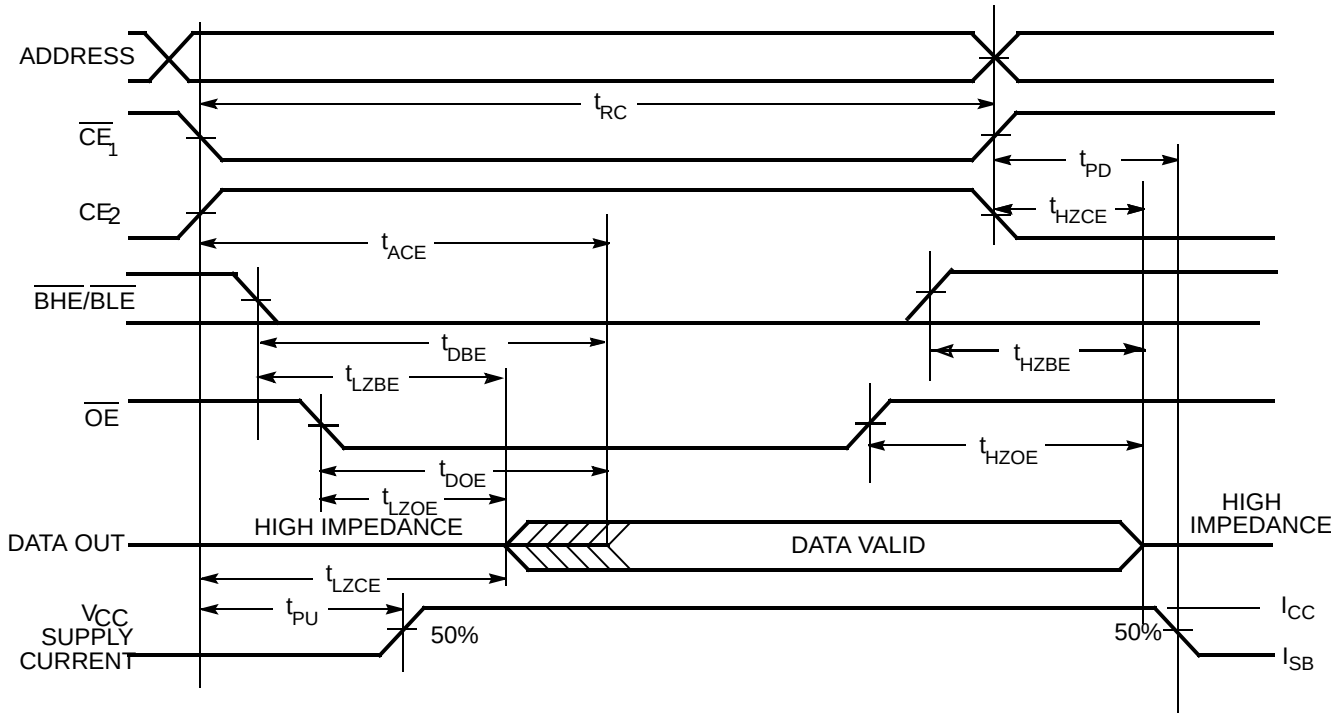
15. Test conditions for all parameters other than three-state parameters assume signal transition time of 1 ns/V, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
16. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
17. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
18. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the Write.

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)[19, 20]



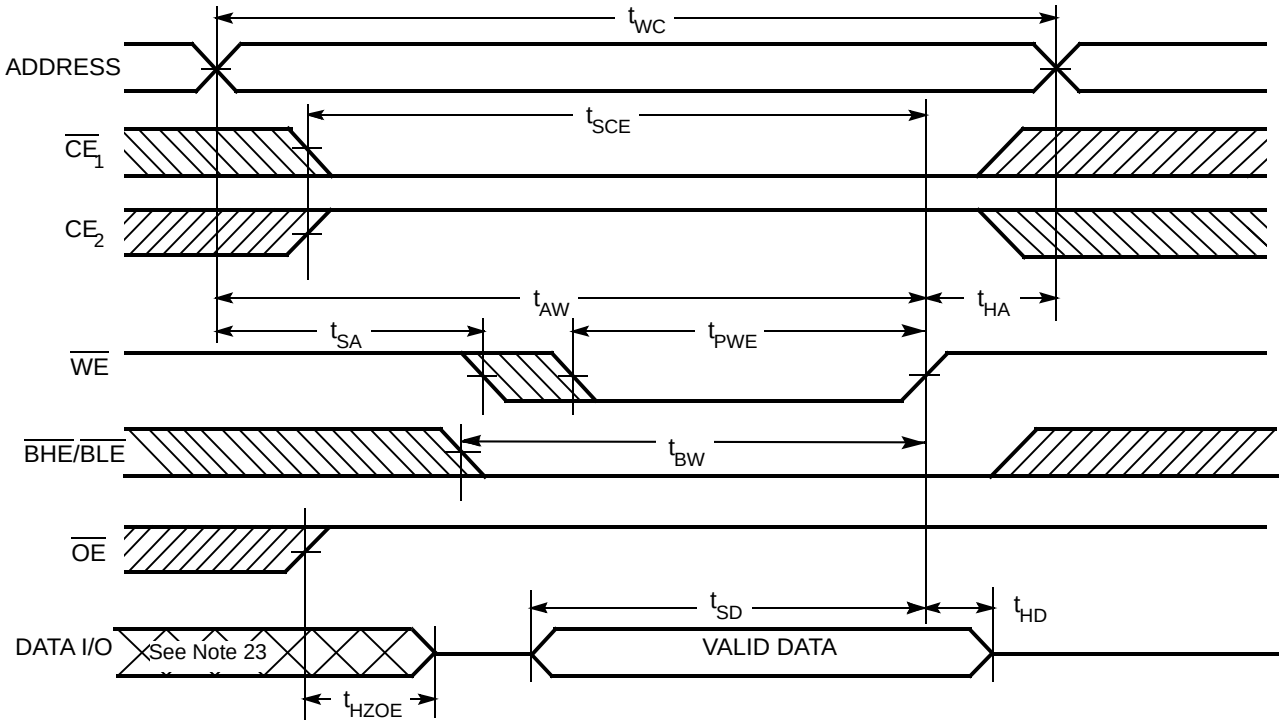
Read Cycle 2 (OE Controlled)[20, 21]



Notes:
19. The device is continuously selected. $\overline{OE}$, $\overline{CE_1} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$.
20. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

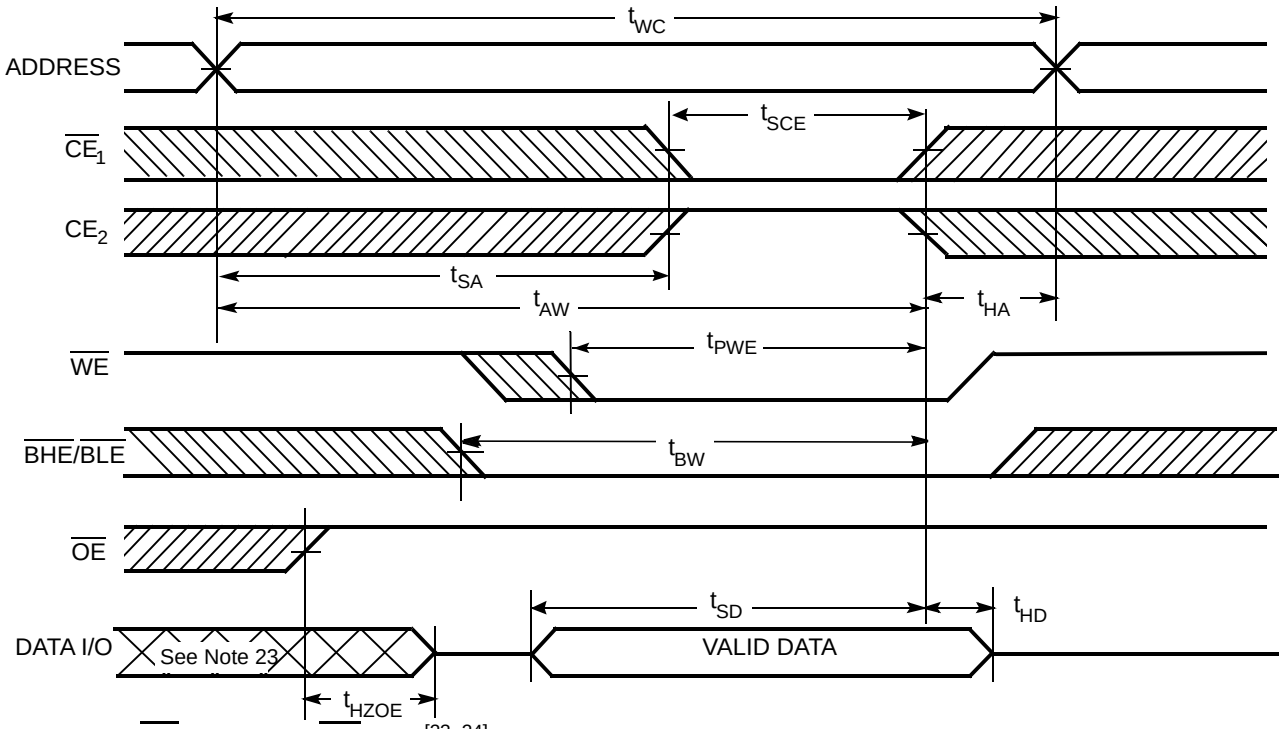
Write Cycle 1 ($\overline{WE}$ Controlled)[18, 22, 23, 24]



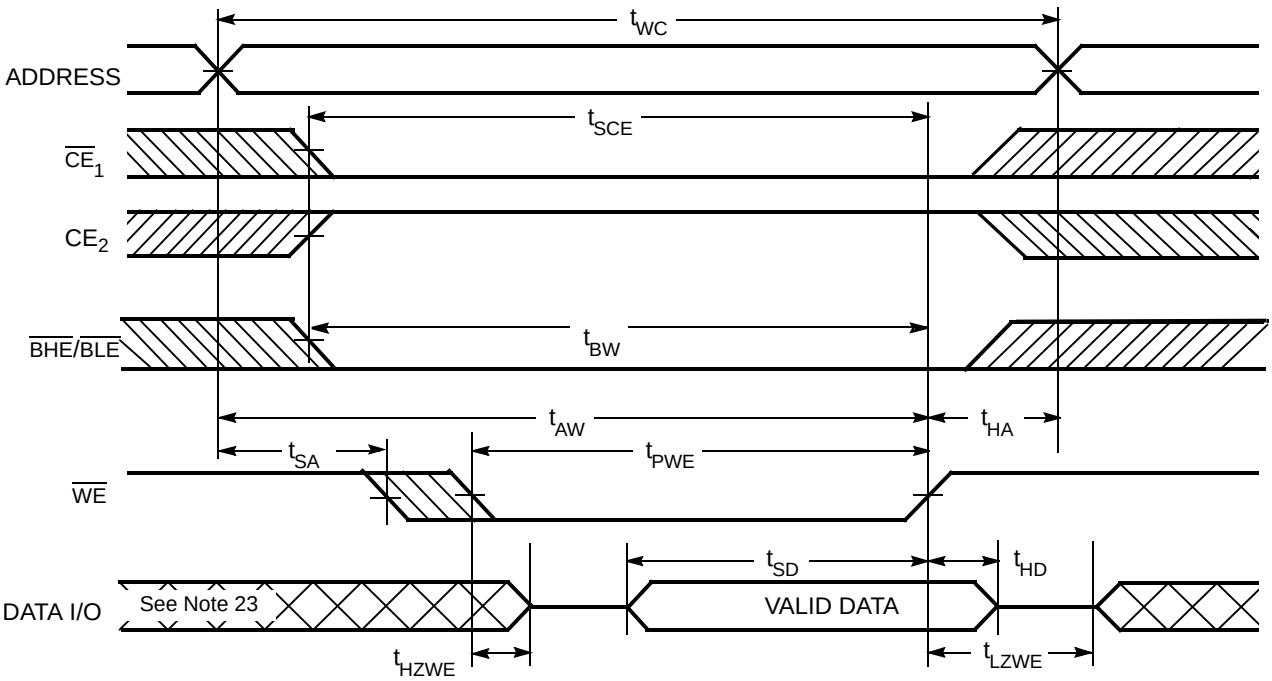
Notes:
21. Address valid prior to or coincident with $\overline{CE_1}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.
22. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
23. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high-impedance state.
24. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle 2 ($\overline{CE}_1$ or CE_2 Controlled)[18, 22, 23, 24]

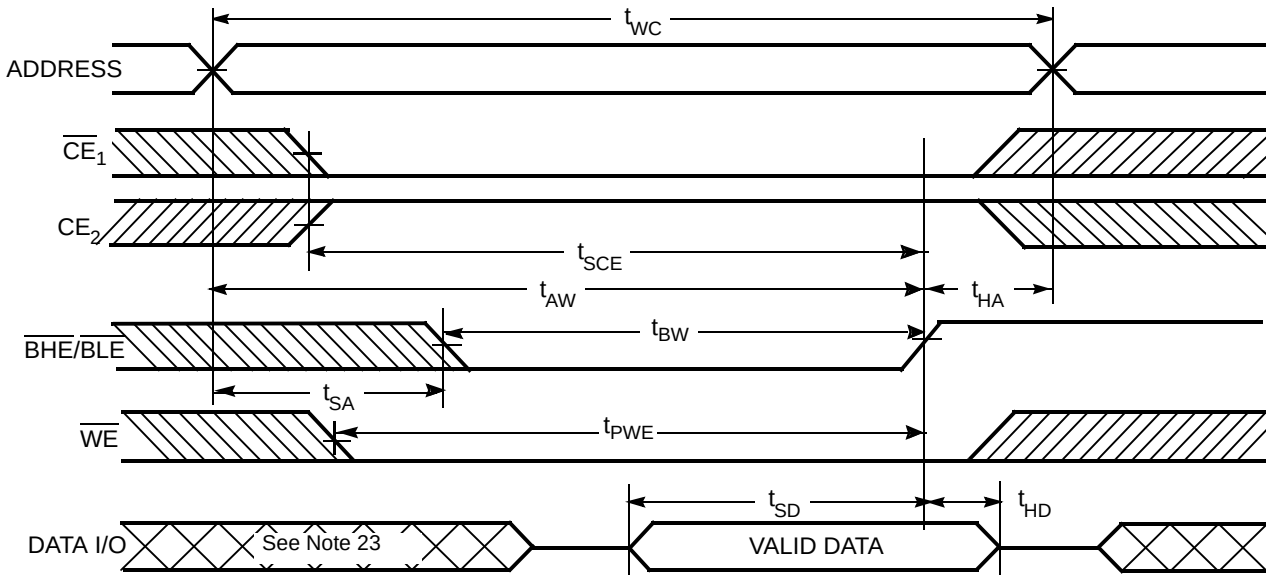


Write Cycle 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[23, 24]



Switching Waveforms (continued)

Write Cycle 4 ($\overline{BHE}$/$\overline{BLE}$ Controlled, $\overline{OE}$ LOW)[23, 24]



Truth Table

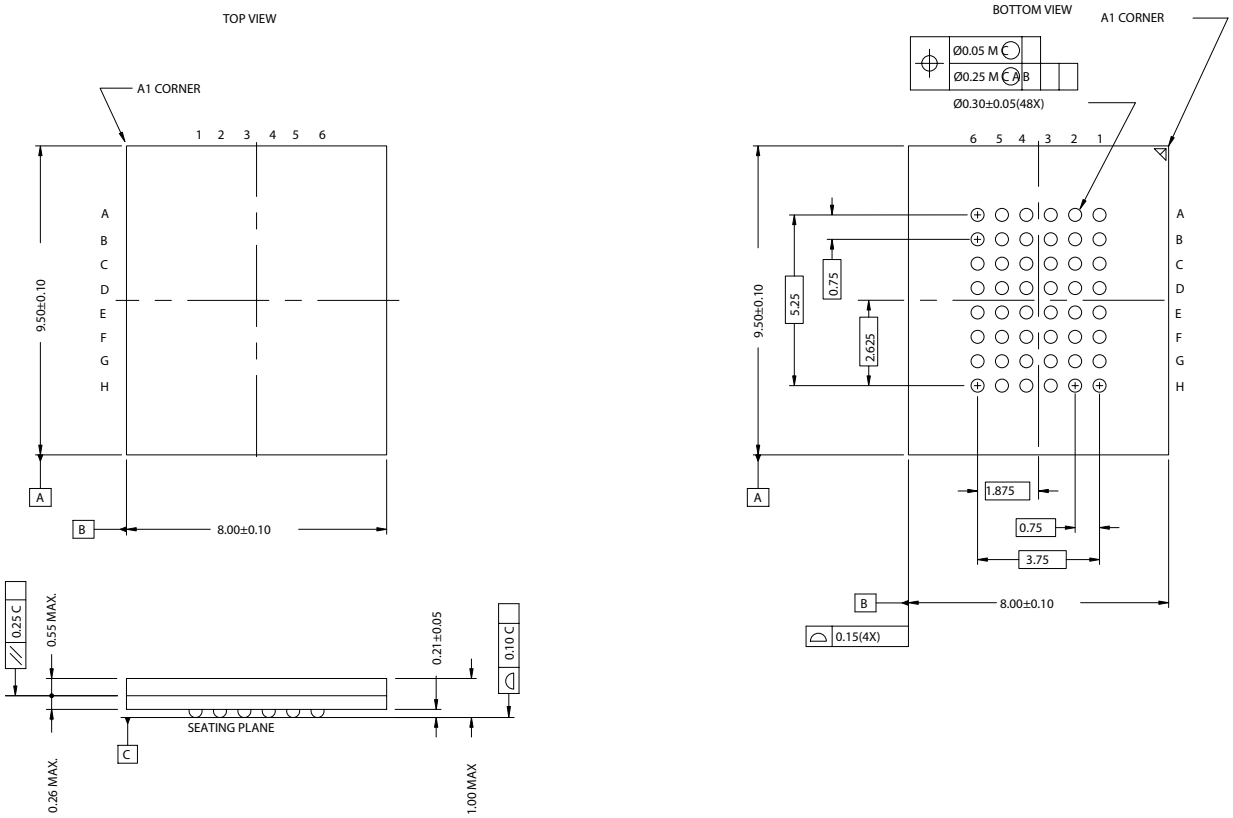
$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O_0–I/O_7); Data Out (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	High Z (I/O_0–I/O_7); Data In (I/O_8–I/O_{15})	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY62167DV30L-45ZI	Z48A	48 Pin TSOP I	Industrial
	CY62167DV30LL-45ZI			
	CY62167DV30LL-45ZXI	Z48A	48 Pin TSOP I (Pb-Free)	Industrial
55	CY62167DV30L-55BVI	BV48B	48-ball Fine Pitch BGA (8 mm × 9.5mm × 1 mm)	Industrial
	CY62167DV30LL-55BVI	BV48B	48-ball Fine Pitch BGA (8 mm × 9.5mm × 1 mm)	Industrial
	CY62167DV30LL-55BVXI	BV48B	48-ball Fine Pitch BGA (8 mm × 9.5mm × 1 mm) (Pb-Free)	Industrial
	CY62167DV30L-55ZI	Z48A	48 Pin TSOP I	Industrial
	CY62167DV30LL-55ZI	Z48A	48-pin TSOP I	Industrial
	CY62167DV30LL-55ZXI	Z48A	48-pin TSOP I (Pb-Free)	Industrial
70	CY62167DV30L-70BVI	BV48B	48-ball Fine Pitch BGA (8 mm × 9.5mm × 1 mm)	Industrial
	CY62167DV30LL-70BVI	BV48B	48-ball Fine Pitch BGA (8 mm × 9.5mm × 1 mm)	Industrial
	CY62167DV30LL-70BVXI	BV48B	48-ball Fine Pitch BGA (8 mm × 9.5mm × 1 mm) (Pb-Free)	Industrial
	CY62167DV30L-70ZI	Z48A	48-pin TSOP I	Industrial
	CY62167DV30LL-70ZI	Z48A	48-pin TSOP I	Industrial
	CY62167DV30LL-70ZXI	Z48A	48-pin TSOP I (Pb-Free)	Industrial

Package Diagrams

48-Lead VFBGA (8 x 9.5 x 1 mm) BV48B

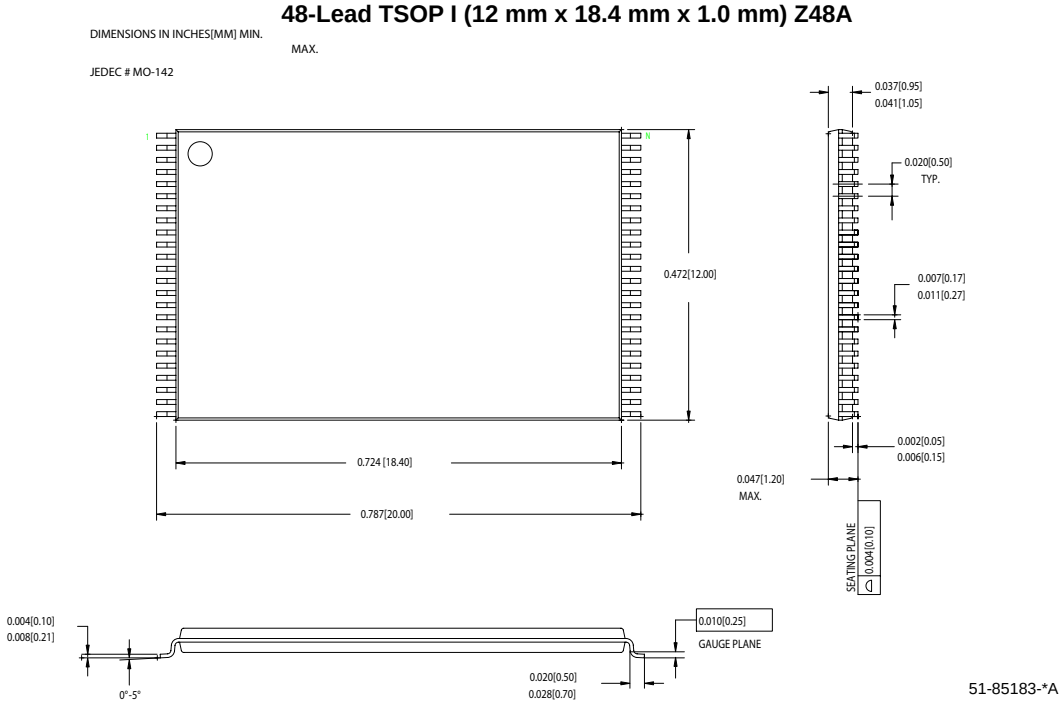


51-85178-**

Shaded areas contain advance information. Please contact your local Cypress sales representative for availability of these parts.

Package Diagrams

48-Lead TSOP I (12 mm x 18.4 mm x 1.0 mm) Z48A



Document History Page

Document Title:CY62167DV30 MoBL® 16-Mbit (1M x 16) Static RAM Document Number: 38-05328				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	118408	09/30/02	GUG	New Data Sheet
*A	123692	02/11/03	DPM	Changed Advanced to Preliminary Added package diagram
*B	126555	04/25/03	DPM	Minor change: Changed Sunset Owner from DPM to HRT
*C	127841	09/10/03	XRJ	Added 48 TSOP I package
*D	205701		AJU	Changed $\overline{\text{BYTE}}$ pin usage description for 48 TSOPI package
*E	238050	See ECN	KKV/AJU	Replaced 48-lead VFBGA package diagram; Modified Package Name in Ordering Information table from BV48A to BV48B
*F	304054	See ECN	PCI	Added 45-ns Speed Bin in AC, DC and Ordering Information tables Added Footnote #12 on page #4 Added Pb-Free packages on page # 10