8-Mbit (512K x 16) MoBL® Static RAM

Features

- **Temperature Ranges**
  - **— Industrial: –40°C to 85°C**
- **Very high speed: 55 ns**
- **Wide voltage range: 2.20V–3.60V**
- **Pin-compatible with CY62157CV25, CY62157CV30, and CY62157CV33**
- **Ultra-low active power**
  - **— Typical active current: 1.5 mA @ f = 1 MHz**
  - **— Typical active current: 12 mA @ f = f_{max}**
- **Ultra-low standby power**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in Pb-free and non Pb-free 48-ball FBGA, and Pb-free 44-pin TSOPII package**

Functional Description

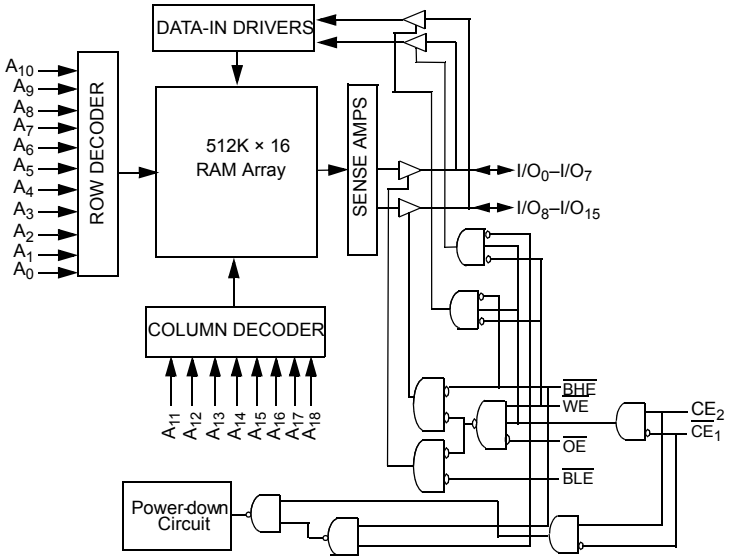
The CY62157DV30 is a high-performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones.The device also has an automatic power-down feature that significantly reduces power consumption. The device can also be put into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both BHE and BLE are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}_1$HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{18}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

Logic Block Diagram



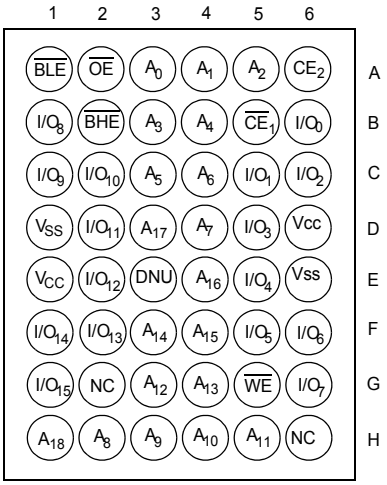
Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC}, (mA)				Standby I_{SB2}, (µA)	
						f = 1MHz		f = f_{max}			
		Min.	Typ.[1]	Max.		Typ.[1]	Max.	Typ.[1]	Max.	Typ.[1]	Max.
CY62157DV30LL	Industrial	2.2	3.0	3.6	55, 70	1.5	3	12	15	2	8

Pin Configuration[2, 3, 4]

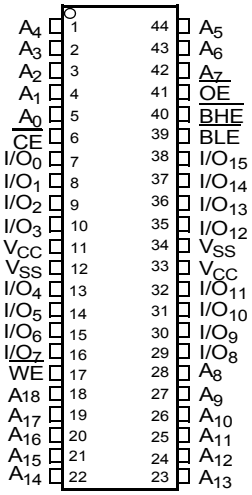
48-Ball FBGA Pinout

Top View



44-pin TSOP II Pinout

Top View



Notes:
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25°C$.
2. NC pins are not internally connected on the die.
3. DNU pins have to be left floating.
4. The 44-TSOPII package device has only one chip enable pin ($\overline{CE}$).

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .....–65°C to + 150°C

Ambient Temperature with Power Applied.....–55°C to + 125°C

Supply Voltage to Ground Potential .....–0.3V to $V_{CC(max)}$ + 0.3V

DC Voltage Applied to Outputs in High-Z State[5, 6].....–0.3V to $V_{CC(max)}$ + 0.3V

DC Input Voltage[5, 6] .....–0.3V to $V_{CC(max)}$ + 0.3V

Output Current into Outputs (LOW).....20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current.....>200 mA

Operating Range

Device	Range	Ambient Temperature (T_A)	V_{CC}[7]
CY62157DV30LL	Industrial	–40°C to +85°C	2.20V to 3.60V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			-55, -70 Min.	-55, -70 Typ.[1]	-55, -70 Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	V_{CC} = 2.20V		2.0			V
		I_{OH} = –1.0 mA	V_{CC} = 2.70V		2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	V_{CC} = 2.20V				0.4	V
		I_{OL} = 2.1 mA	V_{CC} = 2.70V				0.4	V
V_{IH}	Input HIGH Voltage	V_{CC} = 2.2V to 2.7V			1.8		V_{CC} + 0.3	V
		V_{CC}= 2.7V to 3.6V			2.2		V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage	V_{CC} = 2.2V to 2.7V			–0.3		0.6	V
		V_{CC}= 2.7V to 3.6V			–0.3		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	Ind'l		–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	Ind'l		–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = 1/t_{RC}	V_{CC} = V_{CCmax} I_{OUT} = 0 mA CMOS levels	LL		12	15	mA
		f = 1 MHz		LL		1.5	3	mA
I_{SB1}	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE_1}$ ≥ V_{CC} – 0.2V, CE_2 ≤ 0.2V V_{IN} ≥ V_{CC} – 0.2V, V_{IN} ≤ 0.2V) f = f_{MAX} (Address and Data Only), f = 0 (OE, WE, BHE and BLE), V_{CC} = 3.60V	Ind'l	LL		2	8	µA
I_{SB2}	Automatic CE Power-Down Current -CMOS Inputs	$\overline{CE_1}$ ≥ V_{CC}– 0.2V or CE_2 ≤ 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = 3.60V	Ind'l	LL		2	8	µA

Capacitance[8, 9]

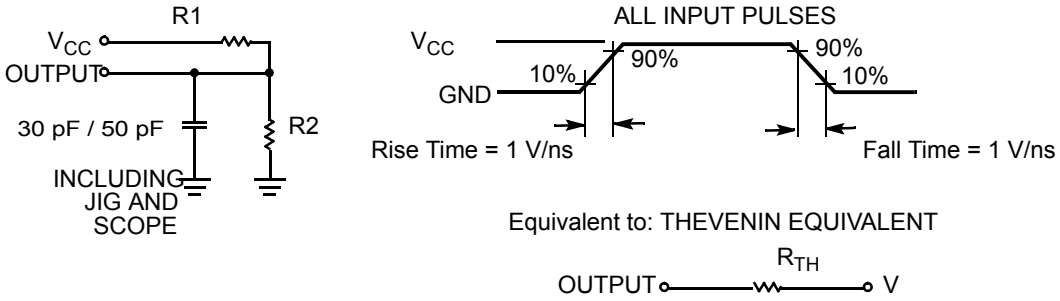
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
5. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
6. $V_{IH(max)}$= V_{CC}+0.75V for pulse duration less than 20 ns.
7. Full device AC operation assumes a 100 µs ramp time from 0 to V_{CC}(min) and 200 µs wait time after V_{CC} stabilization.
8. Tested initially and after any design or process changes that may affect these parameters.
9. The input capacitance on the CE_2 pin of the FBGA package and on the BHE pin of the 44TSOPII package is 15 pF.

Thermal Resistance[8]

Parameter	Description	Test Conditions	FBGA	TSOP II	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	39.3	35.62	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		9.69	9.13	°C/W

AC Test Loads and Waveforms

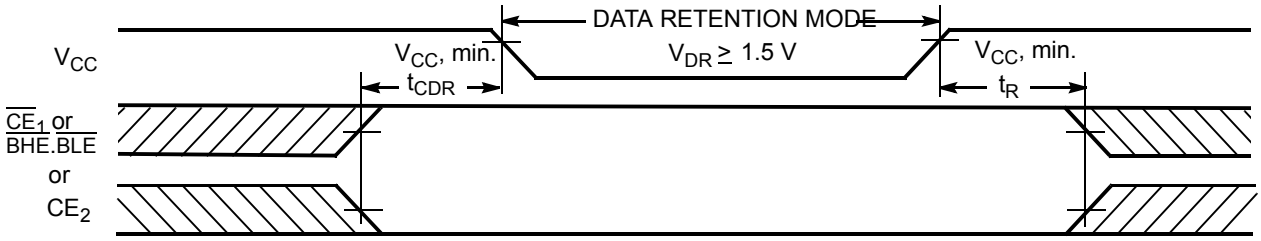


Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			1.5			V
I_{CCDR}	Data Retention Current	V_{CC}= 1.5V $\overline{CE_1} \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	Ind'l			4	µA
t_{CDR}[8]	Chip Deselect to Data Retention Time			0			ns
t_R[10]	Operation Recovery Time			t_{RC}			ns

Data Retention Waveform[11]



Notes:
10. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.

Switching Characteristics Over the Operating Range [12]

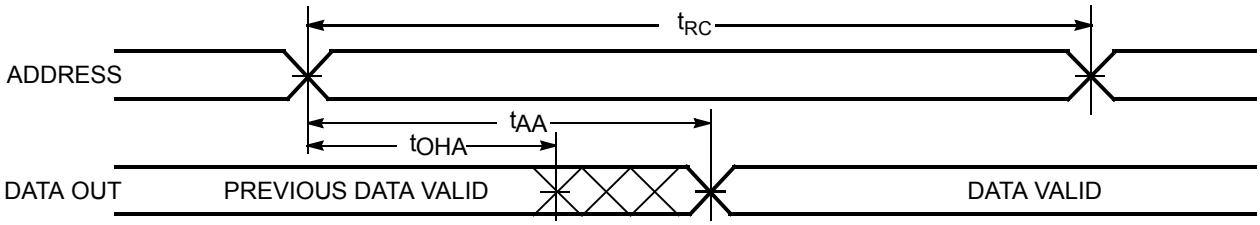
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Data Valid		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[13]	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[13, 14]		20		25	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[13]	10		10		ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z[13, 14]		20		25	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power-Up	0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to Power-Down		55		70	ns
t_{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		55		70	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low Z[13]	10		10		ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z[13, 14]		20		25	ns
Write Cycle[15]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Write End	40		60		ns
t_{AW}	Address Set-up to Write End	40		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	40		45		ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to Write End	40		60		ns
t_{SD}	Data Set-up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[13, 14]		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[13]	10		10		ns

Notes:

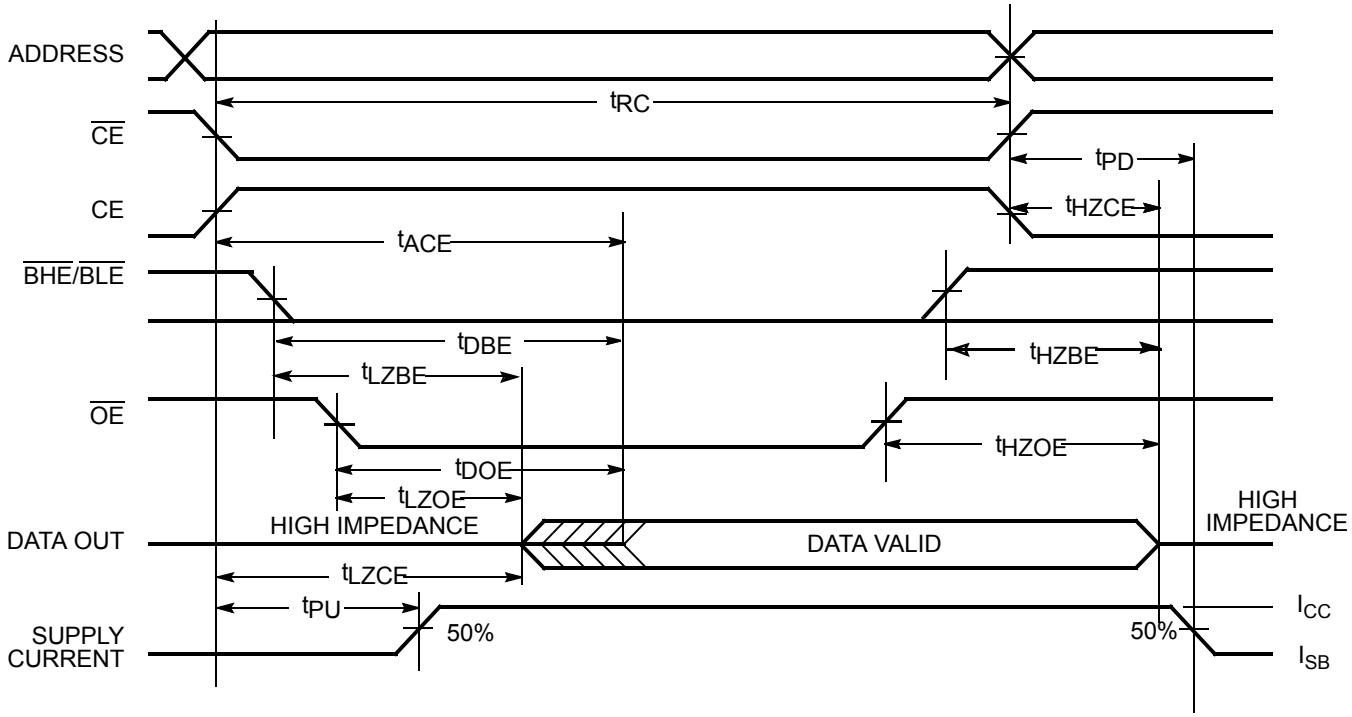
11. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.
12. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
13. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
14. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
15. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)[16, 17]



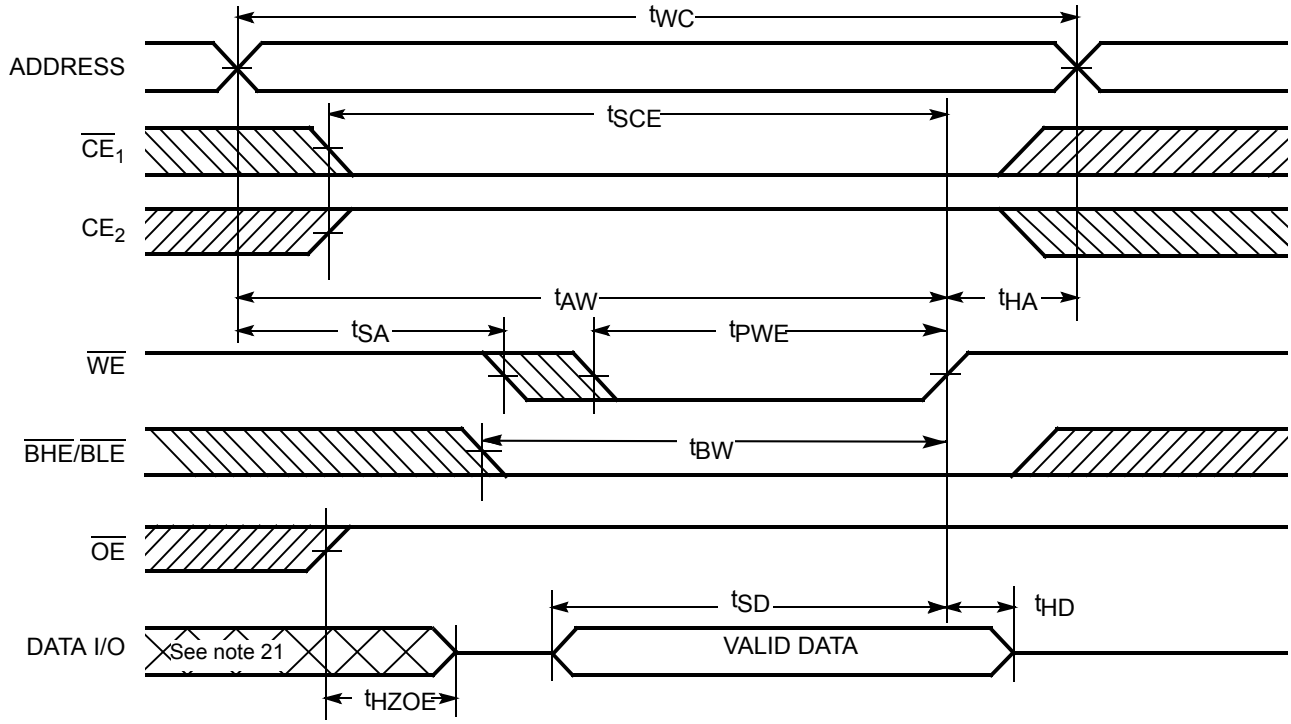
Read Cycle 2 ($\overline{OE}$ Controlled)[17, 18]



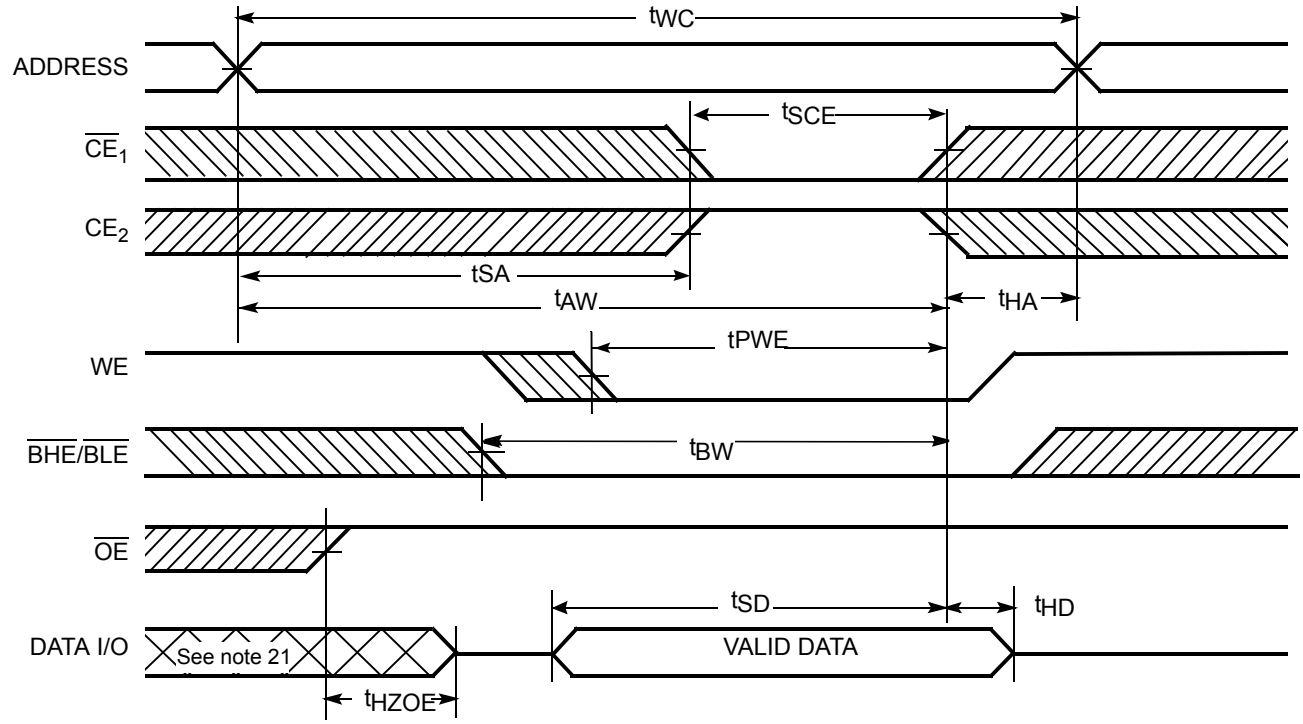
Notes:
16. The device is continuously selected. OE, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}, and CE_2 = V_{IH}.
17. $\overline{WE}$ is HIGH for read cycle.
18. Address valid prior to or coincident with $\overline{CE}_1$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Write Cycle 1 ($\overline{WE}$ Controlled)[15, 19, 20, 21]



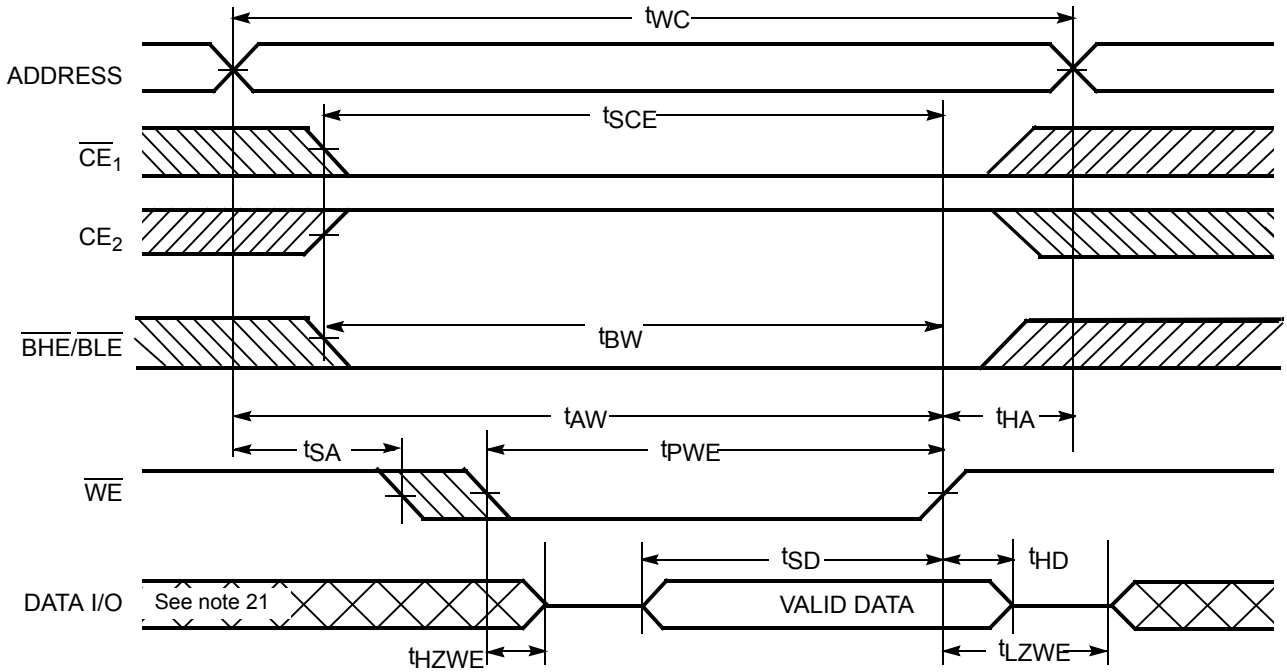
Write Cycle 2 ($\overline{CE_1}$ or CE_2 Controlled)[15, 19, 20, 21]



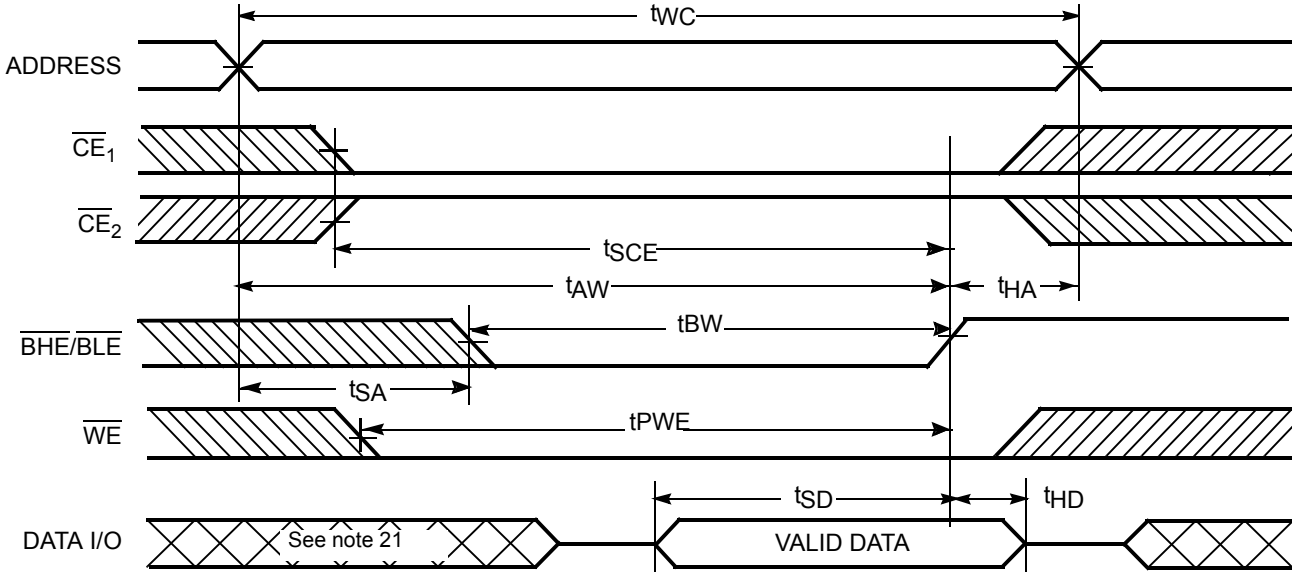
Notes:
19. Data I/O is high-impedance if $\overline{OE}$ = V_{IH}.
20. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high-impedance state.
21. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle 3 (WE Controlled, OE LOW)[20, 21]



Write Cycle 4 (BHE/BLE Controlled, OE LOW)[20, 21]



Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read (Upper byte and Lower Byte)	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Read (Lower Byte only)	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O_0–I/O_7); Data Out (I/O_8–I/O_{15})	Read (Upper Byte only)	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write (Upper byte and Lower Byte)	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Write (Lower Byte only)	Active (I_{CC})
L	H	L	X	L	H	High Z (I/O_0–I/O_7); Data In (I/O_8–I/O_{15})	Write (Upper Byte only)	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62157DV30LL-55BVI	51-85150	48-ball (6 x 8 x 1 mm) FBGA	Industrial
	CY62157DV30LL-55BVXI		48-ball (6 x 8 x 1 mm) FBGA (Pb-free)	
	CY62157DV30LL-55ZSXI	51-85087	44-pin TSOP II (Pb-free)	
70	CY62157DV30LL-70BVXI	51-85150	48-ball (6 x 8 x 1 mm) FBGA (Pb-free)	Industrial

Package Diagrams (continued)

Figure 1. 48-Pin VFBGA (51-85150)

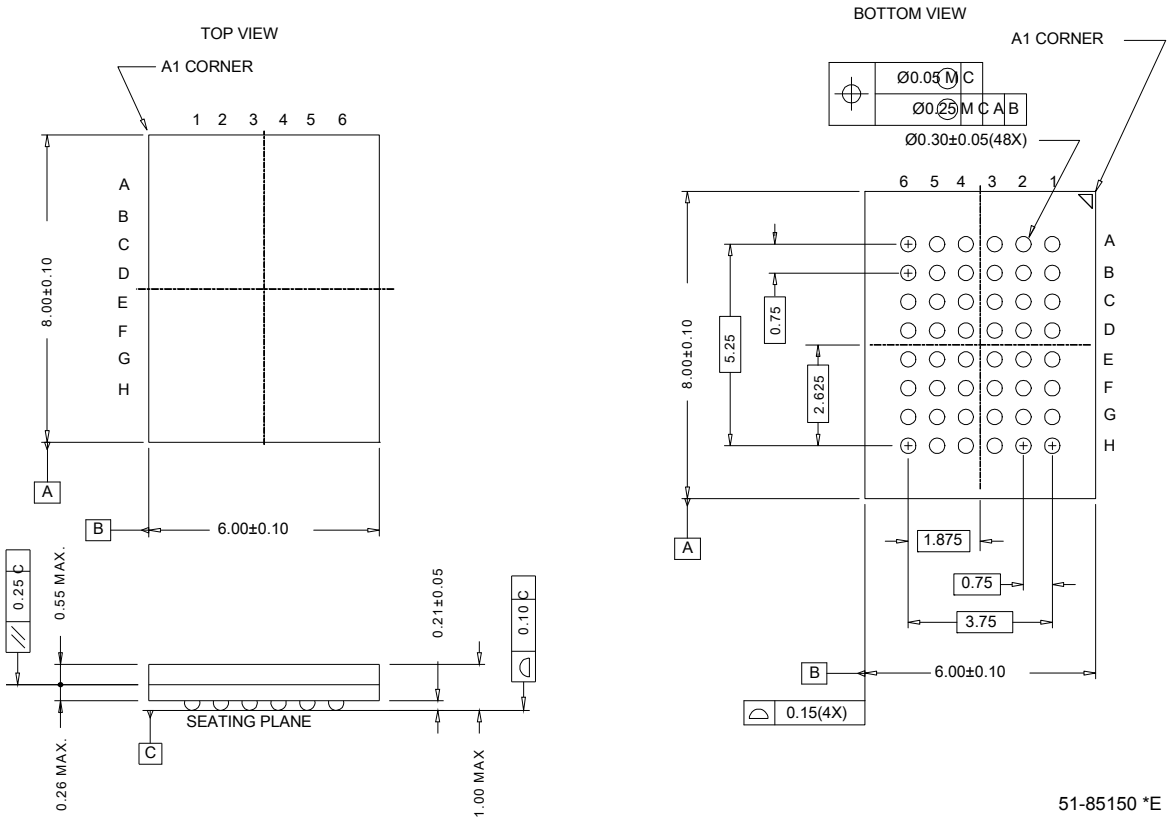
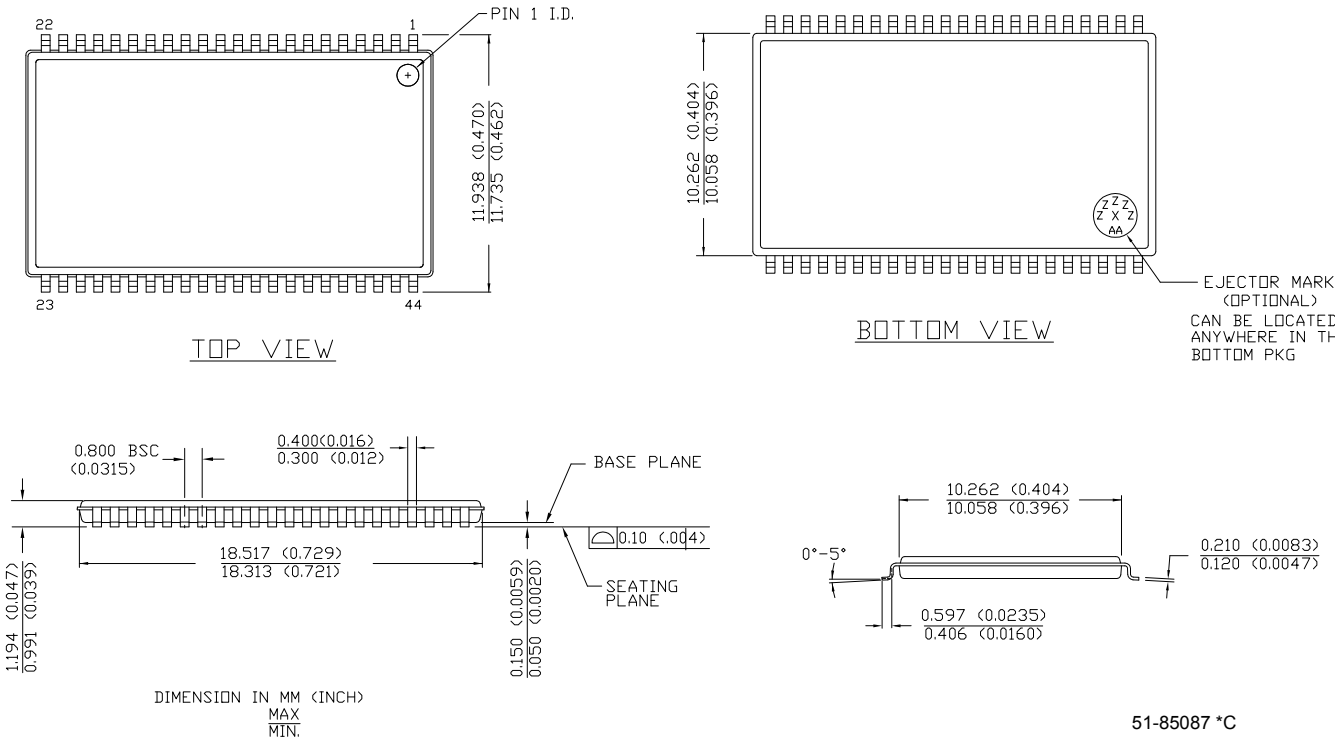


Figure 2. 44-pin TSOP II (51-85087)



Document History Page

Document Title: CY62157DV30 MoBL® 8-Mbit (512K x 16) MoBL® Static RAM Document Number: 38-05392				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	126316	05/22/03	HRT	New Data Sheet
*A	131013	11/19/03	CBD/LDZ	Change from Advance to Preliminary
*B	133115	01/24/04	CBD	Minor Change: Change MPN and upload.
*C	211601	See ECN	AJU	Change from Preliminary to Final Changed Marketing part number from CY62157DV to CY62157DV30 in the title and in the Ordering Information table Added footnotes 4, 5 and 11 Modified footnote 8 to include ramp time and wait time Removed MAX value for VDR on Data Retention Characteristics table Changed ordering code for Pb-free parts Modified voltage limits in Maximum Ratings section
*D	236628	See ECN	SYT/AJU	Added 45-ns and 70-ns Speed Bins Added Automotive product information
*E	257349	See ECN	PCI	Added test condition for 45 ns part (footnote #13 on page 4)
*F	372074	See ECN	SYT	Added Pb-Free Automotive Part in the Ordering Information Removed ‘Preliminary’ tag from Automotive Information
*G	433838	See ECN	ZSD	Changed the address of Cypress Semiconductor Corporation on Page #1 from “3901 North First Street” to “198 Champion Court” Updated the thermal resistance table Updated the ordering information table and changed the package name column to package diagram
*H	488954	See ECN	VKN	Added Automotive-A product Updated ordering Information table
*I	2897932	03/23/2010	VKN	Removed 45ns speed bin Removed Auto-A/Auto-E information Removed 48-Pin TSOP I information Updated ordering Information table Updated package diagrams.