

# 8-Mbit (512K x 16) MoBL<sup>®</sup> Static RAM

## Features

- **Temperature Ranges**
  - Industrial:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
  - Automotive-A:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
  - Automotive-E:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- **Very high speed: 45 ns**
- **Wide voltage range: 2.20V–3.60V**
- **Pin-compatible with CY62157CV25, CY62157CV30, and CY62157CV33**
- **Ultra-low active power**
  - Typical active current: 1.5 mA @  $f = 1\text{ MHz}$
  - Typical active current: 12 mA @  $f = f_{\text{max}}$
- **Ultra-low standby power**
- **Easy memory expansion with  $\overline{\text{CE}}_1$ ,  $\text{CE}_2$ , and  $\overline{\text{OE}}$  features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in Pb-free and non Pb-free 48-ball FBGA, 44-pin TSOPII, and Pb-free 48-pin TSOP1**

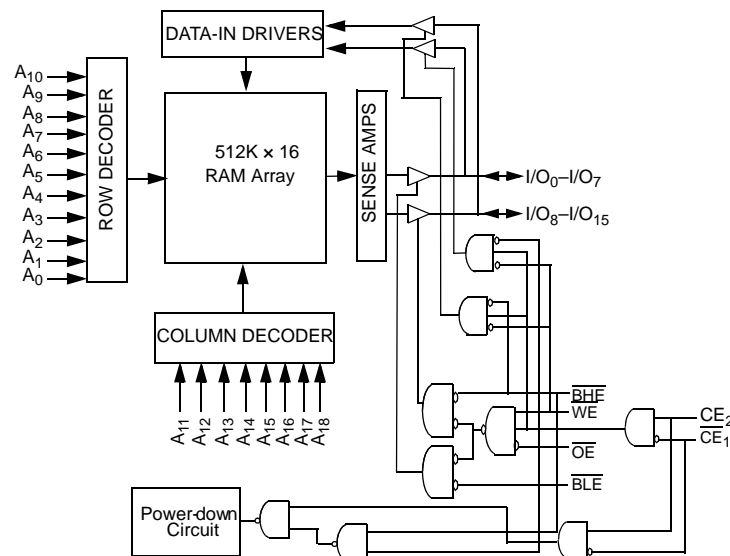
## Functional Description<sup>[1]</sup>

The CY62157DV30 is a high-performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. The device can also be put into standby mode when deselected ( $\overline{\text{CE}}_1$  HIGH or  $\text{CE}_2$  LOW or both BHE and BLE are HIGH). The input/output pins ( $\text{I/O}_0$  through  $\text{I/O}_{15}$ ) are placed in a high-impedance state when: deselected ( $\overline{\text{CE}}_1$  HIGH or  $\text{CE}_2$  LOW), outputs are disabled ( $\overline{\text{OE}}$  HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or during a write operation ( $\overline{\text{CE}}_1$  LOW,  $\text{CE}_2$  HIGH and WE LOW).

Writing to the device is accomplished by taking Chip Enables ( $\overline{\text{CE}}_1$  LOW and  $\text{CE}_2$  HIGH) and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ), is written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{18}$ ). If Byte High Enable (BHE) is LOW, then data from I/O pins ( $\text{I/O}_8$  through  $\text{I/O}_{15}$ ) is written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{18}$ ).

Reading from the device is accomplished by taking Chip Enables ( $\overline{\text{CE}}_1$  LOW and  $\text{CE}_2$  HIGH) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on  $\text{I/O}_0$  to  $\text{I/O}_7$ . If Byte High Enable (BHE) is LOW, then data from memory will appear on  $\text{I/O}_8$  to  $\text{I/O}_{15}$ . See the truth table for a complete description of read and write modes.

## Logic Block Diagram



### Note:

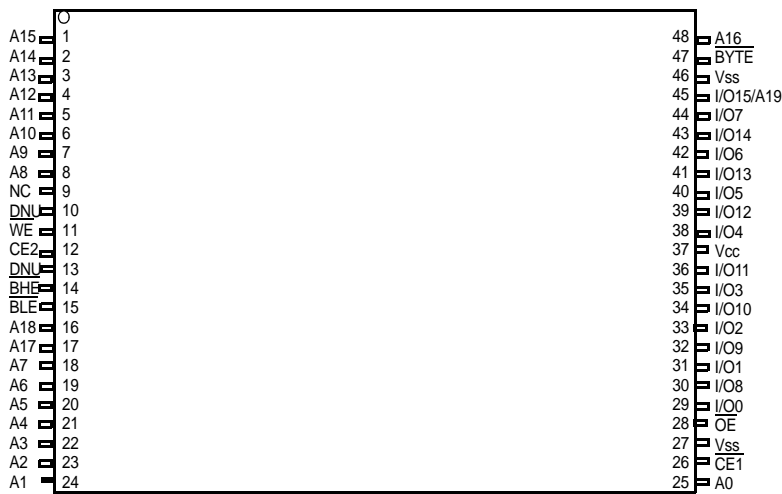
1. For best practice recommendations, please refer to the Cypress application note entitled *System Design Guidelines*, which is available at <http://www.cypress.com>.

Product Portfolio

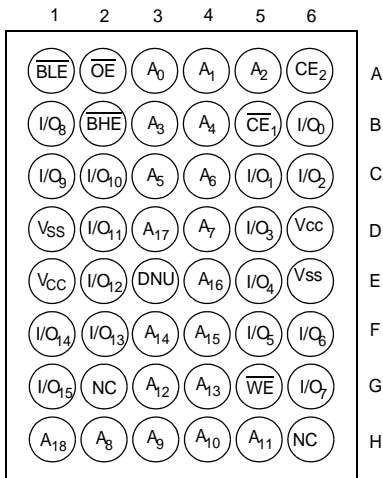
Product	Range	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
						Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
		Min.	Typ. <sup>[2]</sup>	Max.		f = 1MHz		f = f <sub>max</sub>			
						Typ. <sup>[2]</sup>	Max.	Typ. <sup>[2]</sup>	Max.	Typ. <sup>[2]</sup>	Max.
CY62157DV30L	Industrial	2.2	3.0	3.6	45, 55, 70	1.5	3	12	20	2	20
CY62157DV30LL	Industrial	2.2	3.0	3.6	45, 55, 70	1.5	3	12	15	2	8
CY62157DV30LL	Automotive-A	2.2	3.0	3.6	55	1.5	3	12	15	2	8
CY62157DV30L	Automotive-E	2.2	3.0	3.6	55	1.5	3	12	20	2	50

Pin Configuration<sup>[4, 5, 6]</sup>

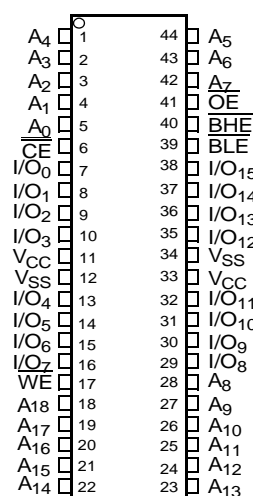
48-Pin TSOP I Pinout  
Top View



48-Ball FBGA Pinout  
Top View



44-pin TSOP II Pinout  
Top View



Notes:

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.
- NC pins are not internally connected on the die.
- DNU pins have to be left floating.
- The BYTE pin in the 48-TSOP I package has to be tied HIGH to use the device as a 512K x 16 SRAM. The 48-TSOP I package can also be used as a 1M x 8 SRAM by tying the BYTE signal LOW. For 1M x 8 Functionality, please refer to the CY62158DV30 datasheet. In the 1M x 8 configuration, Pin 45 is A19, while BHE, BLE and I/O8 to I/O14 pins are not used.
- The 44-TSOP II package device has only one chip enable pin (CE).

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to + 150°C
Ambient Temperature with Power Applied.....	-55°C to + 125°C
Supply Voltage to Ground Potential .....	-0.3V to $V_{CC(max)}$ + 0.3V
DC Voltage Applied to Outputs in High-Z State <sup>[8, 9]</sup> .....	-0.3V to $V_{CC(max)}$ + 0.3V
DC Input Voltage <sup>[8, 9]</sup> .....	-0.3V to $V_{CC(max)}$ + 0.3V
Output Current into Outputs (LOW) .....	20 mA

Static Discharge Voltage..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-up Current..... >200 mA

### Operating Range

Device	Range	Ambient Temperature (T <sub>A</sub> )	V <sub>CC</sub> <sup>[10]</sup>
CY62157DV30L	Industrial	-40°C to +85°C	2.20V to 3.60V
CY62157DV30LL			
CY62157DV30LL	Automotive-A	-40°C to +85°C	
CY62157DV30L	Automotive-E	-40°C to +125°C	

### Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-45, -55, -70			Unit	
			Min.	Typ. <sup>[2]</sup>	Max.		
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> = 2.20V	2.0		V	
		I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 2.70V	2.4		V	
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA	V <sub>CC</sub> = 2.20V		0.4	V	
		I <sub>OL</sub> = 2.1 mA	V <sub>CC</sub> = 2.70V		0.4	V	
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 2.2V to 2.7V		1.8	V <sub>CC</sub> + 0.3	V	
		V <sub>CC</sub> = 2.7V to 3.6V		2.2	V <sub>CC</sub> + 0.3	V	
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> = 2.2V to 2.7V		-0.3	0.6	V	
		V <sub>CC</sub> = 2.7V to 3.6V		-0.3	0.8	V	
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	Ind'l/Auto-A <sup>[7]</sup>	-1	+1	μA	
			Auto-E <sup>[7]</sup>	-4	+4	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	Ind'l/Auto-A <sup>[7]</sup>	-1	+1	μA	
			Auto-E <sup>[7]</sup>	-4	+4	μA	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = V <sub>CCmax</sub> I <sub>OUT</sub> = 0 mA CMOS levels	L	12	20	mA
				LL	12	15	mA
		f = 1 MHz		L	1.5	3	mA
				LL	1.5	3	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current — CMOS Inputs	CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2V, CE <sub>2</sub> ≤ 0.2V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≤ 0.2V f = f <sub>MAX</sub> (Address and Data Only), f = 0 (OE, WE, BHE and BLE), V <sub>CC</sub> = 3.60V	Ind'l	L	2	20	μA
			Ind'l/Auto-A <sup>[7]</sup>	LL	2	8	
			Auto-E <sup>[7]</sup>	L		50	
I <sub>SB2</sub>	Automatic CE Power-Down Current -CMOS Inputs	CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2V or CE <sub>2</sub> ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.60V	Ind'l <sup>[7]</sup>	L	2	20	μA
			Ind'l/Auto-A <sup>[7]</sup>	LL	2	8	
			Auto-E <sup>[7]</sup>	L		50	

### Capacitance<sup>[11, 12]</sup>

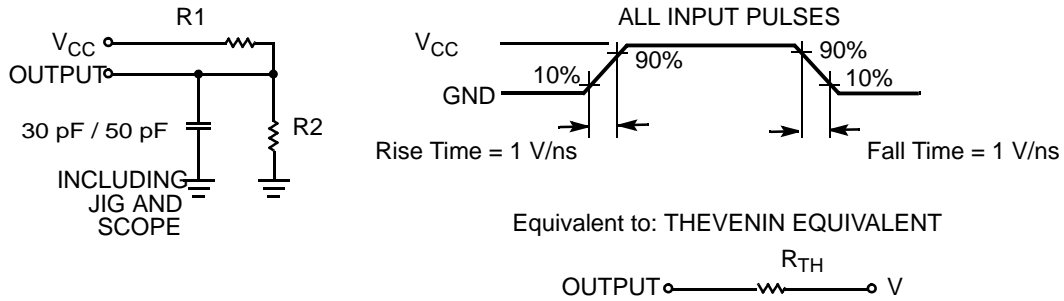
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz,	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = V <sub>CC(typ)</sub>	10	pF

#### Notes:

7. Automotive-A and Automotive-E available only in -55.
8. V<sub>IL(min.)</sub> = -2.0V for pulse durations less than 20 ns.
9. V<sub>IH(max.)</sub> = V<sub>CC</sub> + 0.75V for pulse duration less than 20 ns.
10. Full device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC(min)</sub> and 200 μs wait time after V<sub>CC</sub> stabilization.
11. Tested initially and after any design or process changes that may affect these parameters.
12. The input capacitance on the CE<sub>2</sub> pin of the FBGA and 48TSOPI packages and on the BHE pin of the 44TSOPII package is 15 pF.

**Thermal Resistance<sup>[11]</sup>**

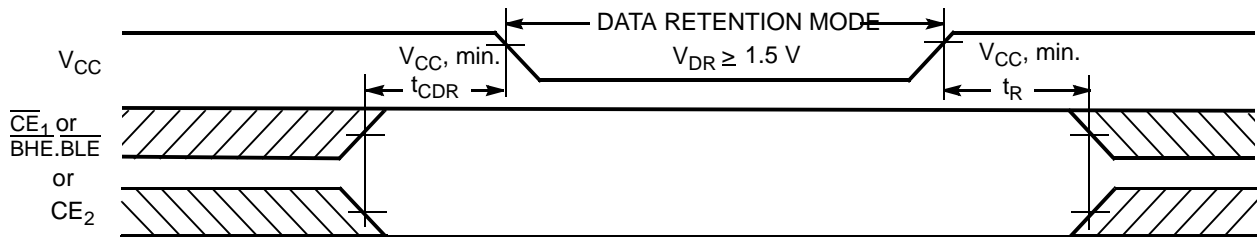
Parameter	Description	Test Conditions	FBGA	TSOP II	TSOP I	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, four-layer printed circuit board	39.3	35.62	36.9	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		9.69	9.13	10.05	°C/W

**AC Test Loads and Waveforms<sup>[13]</sup>**


Parameters	2.50V	3.0V	Unit
R1	16667	1103	$\Omega$
R2	15385	1554	$\Omega$
$R_{TH}$	8000	645	$\Omega$
$V_{TH}$	1.20	1.75	V

**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions	Min.	Typ. <sup>[2]</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		1.5			V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 1.5V$ $CE_1 \geq V_{CC} - 0.2V, CE_2 \leq 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	Ind'I (L)		10	$\mu A$
			Ind'I/Auto-A (LL)		4	
			Auto-E (L)		25	
$t_{CDR}^{[11]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[14]}$	Operation Recovery Time		$t_{RC}$			ns

**Data Retention Waveform<sup>[15]</sup>**

**Notes:**

13. Test condition for the 45 ns part is a load capacitance of 30 pF.

14. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 100 \mu s$  or stable at  $V_{CC(min.)} \geq 100 \mu s$ .

**Switching Characteristics** Over the Operating Range <sup>[16]</sup>

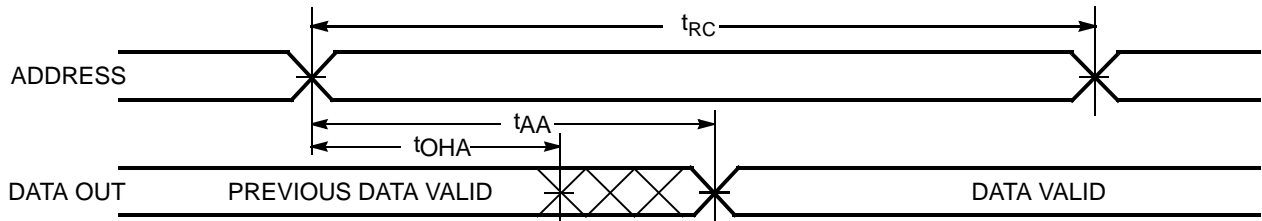
Parameter	Description	45 ns <sup>[13]</sup>		55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>								
t <sub>RC</sub>	Read Cycle Time	45		55		70		ns
t <sub>AA</sub>	Address to Data Valid		45		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		10		ns
t <sub>ACE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Data Valid		45		55		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		25		25		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[17]</sup>	5		5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[17, 18]</sup>		15		20		25	ns
t <sub>LZCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Low Z <sup>[17]</sup>	10		10		10		ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to High Z <sup>[17, 18]</sup>		20		20		25	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Power-Up	0		0		0		ns
t <sub>PD</sub>	$\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to Power-Down		45		55		70	ns
t <sub>DBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		45		55		70	ns
t <sub>LZBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Low Z <sup>[17]</sup>	10		10		10		ns
t <sub>HZBE</sub>	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z <sup>[17, 18]</sup>		15		20		25	ns
<b>Write Cycle<sup>[19]</sup></b>								
t <sub>WC</sub>	Write Cycle Time	45		55		70		ns
t <sub>SCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Write End	40		40		60		ns
t <sub>AW</sub>	Address Set-up to Write End	40		40		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		ns
t <sub>SA</sub>	Address Set-up to Write Start	0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	35		40		45		ns
t <sub>BW</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Write End	40		40		60		ns
t <sub>SD</sub>	Data Set-up to Write End	25		25		30		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High-Z <sup>[17, 18]</sup>		15		20		25	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low-Z <sup>[17]</sup>	10		10		10		ns

**Notes:**

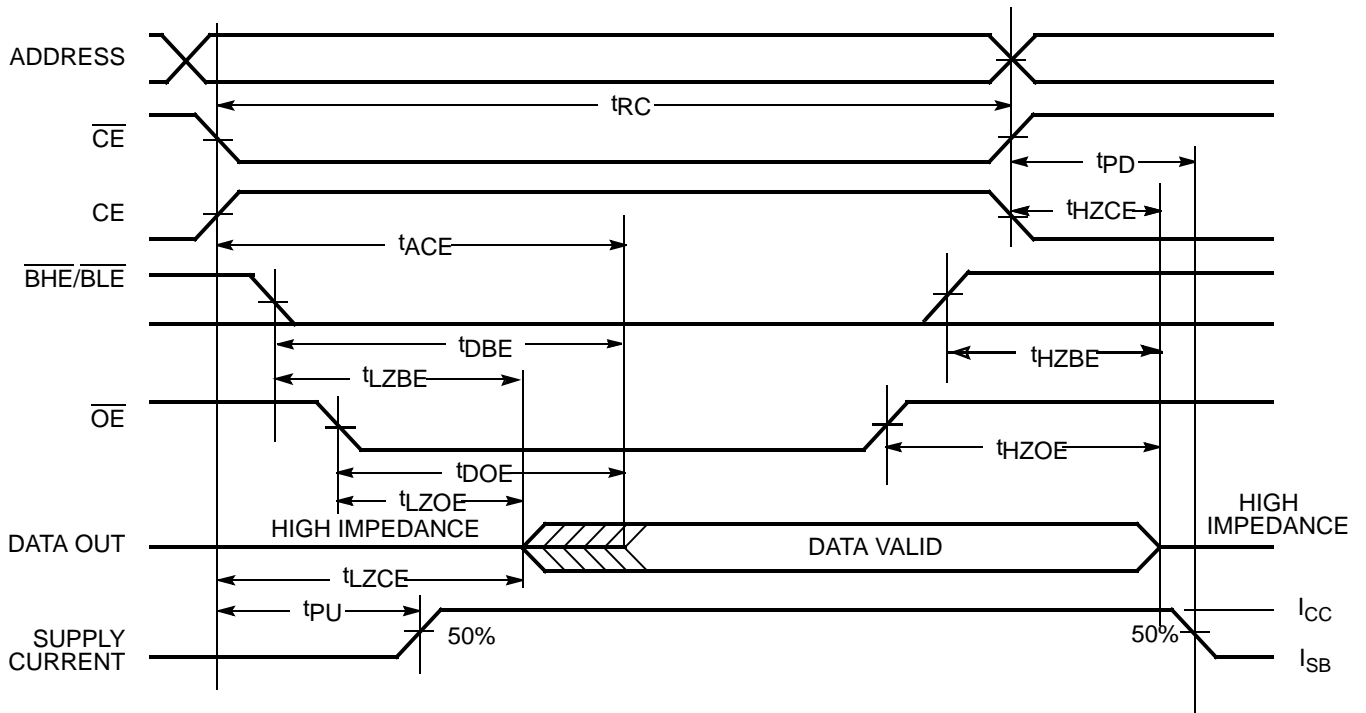
15.  $\overline{BHE}.\overline{BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Chip can be deselected by either disabling the chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .
16. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the "AC Test Loads and Waveforms" section.
17. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZBE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
18. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high-impedance state.
19. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

### Switching Waveforms

Read Cycle 1 (Address Transition Controlled)<sup>[20, 21]</sup>



Read Cycle 2 ( $\overline{OE}$  Controlled)<sup>[21, 22]</sup>



**Notes:**

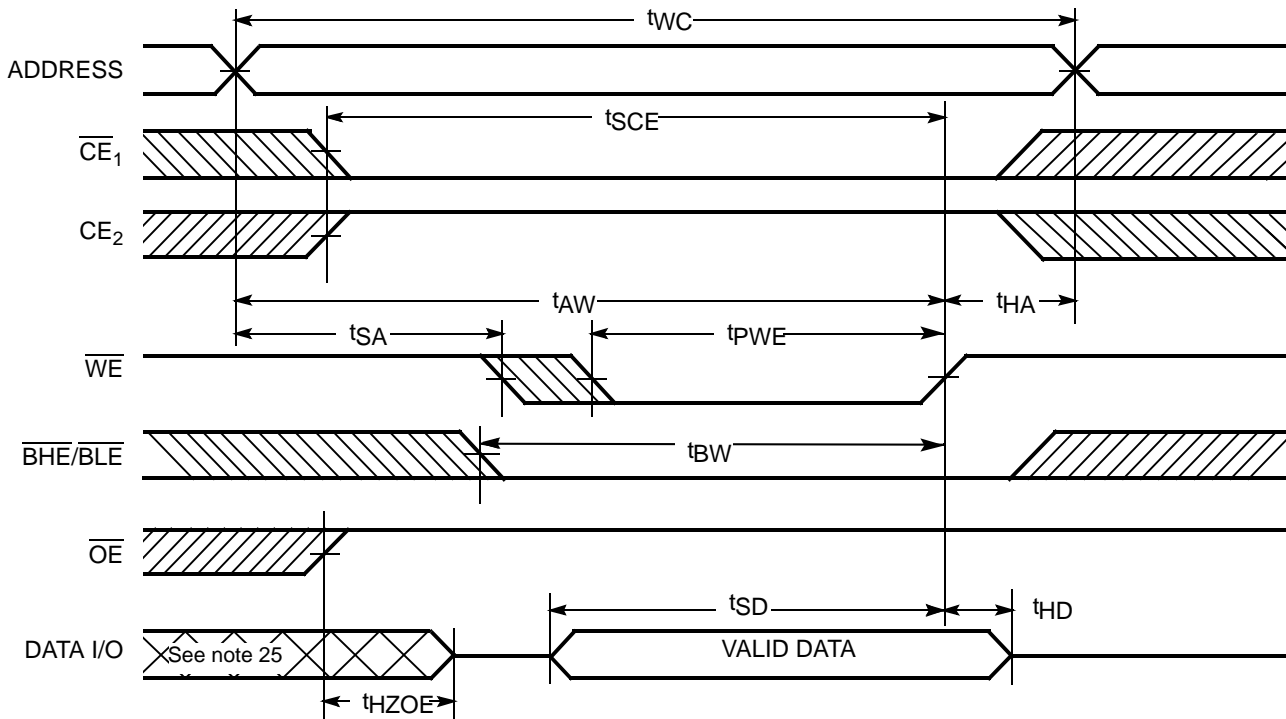
20. The device is continuously selected. OE,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $CE_2 = V_{IH}$ .

21. WE is HIGH for read cycle.

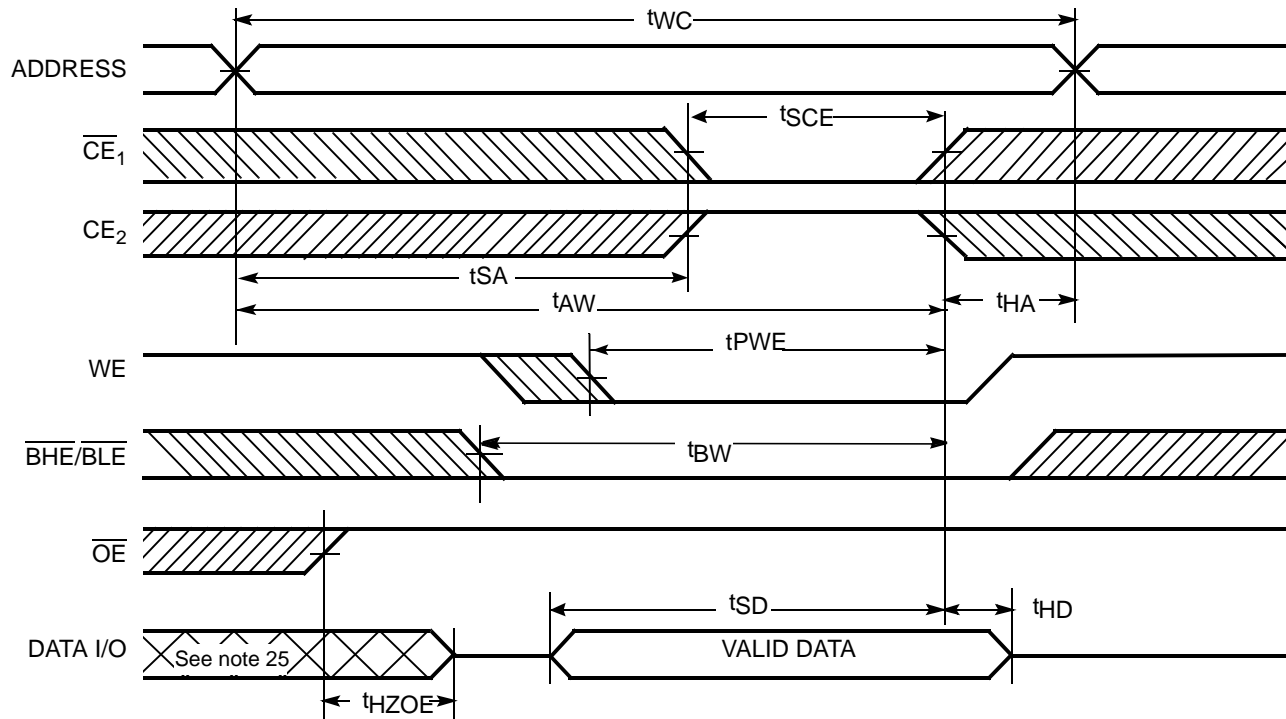
22. Address valid prior to or coincident with  $\overline{CE}_1$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW and  $CE_2$  transition HIGH.

Switching Waveforms (continued)

Write Cycle 1 ( $\overline{WE}$  Controlled)<sup>[19, 23, 24, 25]</sup>



Write Cycle 2 ( $\overline{CE}_1$  or  $\overline{CE}_2$  Controlled)<sup>[19, 23, 24, 25]</sup>

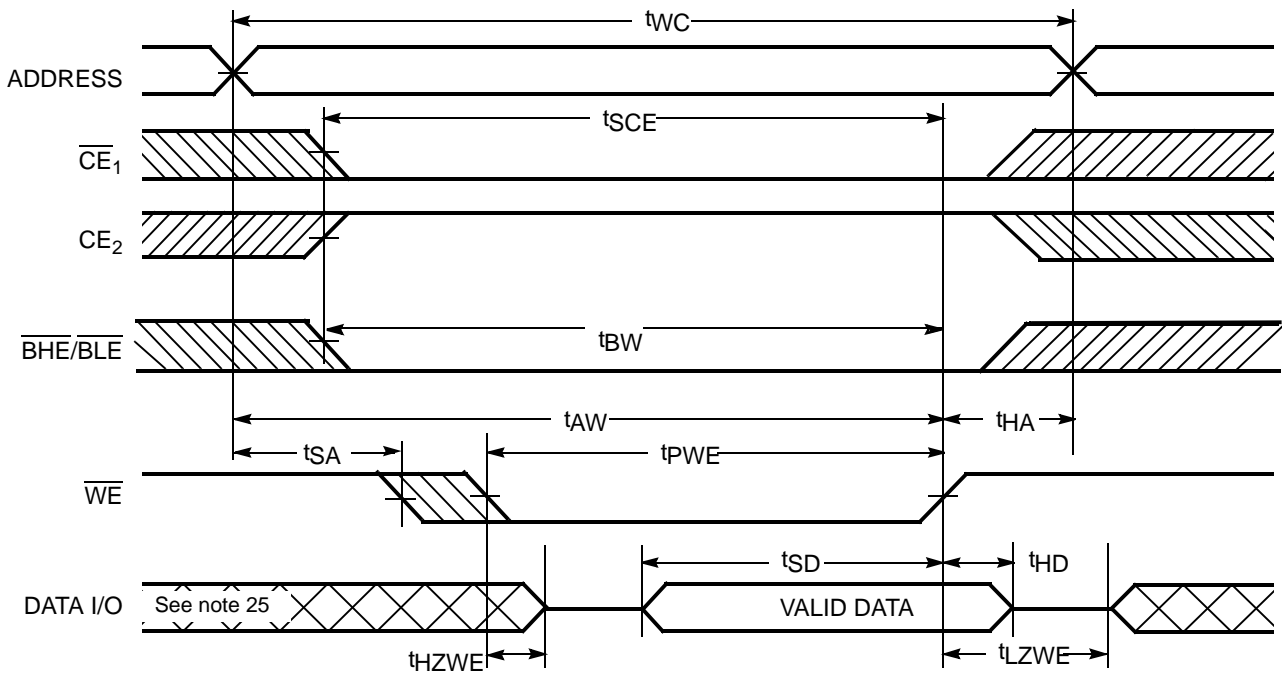


Notes:

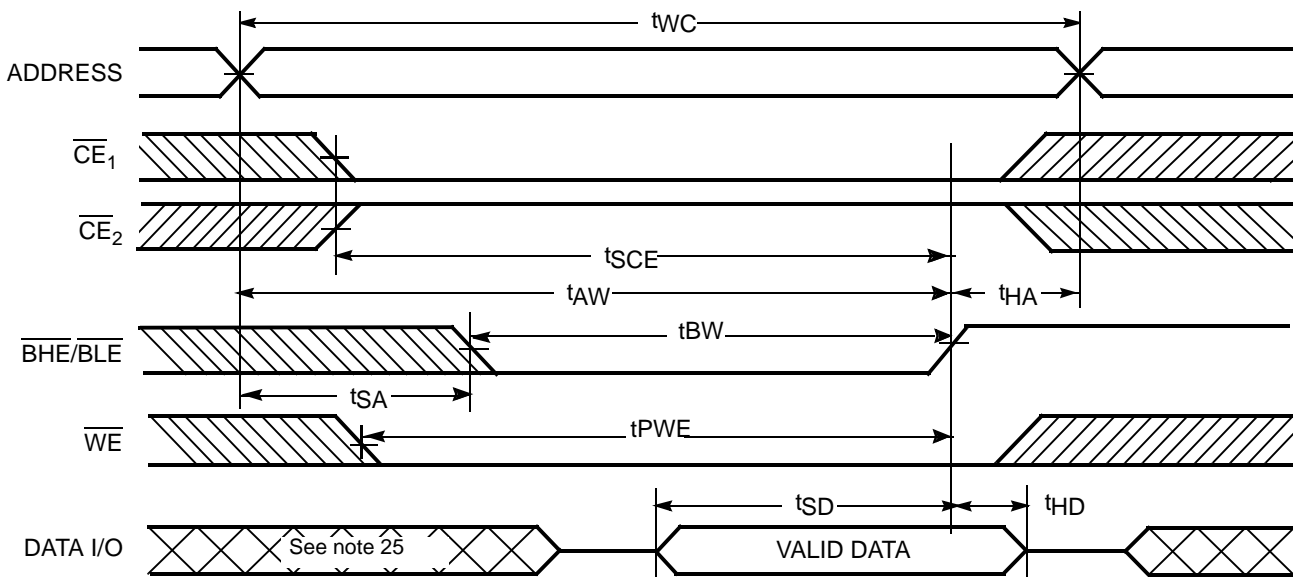
- 23. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
- 24. If  $\overline{CE}_1$  goes HIGH and  $\overline{CE}_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high-impedance state.
- 25. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[24, 25]</sup>



Write Cycle 4 ( $\overline{\text{BHE/BLE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[24, 25]</sup>





**Truth Table**

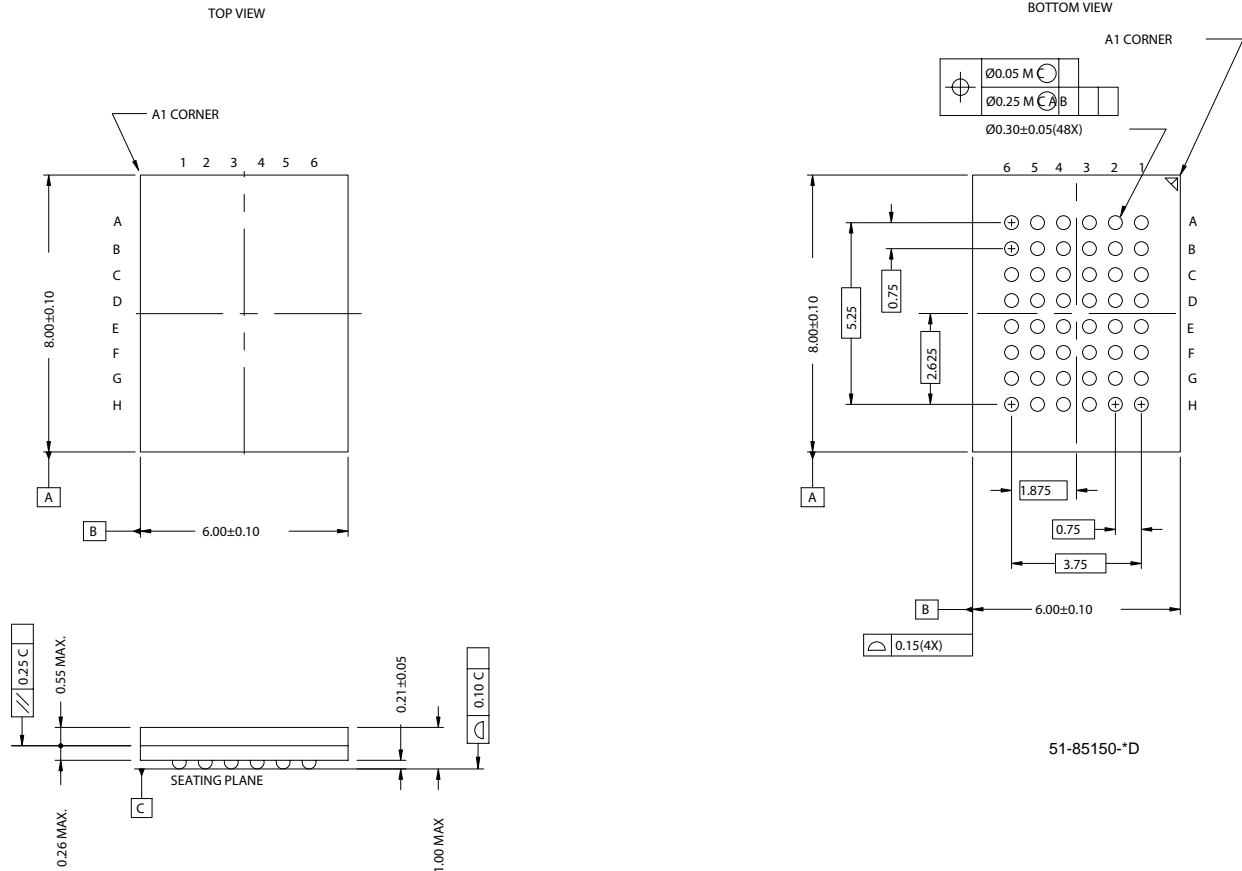
$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read (Upper byte and Lower Byte)	Active ( $I_{CC}$ )
L	H	H	L	H	L	Data Out ( $I/O_0$ – $I/O_7$ ); High Z ( $I/O_8$ – $I/O_{15}$ )	Read (Lower Byte only)	Active ( $I_{CC}$ )
L	H	H	L	L	H	High Z ( $I/O_0$ – $I/O_7$ ); Data Out ( $I/O_8$ – $I/O_{15}$ )	Read (Upper Byte only)	Active ( $I_{CC}$ )
L	H	H	H	L	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	H	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write (Upper byte and Lower Byte)	Active ( $I_{CC}$ )
L	H	L	X	H	L	Data In ( $I/O_0$ – $I/O_7$ ); High Z ( $I/O_8$ – $I/O_{15}$ )	Write (Lower Byte only)	Active ( $I_{CC}$ )
L	H	L	X	L	H	High Z ( $I/O_0$ – $I/O_7$ ); Data In ( $I/O_8$ – $I/O_{15}$ )	Write (Upper Byte only)	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62157DV30L-45BVI	51-85150	48-ball (6 x 8 x 1 mm) FBGA	Industrial
	CY62157DV30LL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	
55	CY62157DV30LL-55BVI	51-85150	48-ball (6 x 8 x 1 mm) FBGA	Industrial
	CY62157DV30L-55BVXI		48-ball (6 x 8 x 1 mm) FBGA (Pb-free)	
	CY62157DV30LL-55BVXI			
	CY62157DV30L-55ZXI	51-85183	44-pin TSOP I (Pb-free)	
	CY62157DV30LL-55ZSI	51-85087	44-pin TSOP II	
	CY62157DV30L-55ZSXI		44-pin TSOP II (Pb-free)	
	CY62157DV30LL-55ZSXI			
	CY62157DV30LL-55BVXA	51-85150	48-ball (6 x 8 x 1 mm) FBGA (Pb-free)	Automotive-A
	CY62157DV30L-55BVXE	51-85150	48-ball (6 x 8 x 1 mm) FBGA (Pb-free)	Automotive-E
CY62157DV30L-55ZSXE	51-85087	44-pin TSOP II (Pb-free)		
70	CY62157DV30LL-70BVI	51-85150	48-ball (6 x 8 x 1 mm) FBGA	Industrial
	CY62157DV30LL-70BVXI		48-ball (6 x 8 x 1 mm) FBGA (Pb-free)	

**Package Diagrams**

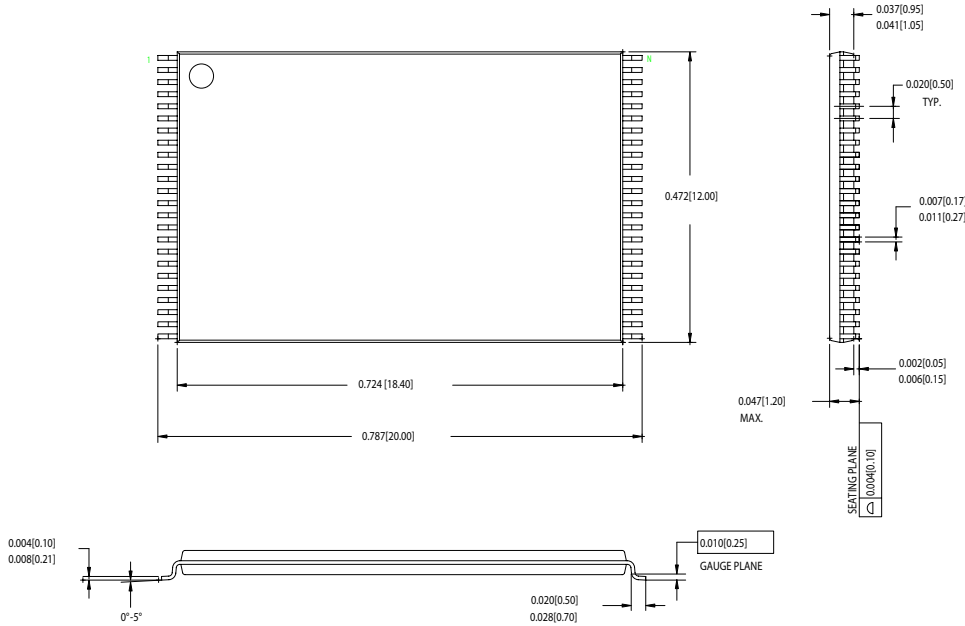
**48-ball FBGA (6 x 8 x 1 mm) (51-85150)**



Package Diagrams (continued)

48-pin TSOP I (12 mm x 18.4 mm x 1.0 mm) (51-85183)

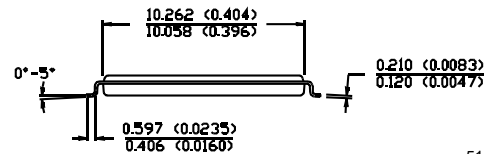
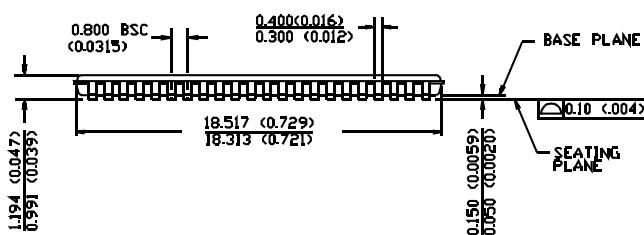
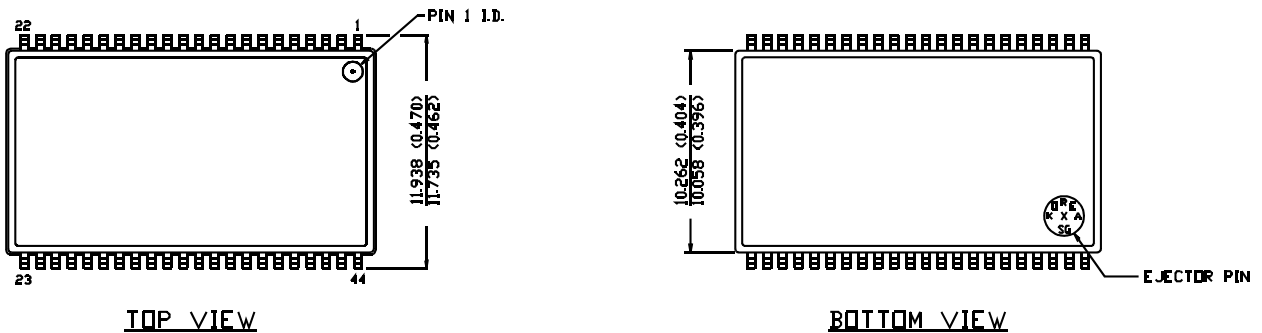
DIMENSIONS IN INCHES(MM) MIN. MAX.  
JEDEC # MO-142



51-85183-A

DIMENSION IN MM (INCH)  
MAX  
MIN

44-pin TSOP II (51-85087)



51-85087-A

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**Document History Page**

Document Title: CY62157DV30 MoBL® 8-Mbit (512K x 16) MoBL® Static RAM Document Number: 38-05392				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	126316	05/22/03	HRT	New Data Sheet
*A	131013	11/19/03	CBD/LDZ	Change from Advance to Preliminary
*B	133115	01/24/04	CBD	Minor Change: Change MPN and upload.
*C	211601	See ECN	AJU	Change from Preliminary to Final Changed Marketing part number from CY62157DV to CY62157DV30 in the title and in the Ordering Information table Added footnotes 4, 5 and 11 Modified footnote 8 to include ramp time and wait time Removed MAX value for VDR on Data Retention Characteristics table Changed ordering code for Pb-free parts Modified voltage limits in Maximum Ratings section
*D	236628	See ECN	SYT/AJU	Added 45-ns and 70-ns Speed Bins Added Automotive product information
*E	257349	See ECN	PCI	Added test condition for 45 ns part (footnote #13 on page 4)
*F	372074	See ECN	SYT	Added Pb-Free Automotive Part in the Ordering Information Removed 'Preliminary' tag from Automotive Information
*G	433838	See ECN	ZSD	Changed the address of Cypress Semiconductor Corporation on Page #1 from "3901 North First Street" to "198 Champion Court" Updated the thermal resistance table Updated the ordering information table and changed the package name column to package diagram
*H	488954	See ECN	VKN	Added Automotive-A product Updated ordering Information table