

8M (512K x 16) Static RAM

Features

- **Very high speed: 55 ns and 70 ns**
- **Voltage range: 1.65V to 1.95V**
- **Pin compatible with CY62157CV18**
- **Ultra-low active power**
 - Typical active current: 1 mA @ f = 1 MHz
 - Typical active current: 10 mA @ f = f_{MAX}
- **Ultra-low standby power**
- **Easy memory expansion with \overline{CE}_1 , \overline{CE}_2 , and \overline{OE} features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Packages offered in a 48-ball FBGA**

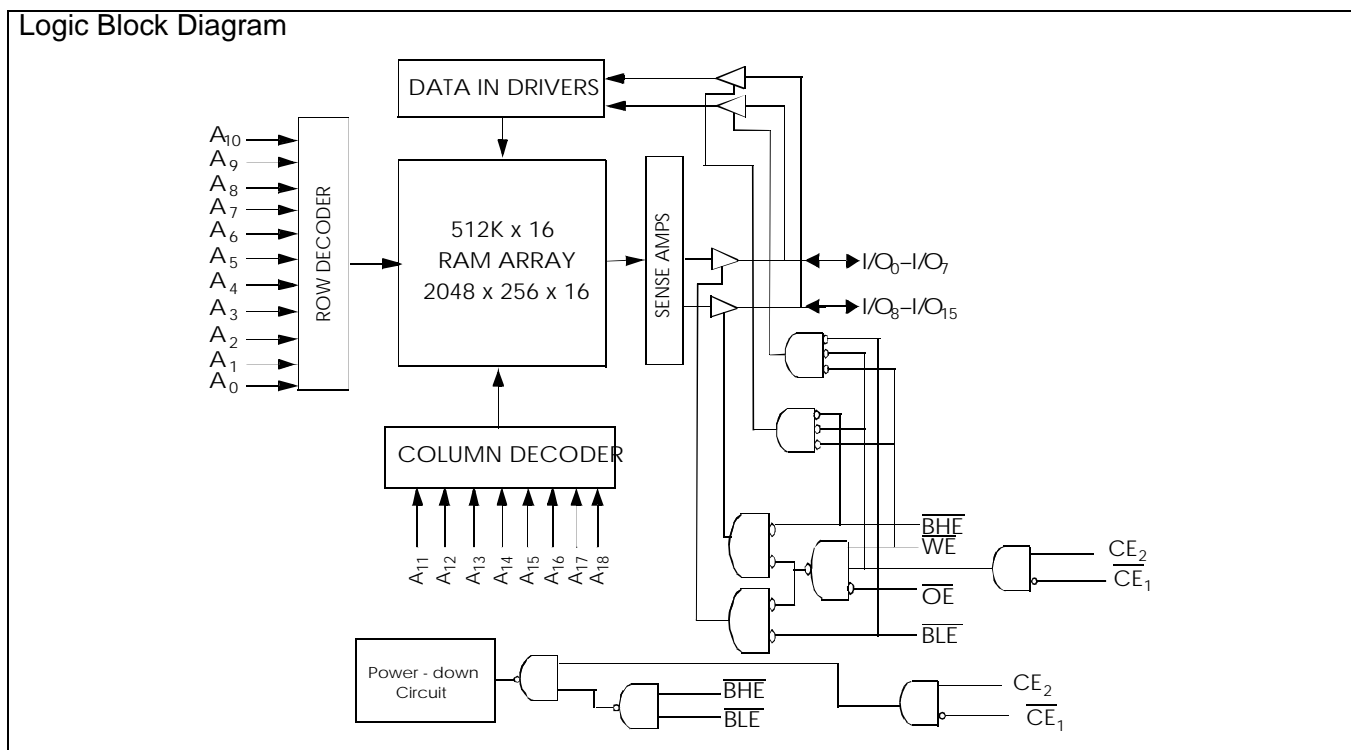
Functional Description^[1]

The CY62157DV18 is a high-performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can be put into standby mode reducing

power consumption by more than 99% when deselected Chip Enable 1 (\overline{CE}_1) HIGH or Chip Enable 2 (\overline{CE}_2) LOW or both BHE and BLE are HIGH. The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when: deselected Chip Enable 1 (\overline{CE}_1) HIGH or Chip Enable 2 (\overline{CE}_2) LOW, outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , BLE HIGH) or during a write operation (Chip Enable 1 (\overline{CE}_1) LOW and Chip Enable 2 (\overline{CE}_2) HIGH and WE LOW).

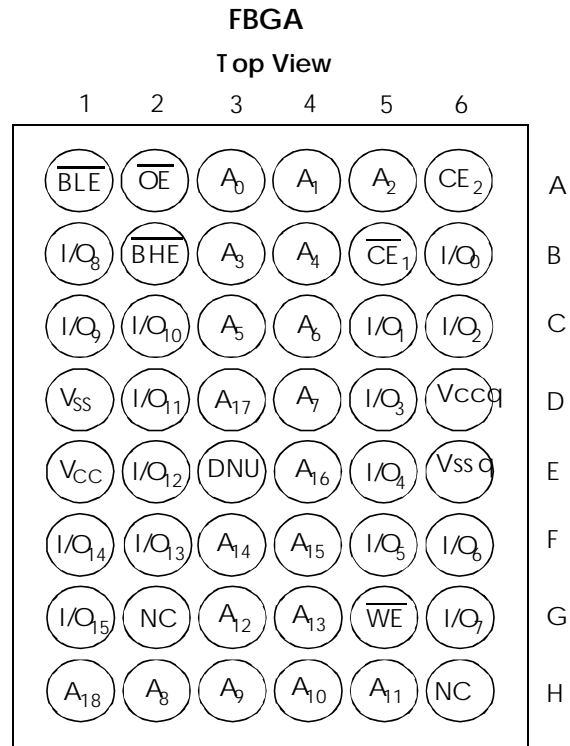
Writing to the device is accomplished by taking Chip Enable 1 (\overline{CE}_1) LOW and Chip Enable 2 (\overline{CE}_2) HIGH and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₈). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₈).

Reading from the device is accomplished by taking Chip Enable 1 (\overline{CE}_1) LOW and Chip Enable 2 (\overline{CE}_2) HIGH and Output Enable (\overline{OE}) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable (\overline{BHE}) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the truth table at the back of this data sheet for a complete description of read and write modes.



Note:

1. For best practice recommendations, please refer to the Cypress application note *System Design Guidelines* on <http://www.cypress.com>.

Pin Configuration^[2, 3]

Notes:

2. NC pins are not connected to the die.
3. DNU pins are to be connected to V_{SS} or left open.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage to Ground Potential..... -0.2V to $V_{CCMAX} + 0.2V$

DC Voltage Applied to Outputs in High-Z State^[4]..... -0.2V to $V_{CC} + 0.2V$

DC Input Voltage^[4]..... -0.2V to $V_{CC} + 0.2V$

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Industrial	-40°C to +85°C	1.65V to 1.95V

Product Portfolio

Product	V_{CC} Range(V)			Speed (ns)	Power Dissipation					
					Operating, I_{CC} (mA)				Standby, I_{SB2} (μ A)	
	f = 1 MHz		f = f_{MAX}							
	Min.	Typ. ^[5]	Max.		Typ. ^[5]	Max.	Typ. ^[5]	Max.	Typ. ^[5]	Max.
CY62157DV18L	1.65	1.8	1.95	55	1	5	10	20	2	20
				70			8	15		
CY62157DV18LL	1.65	1.8	1.95	55	1	5	10	20	2	5
				70			8	15		

DC Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	CY62157DV18-55			CY62157DV18-70			Unit	
			Min.	Typ. ^[5]	Max.	Min.	Typ. ^[5]	Max.		
V_{OH}	Output HIGH Voltage	$I_{OH} = -0.1$ mA, $V_{CC} = 1.65$ V	1.4			1.4			V	
V_{OL}	Output LOW Voltage	$I_{OL} = 0.1$ mA, $V_{CC} = 1.65$ V			0.2			0.2	V	
V_{IH}	Input HIGH Voltage		1.4		$V_{CC} + 0.2$	1.4		$V_{CC} + 0.2$	V	
V_{IL}	Input LOW Voltage		-0.2		0.4	-0.2		0.4	V	
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	-1		+1	μ A	
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	-1		+1	-1		+1	μ A	
I_{CC}	V_{CC} Operating Supply Current	f = $f_{MAX} = 1/t_{RC}$, $V_{CC} = 1.95$ V, $I_{OUT} = 0$ mA, CMOS level		10	20		8	15	mA	
		f = 1 MHz		1	5		1	5		
I_{SB1}	Automatic CE Power-down Current – CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V, $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V, f = f_{MAX} (Address and Data Only), f = 0 (OE, WE, BHE and BLE)	L		2	20		2	20	μ A
			LL		2	5		2	5	
I_{SB2}	Automatic CE Power-down Current – CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V, $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0, $V_{CC} = 1.95$ V	L		2	20		2	20	μ A
			LL		2	5		2	5	

Capacitance^[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ$ C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	$V_{CC} = V_{CC}(typ)$	8	pF

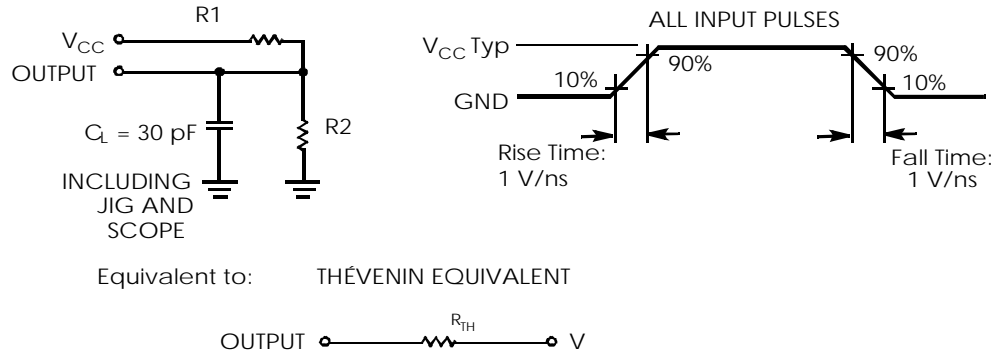
Notes:

- $V_{IL}(min.) = -2.0$ V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC}(typ)$, $T_A = 25^\circ$ C.
- Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance

Parameter	Description	Test Conditions	BGA	Unit
θ_{JA}	Thermal Resistance (Junction to Ambient) ^[6]	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	55	C/W
θ_{JC}	Thermal Resistance (Junction to Case) ^[6]		16	C/W

AC Test Loads and Waveforms

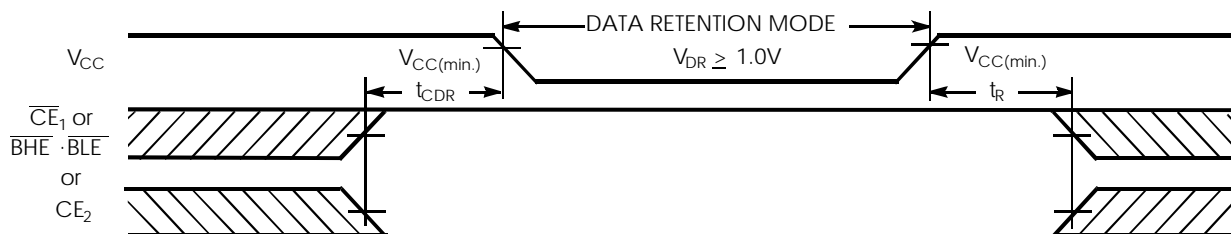


Parameters	1.8V	UNIT
R1	13500	Ω
R2	10800	Ω
R_{TH}	6000	Ω
V_{TH}	0.80	V

Data Retention Characteristics

Parameter	Description	Conditions	Min.	Typ. ^[5]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.0		1.95	V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.0V, \overline{CE}_1 \geq V_{CC} - 0.2V, \overline{CE}_2 \leq 0.2V, V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	L	1	10	μA
			LL		3	
$t_{CDR}^{[6]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[7]}$	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform^[8]

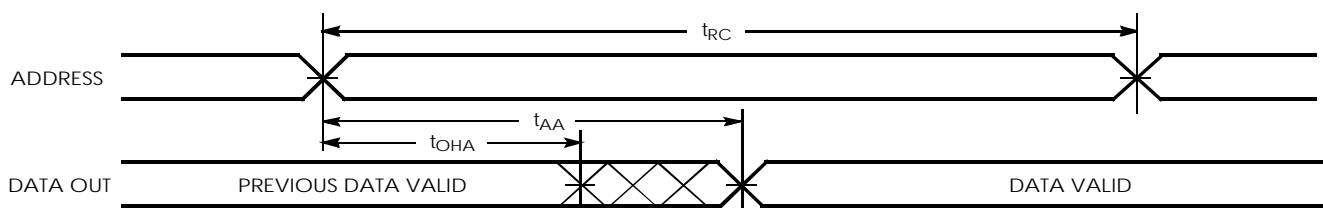


Notes:

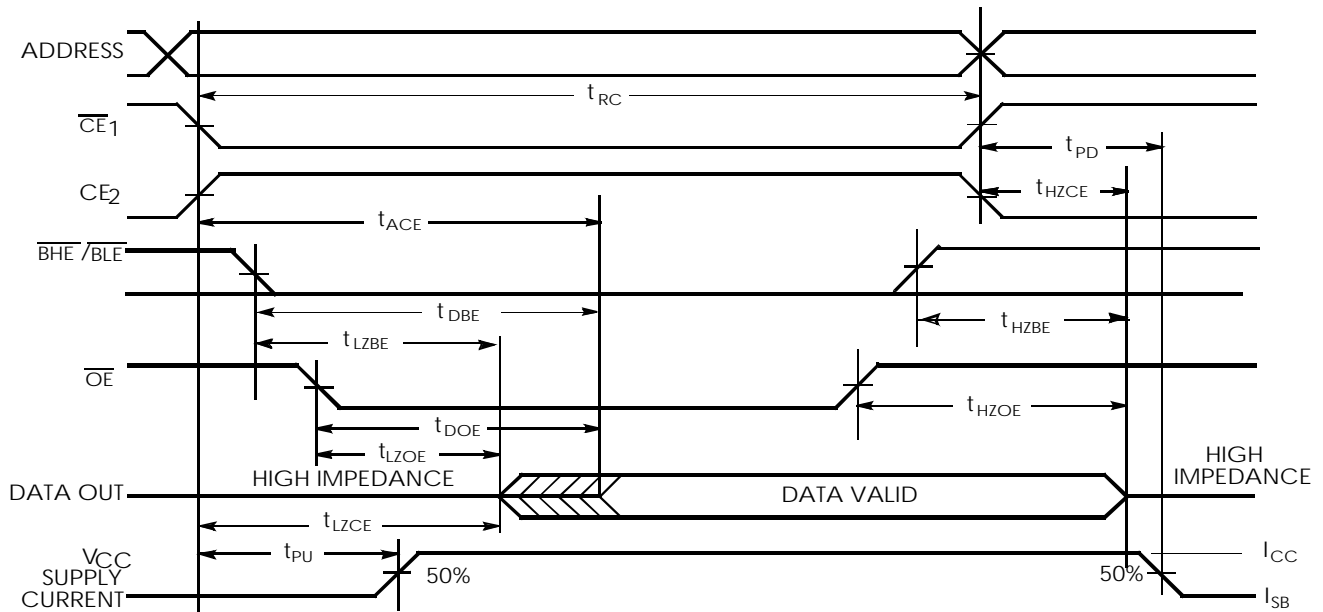
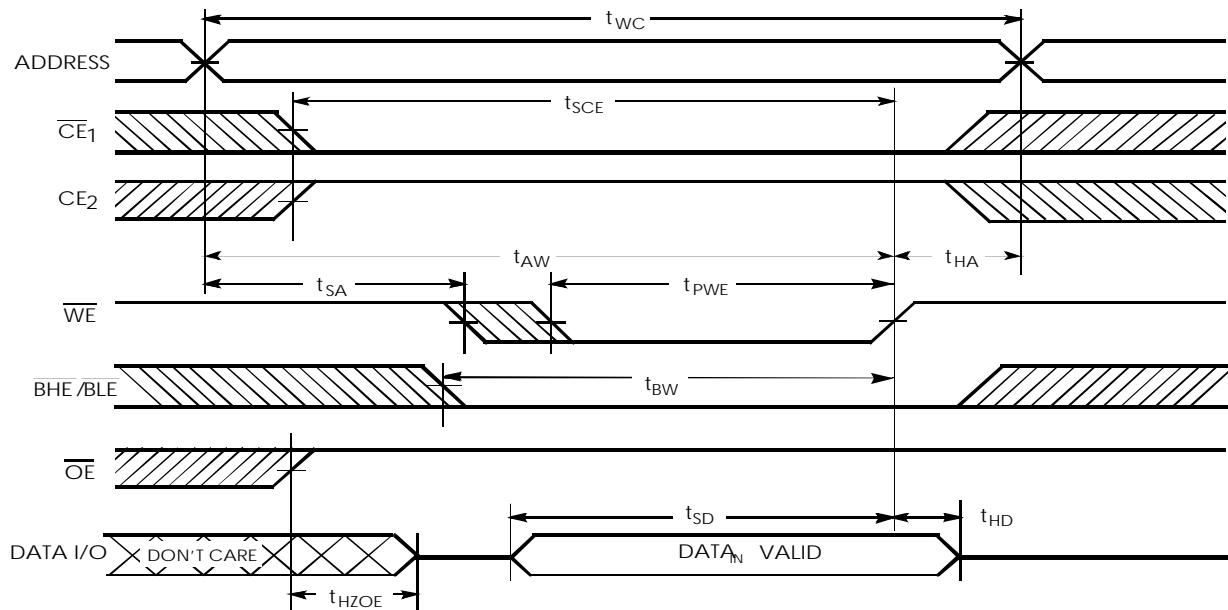
- Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} > 100 \mu s$ or stable at $V_{CC(min.)} > 100 \mu s$.
- $\overline{BHE} \cdot \overline{BLE}$ is the AND of both \overline{BHE} and \overline{BLE} . Chip can be deselected by either disabling the chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .

Switching Characteristics (Over the Operating Range)^[9]

Parameter	Description	CY62157DV18-55		CY62157DV18-70		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	\overline{CE}_1 LOW or CE_2 HIGH to Data Valid		55		70	ns
t_{DOE}	\overline{OE} LOW to Data Valid		25		35	ns
t_{LZOE}	\overline{OE} LOW to Low $Z^{[10]}$	5		5		ns
t_{HZOE}	\overline{OE} HIGH to High $Z^{[10, 12]}$		20		25	ns
t_{LZCE}	\overline{CE}_1 LOW or CE_2 HIGH to Low $Z^{[10]}$	10		10		ns
t_{HZCE}	\overline{CE}_1 HIGH or CE_2 LOW to High $Z^{[10, 12]}$		20		25	ns
t_{PU}	\overline{CE}_1 LOW or CE_2 HIGH to Power-up	0		0		ns
t_{PD}	\overline{CE}_1 HIGH or CE_2 LOW to Power-down		55		70	ns
t_{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		55		70	ns
$t_{LZBE}^{[11]}$	$\overline{BLE}/\overline{BHE}$ LOW to Low $Z^{[10]}$	5		5		ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to High- $Z^{[10, 12]}$		20		25	ns
Write Cycle^[13]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	\overline{CE}_1 LOW or CE_2 HIGH to Write End	45		60		ns
t_{AW}	Address Set-up to Write End	45		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	\overline{WE} Pulse Width	45		50		ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to Write End	45		60		ns
t_{SD}	Data Set-up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	\overline{WE} LOW to High $Z^{[10, 12]}$		20		25	ns
t_{LZWE}	\overline{WE} HIGH to Low $Z^{[10]}$	10		10		ns

Switching Waveforms
Read Cycle No. 1 (Address Transition Controlled)^[14, 15]

Notes:

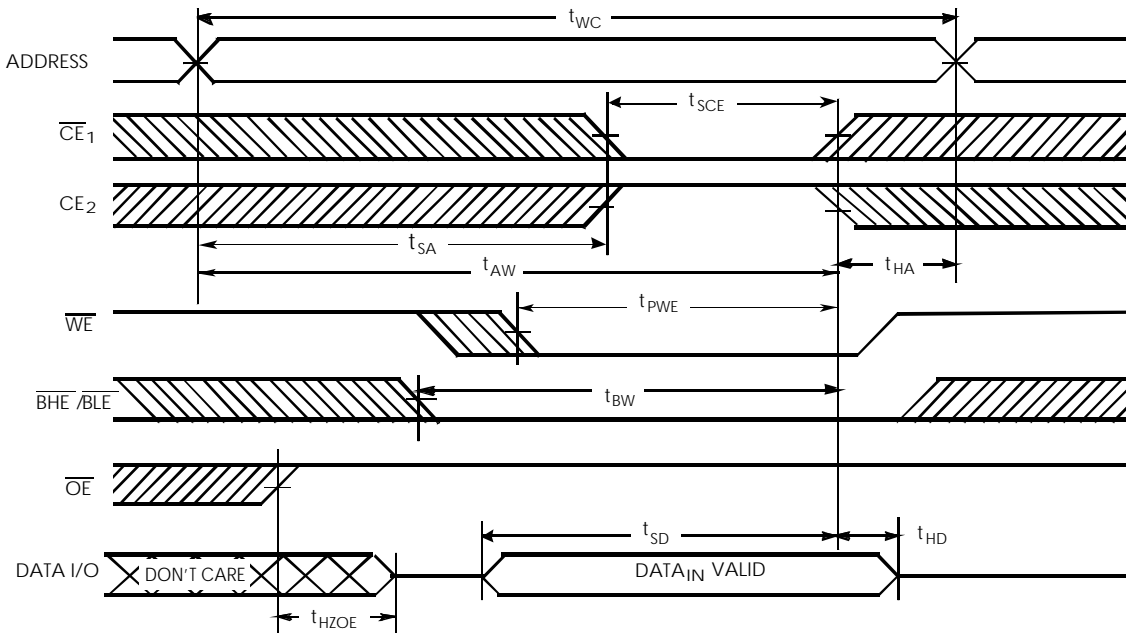
9. Test conditions assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL} .
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} .
11. If both byte enables are toggled together, this value is 10 ns.
12. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
13. The internal Write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$.
14. Device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, $\overline{CE}_2 = V_{IH}$.
15. \overline{WE} is HIGH for Read cycle.

Switching Waveforms (continued)
Read Cycle No. 2 (\overline{OE} Controlled)^[15, 16]

Write Cycle No. 1 (\overline{WE} Controlled)^[13, 17, 18, 19]

Notes:

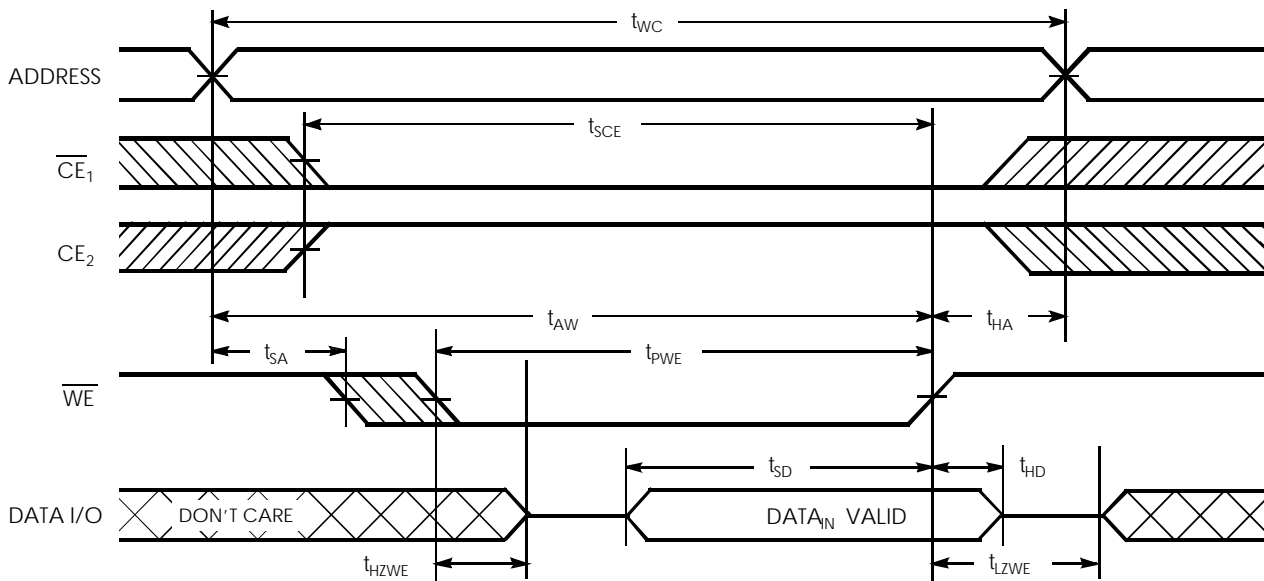
16. Address valid prior to or coincident with \overline{CE}_1 , \overline{BHE} , \overline{BLE} transition LOW and CE_2 transition HIGH.
17. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
18. If \overline{CE}_1 goes HIGH or CE_2 goes LOW simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
19. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

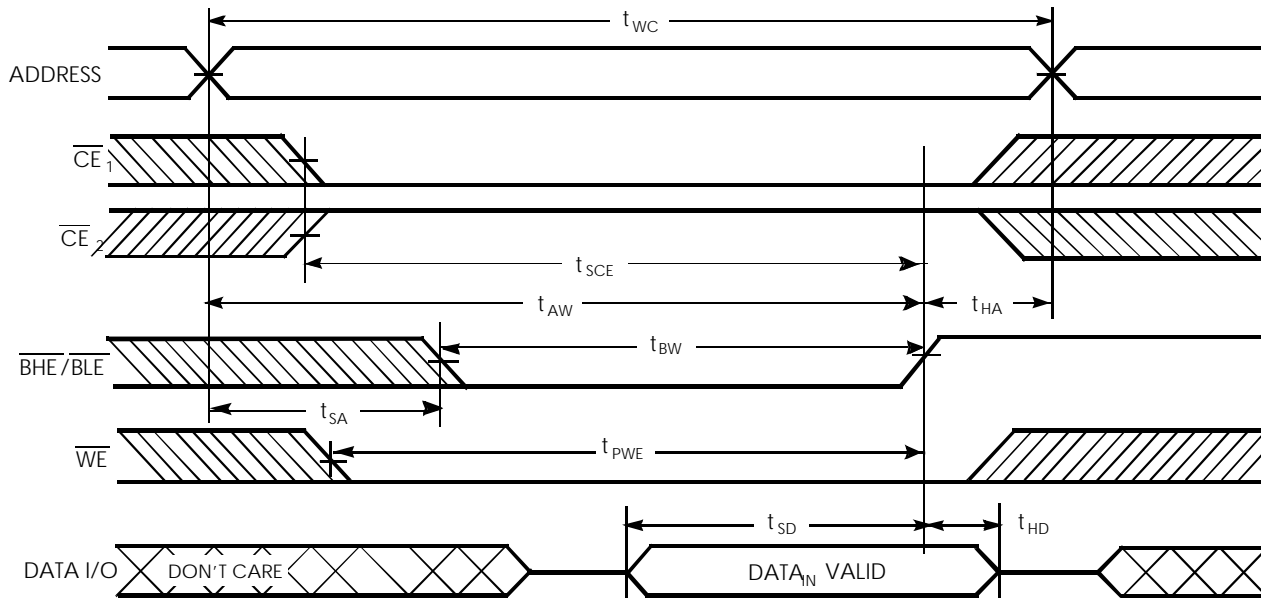
Write Cycle No. 2 (\overline{CE}_1 or \overline{CE}_2 Controlled) [13, 17, 18, 19]



Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [18, 19]



Switching Waveforms (continued)

Write Cycle No. 4 (BHE/BLE Controlled, \overline{OE} LOW)^[19]

Truth Table

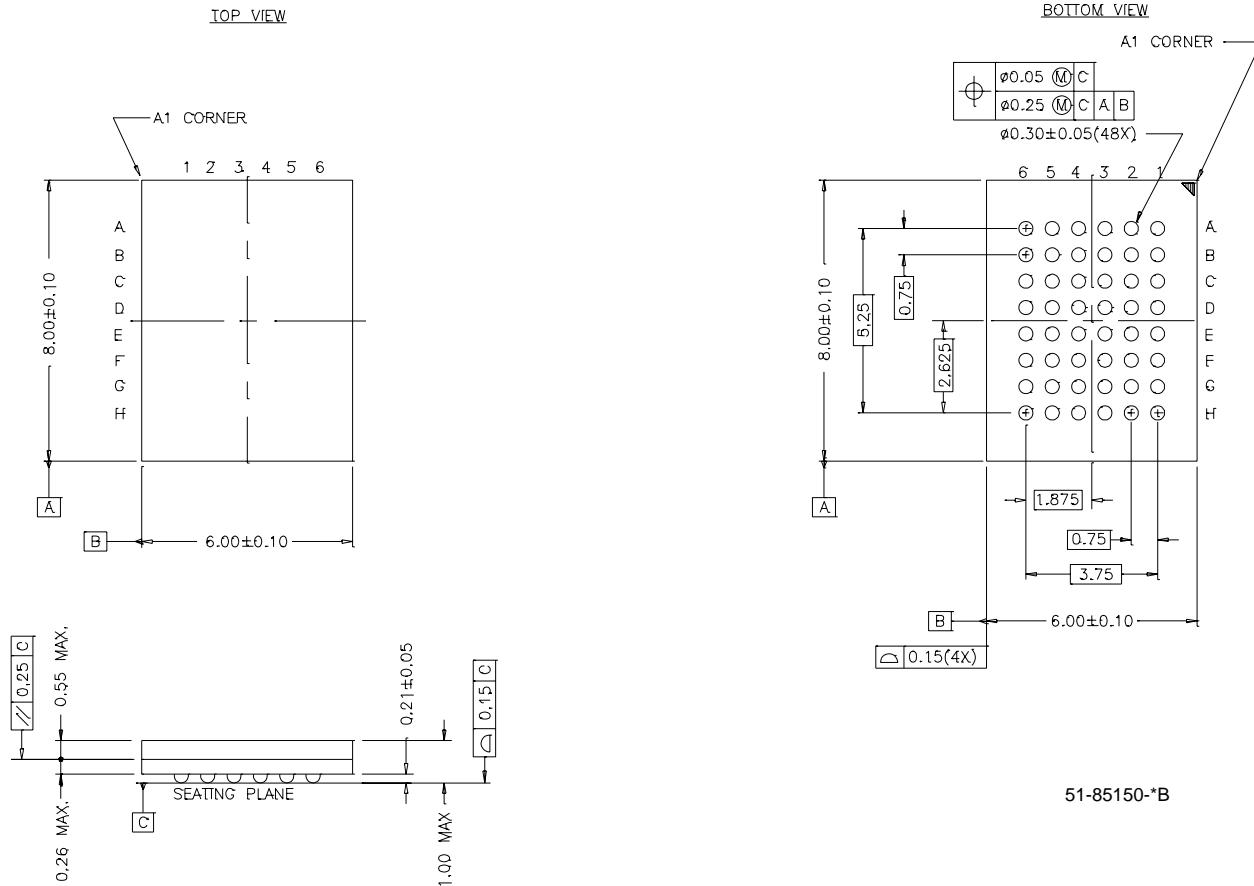
CE ₁	CE ₂	WE	OE	BHE	BLE	Input / Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-down	Standby(I _{SB})
X	L	X	X	X	X	High Z	Deselect/Power-down	Standby(I _{SB})
X	X	X	X	H	H	High Z	Deselect/Power-down	Standby(I _{SB})
L	H	H	L	L	L	Data Ou(I/O0- I/O15)	Read	Active(I _{CC})
L	H	H	L	H	L	Data Ou(I/O0- I/O7); High Z (I/O8- I/O15)	Read	Active(I _{CC})
L	H	H	L	L	H	High Z (I/O0- I/O7); Data Ou(I/O8- I/O15)	Read	Active(I _{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active(I _{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active(I _{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active(I _{CC})
L	H	L	X	L	L	Data In (I/O0- I/O15)	Write	Active(I _{CC})
L	H	L	X	H	L	Data In (I/O0- I/O7); High Z (I/O8- I/O15)	Write	Active(I _{CC})
L	H	L	X	L	H	High Z (I/O0- I/O7); Data In (I/O8- I/O15)	Write	Active(I _{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62157DV18L-55BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	Industrial
	CY62157DV18LL-55BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
70	CY62157DV18L-70BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	Industrial
	CY62157DV18LL-70BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	

Package Diagrams

48-Lead VFBGA (6 x 8 x 1 mm) BV48A



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Document History Page

Document Title: CY62157DV18 MoBL2™ 8M (512K x 16) Static RAM				
Document Number: 38-05126				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	112603	03/01/02	GAV	New Data Sheet, Die rev replacing CY62157CV18
*A	116601	06/14/02	MGN	Added second power bin (L and LL) Changed from Advance Information to Preliminary
*B	124694	03/18/03	DPM	Changed Preliminary to Final Added LL Bin to lccdr = 3 uA max Added new footnotes (1 and 2) Filled in TBD values