

## 512K x 8 MoBL Static RAM

### Features

- **High Speed**
  - 55 ns and 70 ns availability
- **Low voltage range:**
  - CY62148CV25: 2.2V–2.7V
  - CY62148CV30: 2.7V–3.3V
  - CY62148CV33: 3.0V–3.6V
- **Pin compatible with CY62148V**
- **Ultra low active power**
  - Typical active current: 1.5 mA @ f = 1MHz
  - Typical active current: 5.5 mA @ f = f<sub>max</sub> (70 ns speed)
- **Low standby power**
- **Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

### Functional Description

The CY62148CV25/30/33 are high-performance CMOS static RAMs organized as 512K words by 8 bits. This device features

advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 80% when addresses are not toggling. The device can be put into standby mode when deselected ( $\overline{CE}$  HIGH).

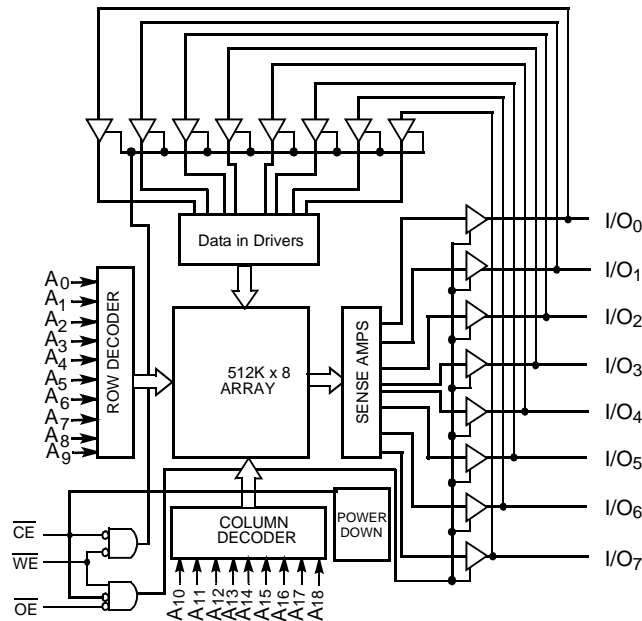
Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ).

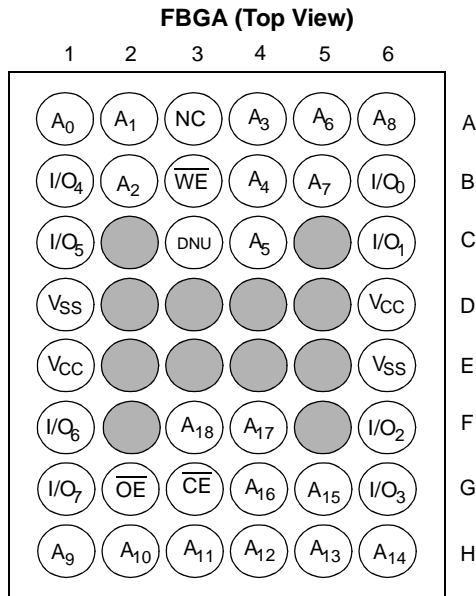
Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

The CY62148CV25/30/33 are available in a 36-ball FBGA package.

### Logic Block Diagram



**Pin Configurations<sup>[1,2]</sup>**

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....-65°C to +150°C  
 Ambient Temperature with Power Applied.....-55°C to +125°C  
 Supply Voltage to Ground Potential.....-0.5V to V<sub>CCmax</sub> + 0.5V

**DC Voltage Applied to Outputs**

in High Z State<sup>[3]</sup> .....-0.5V to V<sub>CC</sub> + 0.3V  
 DC Input Voltage<sup>[3]</sup> .....-0.5V to V<sub>CC</sub> + 0.3V  
 Output Current into Outputs (LOW).....20 mA  
 Static Discharge Voltage.....>2001V  
 MIL-STD-883, Method 3015)  
 Latch-Up Current >.....>200 mA

**Operating Range**

Product	Range	Ambient Temperature	V <sub>CC</sub>
CY62148CV25	Industrial	-40°C to +85°C	2.2V to 2.7V
CY62148CV30			2.7V to 3.3V
CY62148CV33			3.0V to 3.6V

**Product Portfolio**

Product	V <sub>CC</sub> Range			Speed	Power Dissipation (Industrial)					
					Operating (I <sub>CC</sub> )				Standby (I <sub>SB2</sub> )	
	Min.	Typ. <sup>[4]</sup>	Max.		f = 1 MHz		f = f <sub>max</sub>		Typ. <sup>[4]</sup>	Max.
					Typ. <sup>[4]</sup>	Max.	Typ. <sup>[4]</sup>	Max.		
CY62148CV25	2.2V	2.5V	2.7V	55 ns	1.5 mA	3 mA	7 mA	15 mA	5 μA	15 μA
				70 ns	1.5 mA	3 mA	5.5 mA	12 mA		
CY62148CV30	2.7V	3.0V	3.3V	55 ns	1.5 mA	3 mA	7 mA	15 mA	7 μA	15 μA
				70 ns	1.5 mA	3 mA	5.5 mA	12 mA		
CY62148CV33	3.0V	3.3V	3.6V	55 ns	1.5 mA	3 mA	7 mA	15 mA	8 μA	20 μA
				70 ns	1.5 mA	3 mA	5.5 mA	12 mA		

**Notes:**

- NC pins are not connected to the die.
- C3 (DNU) can be left as NC or V<sub>SS</sub> to ensure proper application.
- V<sub>L(min.)</sub> = -2.0V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions		CY62148CV25-55			CY62148CV25-70			Unit
				Min.	Typ. <sup>[4]</sup>	Max.	Min.	Typ. <sup>[4]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> = Min.	2.0			2.0			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA	V <sub>CC</sub> = MinV			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage			1.8		V <sub>CC</sub> +0.3V	1.8		V <sub>CC</sub> +0.3V	V
V <sub>IL</sub>	Input LOW Voltage			-0.3		0.6	-0.3		0.6	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = 3.6V		7	15		5.5	12	mA
		f = 1 MHz	I <sub>OUT</sub> = 0 mA CMOS Levels		1.5	3		1.5	3	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = f_{max}$ (Address and Data Only), $f = 0$ (OE, WE)			5	15		5	15	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0$ , V <sub>CC</sub> = 3.6V								

Parameter	Description	Test Conditions		CY62148CV30-55			CY62148CV30-70			Unit
				Min.	Typ. <sup>[4]</sup>	Max.	Min.	Typ. <sup>[4]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = Min.	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA	V <sub>CC</sub> = MinV			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage			2.2		V <sub>CC</sub> +0.5V	2.2		V <sub>CC</sub> +0.5V	V
V <sub>IL</sub>	Input LOW Voltage			-0.3		0.8	-0.3		0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = 3.6V		12	25		7	15	mA
		f = 1 MHz	I <sub>OUT</sub> = 0 mA CMOS Levels		1.5	3		1.5	3	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = f_{max}$ (Address and Data Only), $f = 0$ (OE, WE)			7	15		7	15	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0$ , V <sub>CC</sub> = 3.6V								

Parameter	Description	Test Conditions		CY62148CV33-55			CY62148CV33-70			Unit
				Min.	Typ. <sup>[4]</sup>	Max.	Min.	Typ. <sup>[4]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 3.0V	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA	V <sub>CC</sub> = 3.0V			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage			2.2		V <sub>CC</sub> +0.5V	2.2		V <sub>CC</sub> +0.5V	V
V <sub>IL</sub>	Input LOW Voltage			-0.3		0.8	-0.3		0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = 3.6V		7	15		5.5	12	mA
		f = 1 MHz	I <sub>OUT</sub> = 0 mA CMOS Levels		1.5	3		1.5	3	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = f_{max}$ (Address and Data Only), $f = 0$ (OE, WE)			8	20		8	20	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0, V_{CC} = 3.6V$								

### Capacitance<sup>5</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ.)</sub>	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

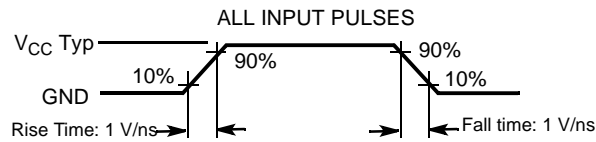
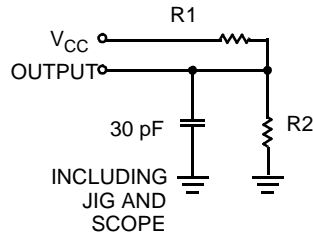
### Thermal Resistance

Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance <sup>[5]</sup> (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	Θ <sub>JA</sub>	55	°C/W
Thermal Resistance <sup>[5]</sup> (Junction to Case)		Θ <sub>JC</sub>	16	°C/W

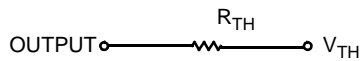
**Note:**

- Tested initially and after any design or process changes that may affect these parameters.

### AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

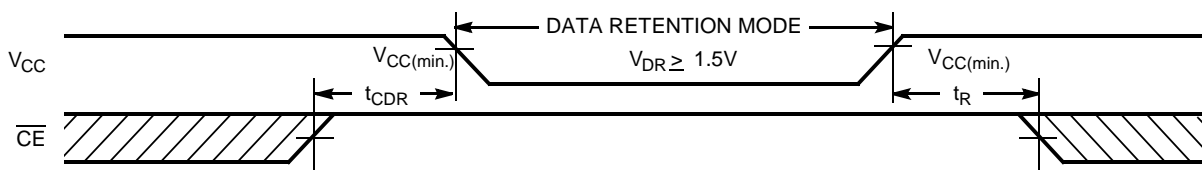


Parameters	2.5V	3.0V	3.3V	Unit
R1	16.6	1.105	1.216	K Ohms
R2	15.4	1.550	1.374	K Ohms
R <sub>TH</sub>	8.0	0.645	0.645	K Ohms
V <sub>TH</sub>	1.20	1.75	1.75	Volts

### Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. <sup>[4]</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.5		V <sub>CCmax</sub>	V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = 1.5V CE ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V		3	10	μA
t <sub>CDR</sub> <sup>[5]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[6]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

### Data Retention Waveform



**Note:**

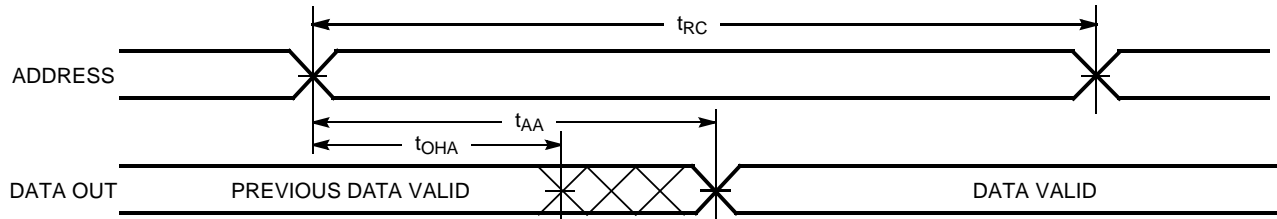
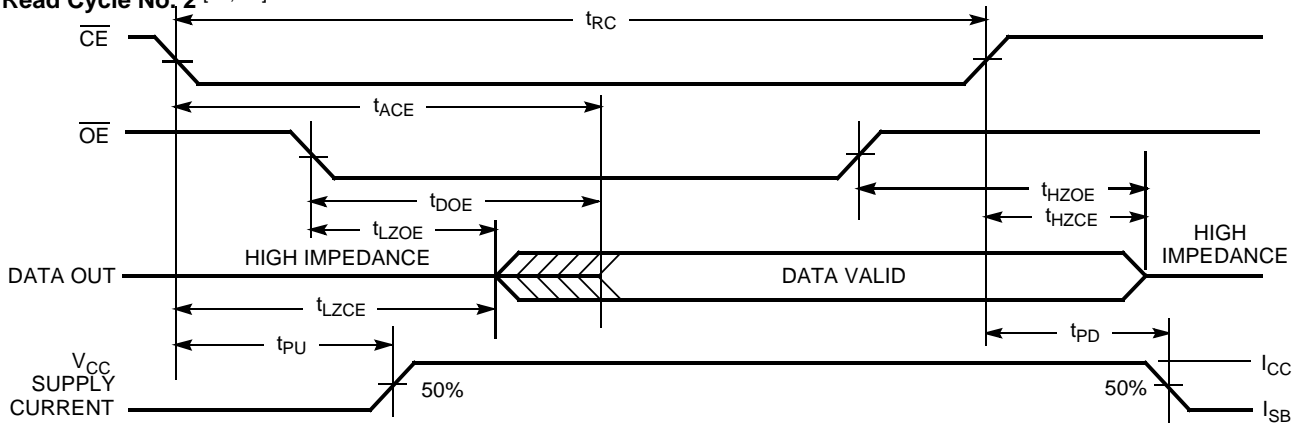
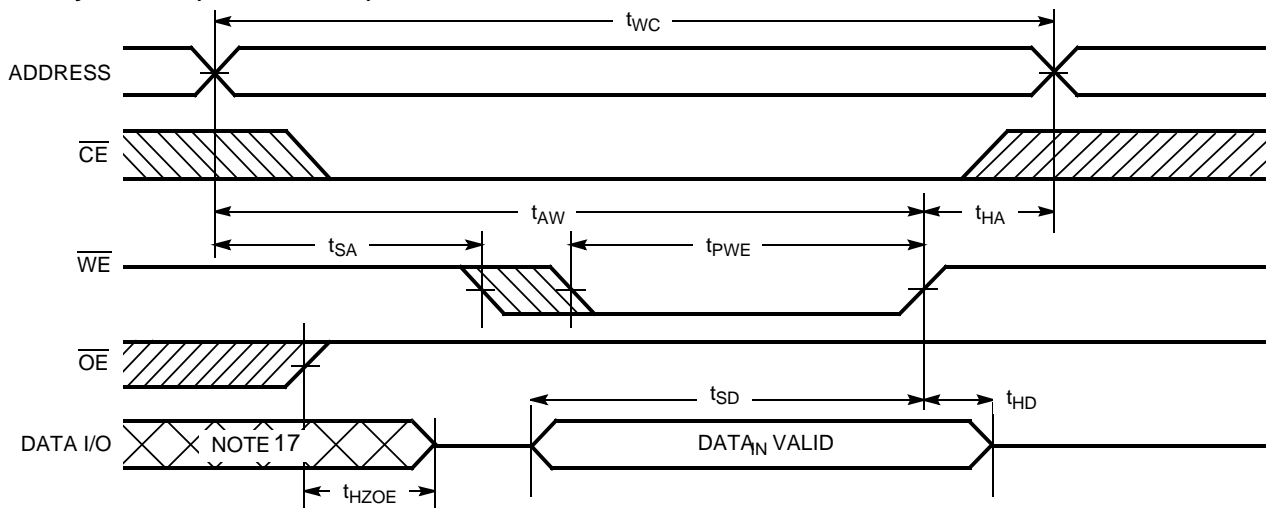
- Full Device AC operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min.)</sub> ≥ 50 μs or stable at V<sub>CC(min.)</sub> ≥ 50 μs.

**Switching Characteristics** Over the Operating Range<sup>[7]</sup>

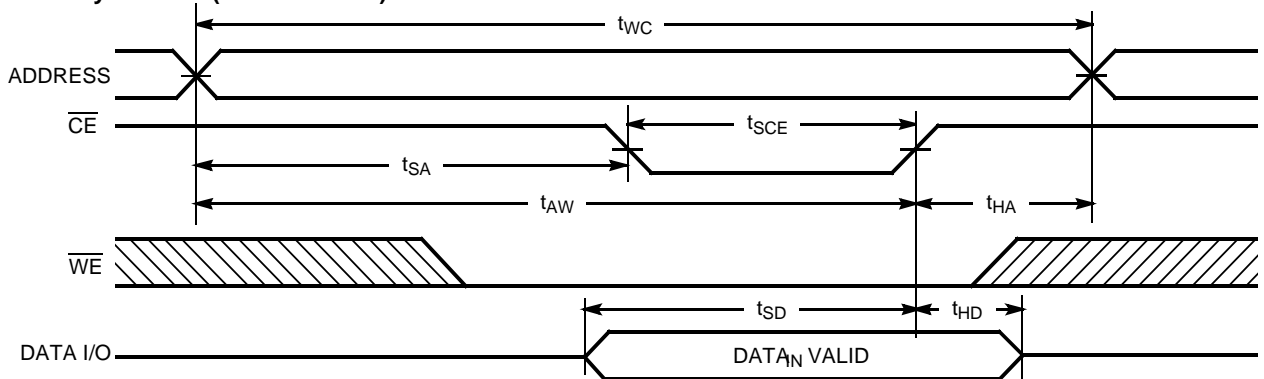
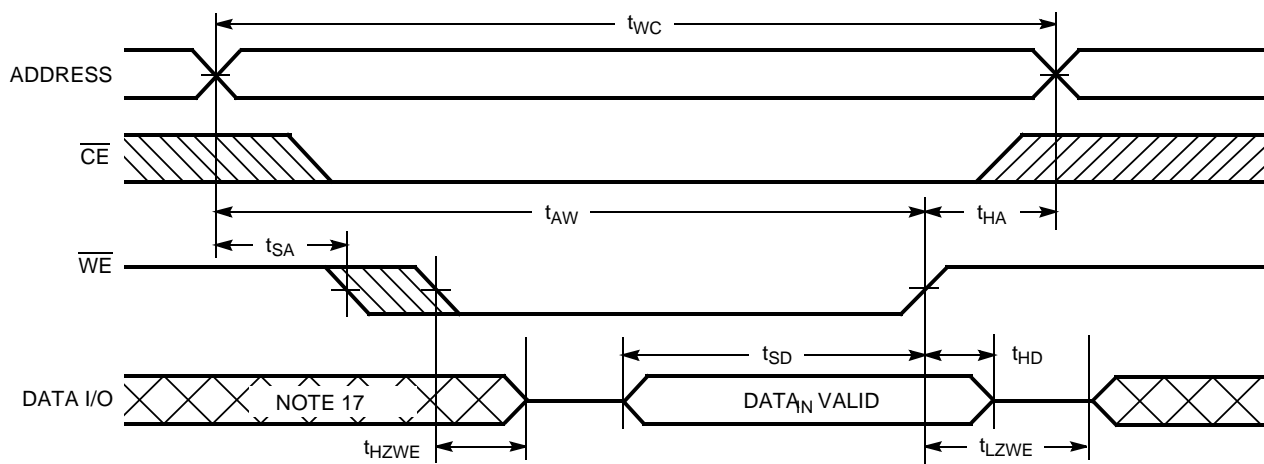
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
$t_{RC}$	Read Cycle Time	55		70		ns
$t_{AA}$	Address to Data Valid		55		70	ns
$t_{OHA}$	Data Hold from Address Change	10		10		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		55		70	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		25		35	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[8]</sup>	5		5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[9]</sup>		20		25	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[8]</sup>	10		10		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[8, 9]</sup>		20		25	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		55		70	ns
<b>WRITE CYCLE<sup>[10, 11]</sup></b>						
$t_{WC}$	Write Cycle Time	55		70		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	45		60		ns
$t_{AW}$	Address Set-Up to Write End	45		60		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	45		50		ns
$t_{SD}$	Data Set-Up to Write End	30		30		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[8, 9]</sup>		20		25	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[8]</sup>	5		10		ns

**Notes:**

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to  $V_{CC(typ.)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) of AC Test Loads. Transition is measured  $\pm 200$  mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle #3 (WE controlled, OE LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Switching Waveforms**
**Read Cycle No. 1** [12, 13]

**Read Cycle No. 2** [13, 14]

**Write Cycle No. 1 (WE Controlled)** [10, 15, 16]

**Notes:**

12. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
13.  $\overline{WE}$  is HIGH for read cycle.
14. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
15. Data I/O is high impedance if  $\overline{OE} = V_{IL}$ .
16. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.

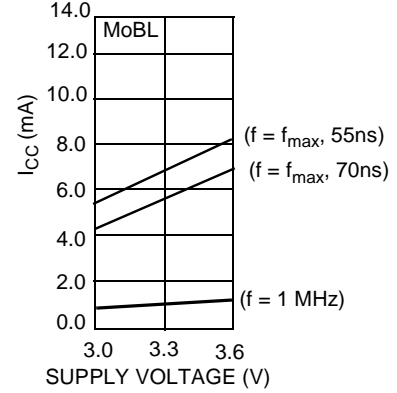
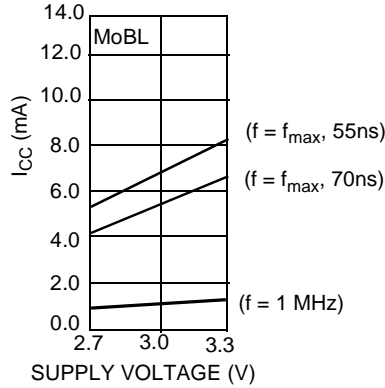
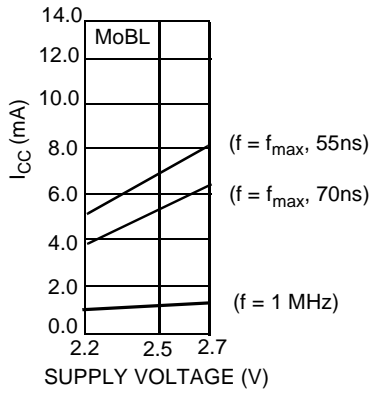
**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)** [10, 15, 16]

**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)** [11, 16]




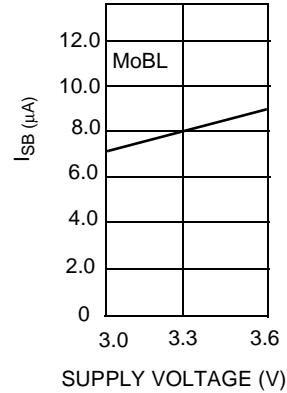
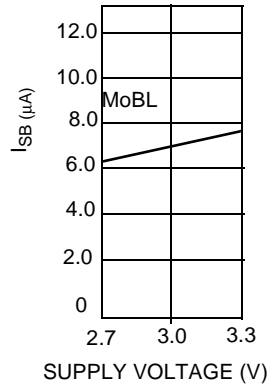
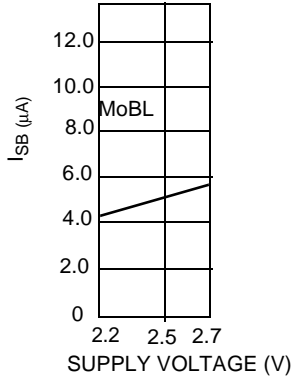
## Typical DC and AC Parameters

(Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25^\circ\text{C}$ .)

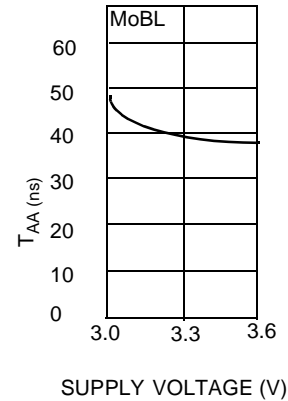
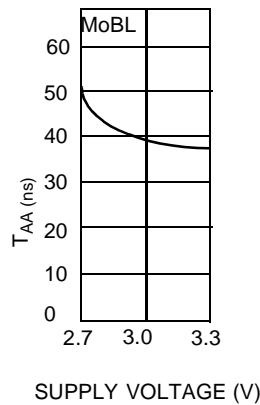
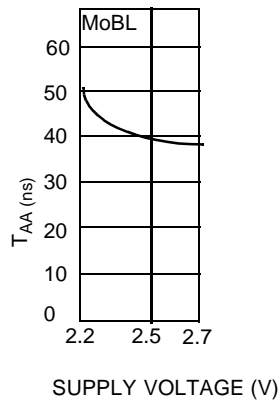
### Operating Current vs. Supply Voltage



### Standby Current vs. Supply Voltage



### Access Time vs. Supply Voltage



### Truth Table

CE	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	L	X	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Output Disabled	Active ( $I_{CC}$ )

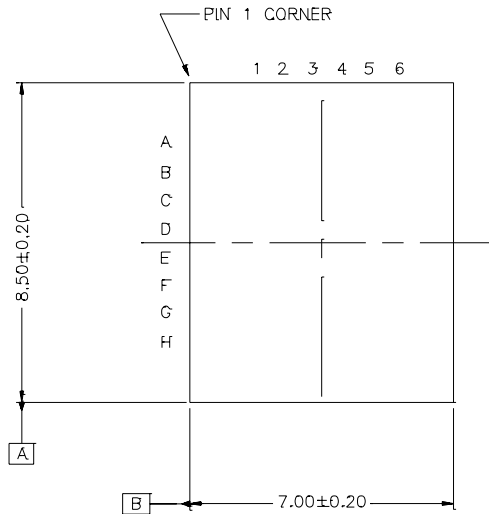
**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62148CV25LL-70BAI	BA36B	36-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	Industrial
	CY62148CV25LL-70BVI	BV36A	36-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62148CV30LL-70BAI	BA36B	36-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62148CV30LL-70BVI	BV36A	36-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62148CV33LL-70BAI	BA36B	36-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62148CV33LL-70BVI	BV36A	36-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
55	CY62148CV25LL-55BAI	BA36B	36-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62148CV25LL-55BVI	BV36A	36-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62148CV30LL-55BAI	BA36B	36-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62148CV30LL-55BVI	BV36A	36-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62148CV33LL-55BAI	BA36B	36-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62148CV33LL-55BVI	BV36A	36-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	

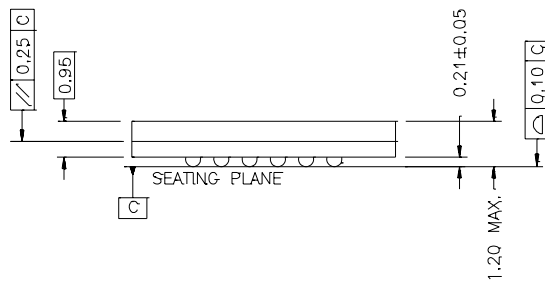
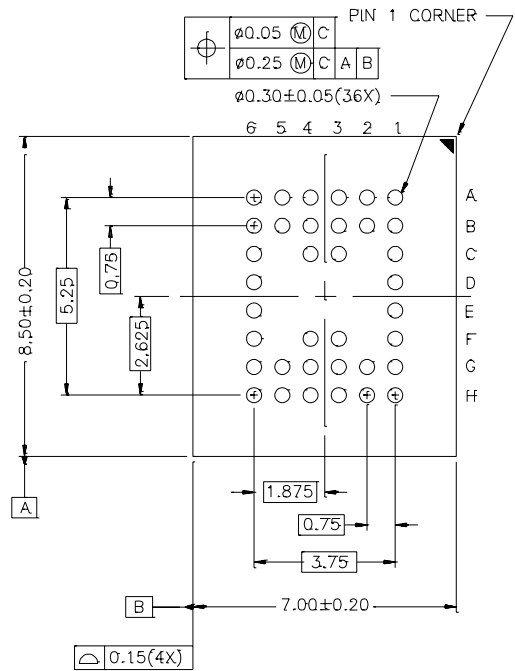
**Package Diagrams**

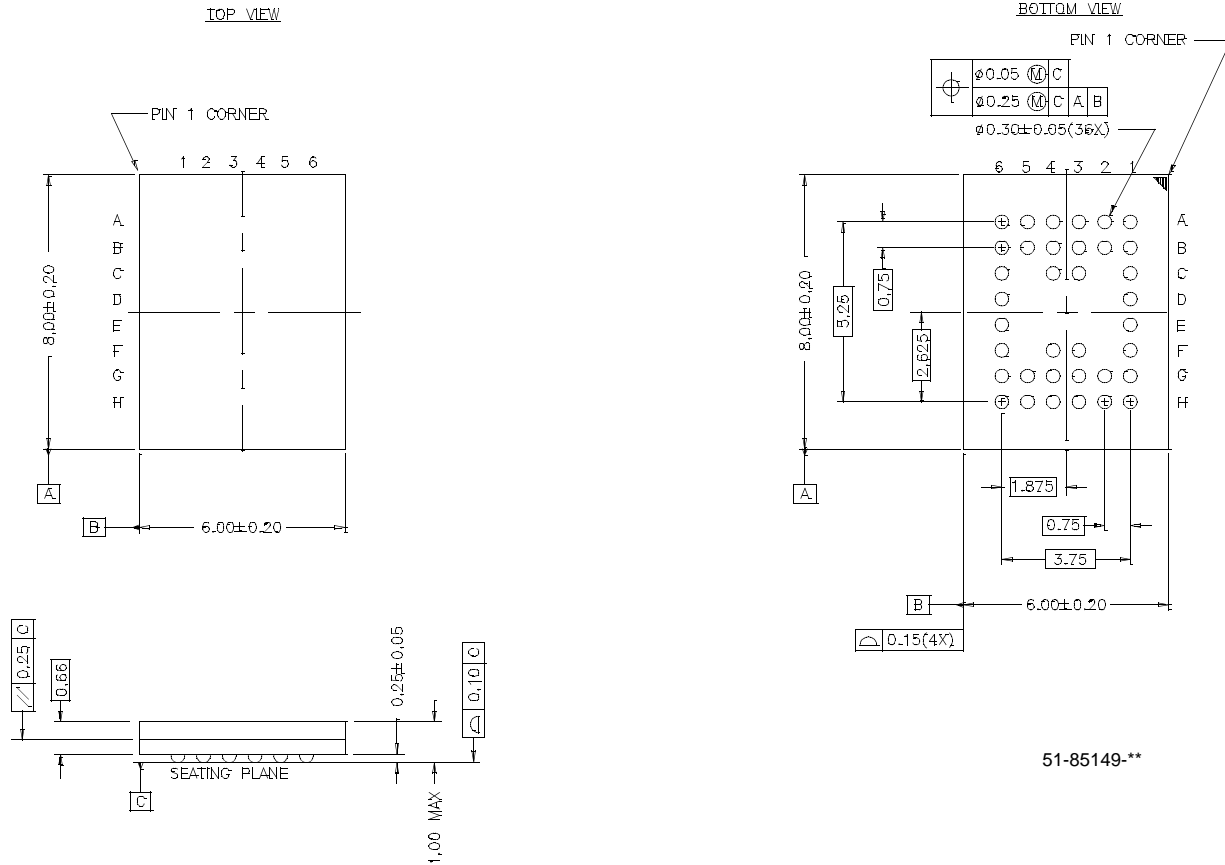
**36-Ball (7.00 mm x 8.5 mm x 1.2 mm) Thin BGA BA36B**

TOP VIEW



BOTTOM VIEW



**Package Diagrams (continued)**
**36-Lead VFBGA (6 x 8 x 1 mm) BV36A**


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<b>Document Title: CY62148CV25/30/33 MoBL™ 512K x 8 MoBL Static RAM</b> <b>Document Number: 38-05035</b>				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109951	12/02/01	SZV	Change from Spec number: 38-01126 to 38-05035
*A	110643	05/01/02	MGN	Advance to Final, Improved Typical and Max Icc values, added BV package