

## 256K x 16 Static RAM

### Features

- **High Speed**
  - 55 ns and 70 ns availability
- **Voltage range:**
  - CY62147CV25: 2.2V–2.7V
  - CY62147CV30: 2.7V–3.3V
  - CY62147CV33: 3.0V–3.6V
- **Pin Compatible with CY62147V**
- **Ultra-low active power**
  - Typical active current: 1.5 mA @ f = 1 MHz
  - Typical active current: 5.5 mA @ f = f<sub>max</sub> (70 ns speed)
- **Low standby power**
- **Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

### Functional Description

The CY62147CV25/30/33 are high-performance CMOS static RAMs organized as 256K words by 16 bits. These devices feature advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The devices also have an automatic power-down feature that signifi-

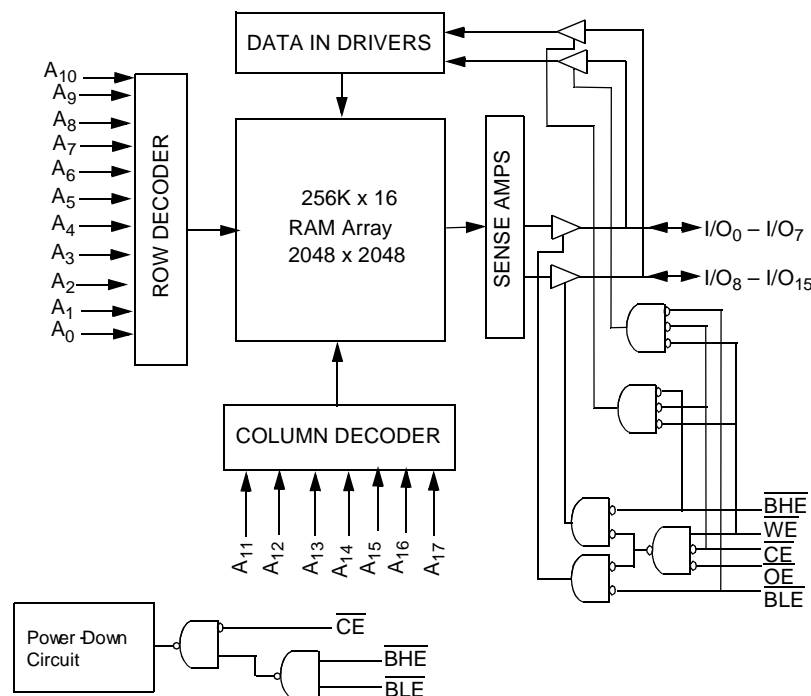
cantly reduces power consumption by 80% when addresses are not toggling. The device can also be put into standby mode reducing power consumption by more than 99% when deselected ( $\overline{\text{CE}}$  HIGH or both  $\overline{\text{BLE}}$  and  $\overline{\text{BHE}}$  are HIGH). The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when: deselected ( $\overline{\text{CE}}$  HIGH), outputs are disabled ( $\overline{\text{OE}}$  HIGH), both Byte High Enable and Byte Low Enable are disabled ( $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  HIGH), or during a write operation ( $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW).

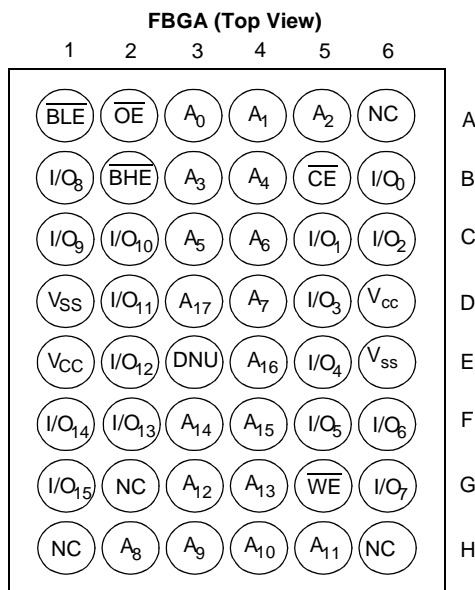
Writing to the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Write Enable ( $\overline{\text{WE}}$ ) inputs LOW. If Byte Low Enable ( $\overline{\text{BLE}}$ ) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>). If Byte High Enable ( $\overline{\text{BHE}}$ ) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>).

Reading from the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing the Write Enable ( $\overline{\text{WE}}$ ) HIGH. If Byte Low Enable ( $\overline{\text{BLE}}$ ) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable ( $\overline{\text{BHE}}$ ) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the back of this data sheet for a complete description of read and write modes.

The CY62147CV25/30/33 are available in a 48-ball FBGA package.

### Logic Block Diagram



**Pin Configuration<sup>[1, 2]</sup>**

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied..... -55°C to +125°C

Supply Voltage to Ground Potential ... -0.5V to V<sub>CCmax</sub> + 0.5V

DC Voltage Applied to Outputs in High Z State<sup>[3]</sup> ..... -0.5V to V<sub>CC</sub> + 0.3V

DC Input Voltage<sup>[3]</sup> ..... -0.5V to V<sub>CC</sub> + 0.3V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

**Operating Range**

Device	Range	Ambient Temperature	V <sub>CC</sub>
CY62147CV25	Industrial	-40°C to +85°C	2.2V to 2.7V
CY62147CV30			2.7V to 3.3V
CY62147CV33			3.0V to 3.6V

**Product Portfolio**

Product	V <sub>CC</sub> Range			Speed	Power Dissipation (Industrial)					
					Operating, I <sub>CC</sub>				Standby (I <sub>SB2</sub> )	
	V <sub>CC(min.)</sub>	V <sub>CC(typ.)</sub> <sup>[4]</sup>	V <sub>CC(max.)</sub>		f = 1 MHz		f = f <sub>max</sub>		Standby (I <sub>SB2</sub> )	
					Typ. <sup>[4]</sup>	Max.	Typ. <sup>[4]</sup>	Max.	Typ. <sup>[4]</sup>	Max.
CY62147CV25	2.2V	2.5V	2.7V	55 ns	1.5 mA	3 mA	7 mA	15 mA	5 μA	15 μA
				70 ns	1.5 mA	3 mA	5.5 mA	12 mA		
CY62147CV30	2.7V	3.0V	3.3V	55 ns	1.5 mA	3 mA	7 mA	15 mA	7 μA	15 μA
				70 ns	1.5 mA	3 mA	5.5 mA	12 mA		
CY62147CV33	3.0V	3.3V	3.6V	55 ns	1.5 mA	3 mA	7 mA	15 mA	8 μA	20 μA
				70 ns	1.5 mA	3 mA	5.5 mA	12 mA		

**Notes:**

1. NC pins are not connected to the die.
2. E3 (DNU) can be left as NC or V<sub>SS</sub> to ensure proper application.
3. V<sub>IL(min.)</sub> = -2.0V for pulse durations less than 20 ns.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions		CY62147CV25-55			CY62147CV25-70			Unit
				Min.	Typ. <sup>[4]</sup>	Max.	Min.	Typ. <sup>[4]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> = 2.2V	2.0			2.0			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA	V <sub>CC</sub> = 2.2V			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage			1.8		V <sub>CC</sub> + 0.3V	1.8		V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage			-0.3		0.6	-0.3		0.6	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = 2.7V I <sub>OUT</sub> = 0 mA CMOS Levels		7	15		5.5	12	mA
		f = 1 MHz			1.5	3		1.5	3	
I <sub>SB1</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = f_{max}$ (Address and Data Only), $f=0$ (OE,WE,BHE and BLE)			5	15		5	15	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0$ , V <sub>CC</sub> = 2.7V								

Parameter	Description	Test Conditions		CY62147CV30-55			CY62147CV30-70			Unit
				Min.	Typ. <sup>[4]</sup>	Max.	Min.	Typ. <sup>[4]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 2.7V	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA	V <sub>CC</sub> = 2.7V			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage			2.2		V <sub>CC</sub> + 0.3V	2.2		V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage			-0.3		0.8	-0.3		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = 3.3V I <sub>OUT</sub> = 0 mA CMOS Levels		7	15		5.5	12	mA
		f = 1 MHz			1.5	3		1.5	3	
I <sub>SB1</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = f_{max}$ (Address and Data Only), $f=0$ (OE,WE,BHE and BLE)			7	15		7	15	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0$ , V <sub>CC</sub> = 3.3V								

**Electrical Characteristics** Over the Operating Range (continued)

Parameter	Description	Test Conditions	CY62147CV33-55			CY62147CV33-70			Unit
			Min.	Typ. <sup>[4]</sup>	Max.	Min.	Typ. <sup>[4]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA V <sub>CC</sub> = 3.0V	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA V <sub>CC</sub> = 3.0V			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2		V <sub>CC</sub> + 0.3V	2.2		V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage		-0.3		0.8	-0.3		0.8	V
I <sub>Ix</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub> V <sub>CC</sub> = 3.6V I <sub>OUT</sub> = 0 mA CMOS Levels		7	15		5.5	12	mA
		f = 1 MHz		1.5	3		1.5	3	
I <sub>SB1</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , f = f <sub>max</sub> (Address and Data Only), f=0 (OE,WE,BHE and BLE)		8	20		8	20	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , f = 0, V <sub>CC</sub> = 3.6V							

**Capacitance<sup>[5]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC</sub> (typ.)	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

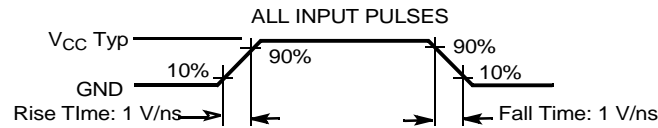
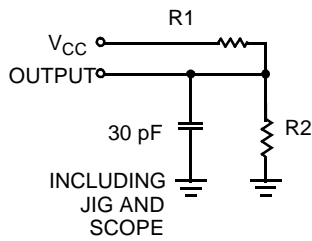
**Thermal Resistance**

Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance (Junction to Ambient) <sup>[5]</sup>	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	θ <sub>JA</sub>	55	°C/W
Thermal Resistance (Junction to Case) <sup>[5]</sup>		θ <sub>JC</sub>	16	°C/W

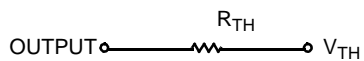
**Note:**

5. Tested initially and after any design or process changes that may affect these parameters.

### AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

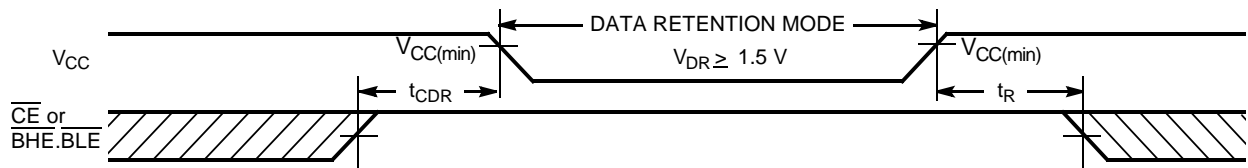


Parameters	2.5V	3.0V	3.3V	Unit
R1	16.6	1.105	1.216	KΩ
R2	15.4	1.550	1.374	KΩ
R <sub>TH</sub>	8	0.645	0.645	KΩ
V <sub>TH</sub>	1.20	1.75	1.75	Volts

### Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. <sup>[4]</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.5		V <sub>CCmax</sub>	V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = 1.5V CE ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V		3	10	μA
t <sub>CDR</sub> <sup>[5]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[6]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

### Data Retention Waveform<sup>[7]</sup>



**Note:**

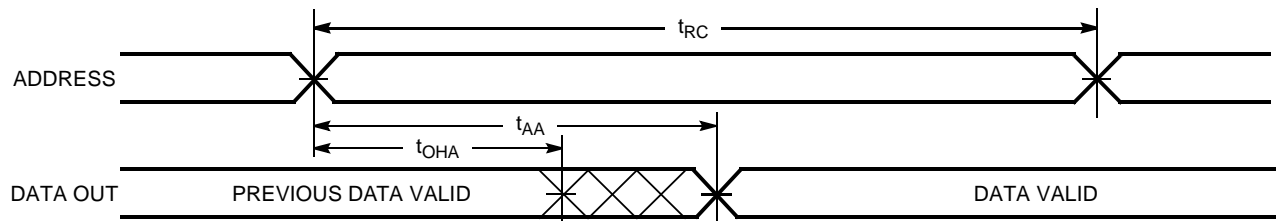
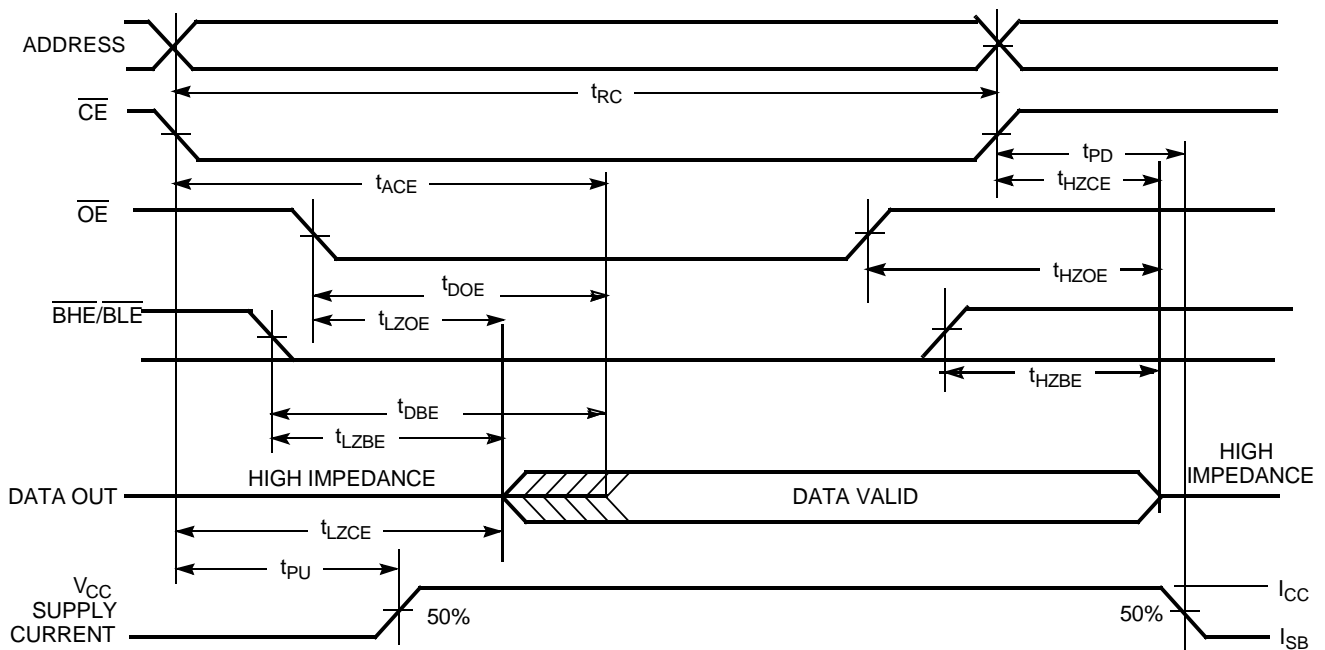
- Full Device AC operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min.)</sub> > 100μs or stable at V<sub>CC(min.)</sub> > 100 μs.
- BHE.BLE is the AND of both BHE and BLE. Chip can be deselected by either disabling the chip enable signals or by disabling both BHE and BLE.

**Switching Characteristics** Over the Operating Range<sup>[8]</sup>

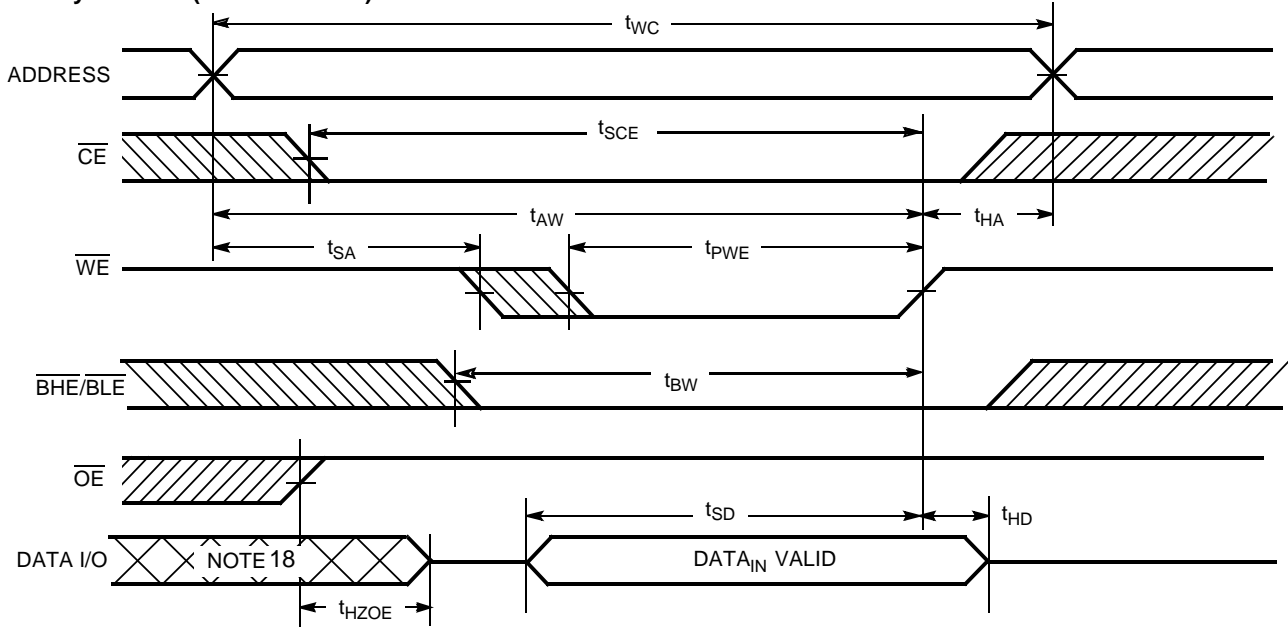
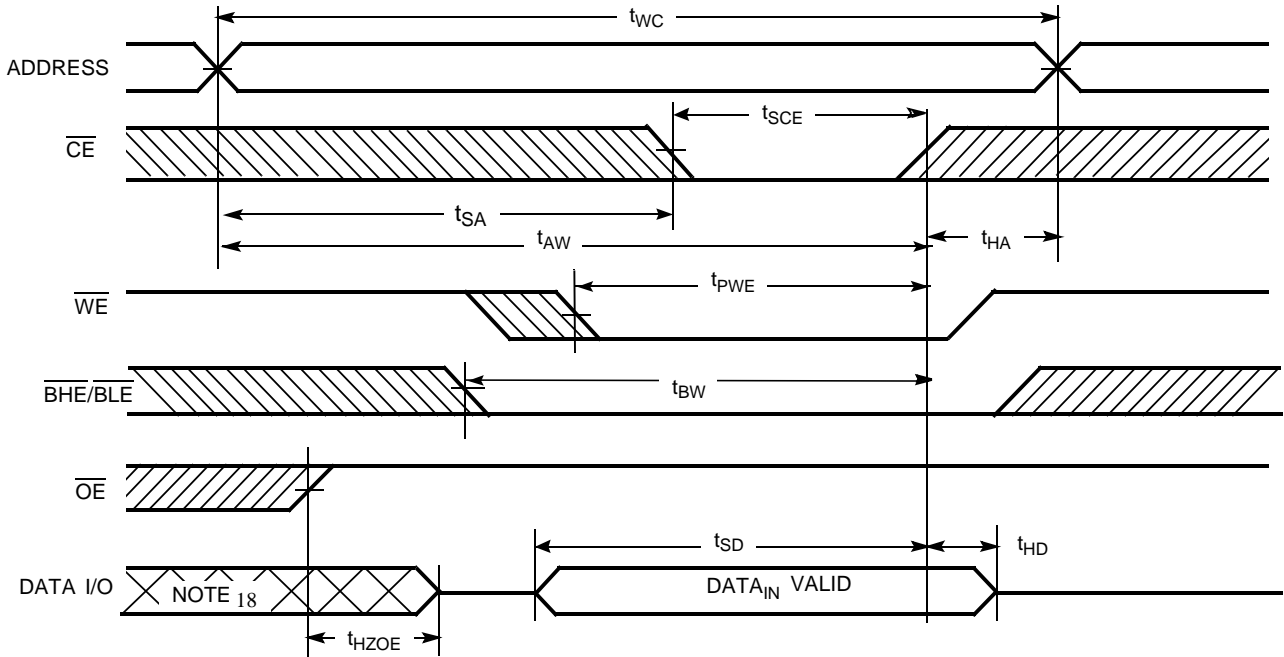
Parameter	Description	55 ns		70 ns		Unit
		Min	Max	Min	Max	
<b>READ CYCLE</b>						
t <sub>RC</sub>	Read Cycle Time	55		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		55		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		25		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[9]</sup>	5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[9, 11]</sup>		20		25	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[9]</sup>	10		10		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[9, 11]</sup>		20		25	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		55		70	ns
t <sub>DBE</sub>	$\overline{BHE}$ / $\overline{BLE}$ LOW to Data Valid		55		70	ns
t <sub>LZBE</sub> <sup>[10]</sup>	$\overline{BHE}$ / $\overline{BLE}$ LOW to Low Z <sup>[9]</sup>	5		5		ns
t <sub>HZBE</sub>	$\overline{BHE}$ / $\overline{BLE}$ HIGH to High Z <sup>[9, 11]</sup>		20		25	ns
<b>WRITE CYCLE<sup>[12]</sup></b>						
t <sub>WC</sub>	Write Cycle Time	55		70		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	45		60		ns
t <sub>AW</sub>	Address Set-Up to Write End	45		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	45		50		ns
t <sub>BW</sub>	$\overline{BHE}$ / $\overline{BLE}$ Pulse Width	50		60		ns
t <sub>SD</sub>	Data Set-Up to Write End	25		30		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[9, 11]</sup>		20		25	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[9]</sup>	5		5		ns

**Notes:**

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of  $V_{CC(typ.)}/2$ , input pulse levels of 0 to  $V_{CC(typ.)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZBE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- If both byte enables are toggled together this value is 10 ns.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high impedance state.
- The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

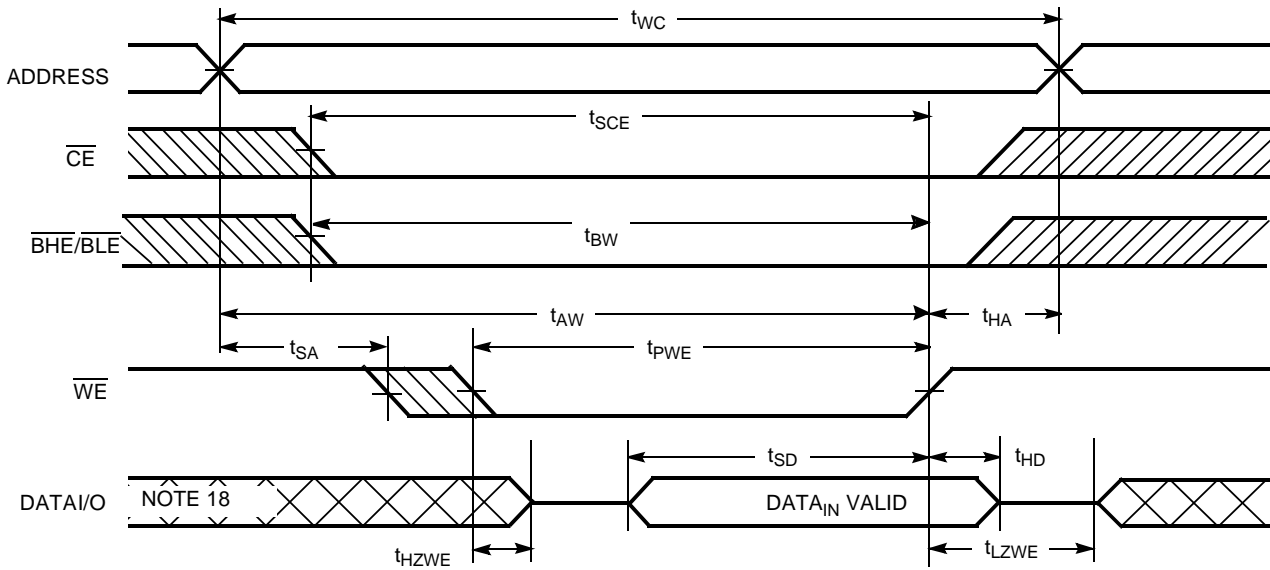
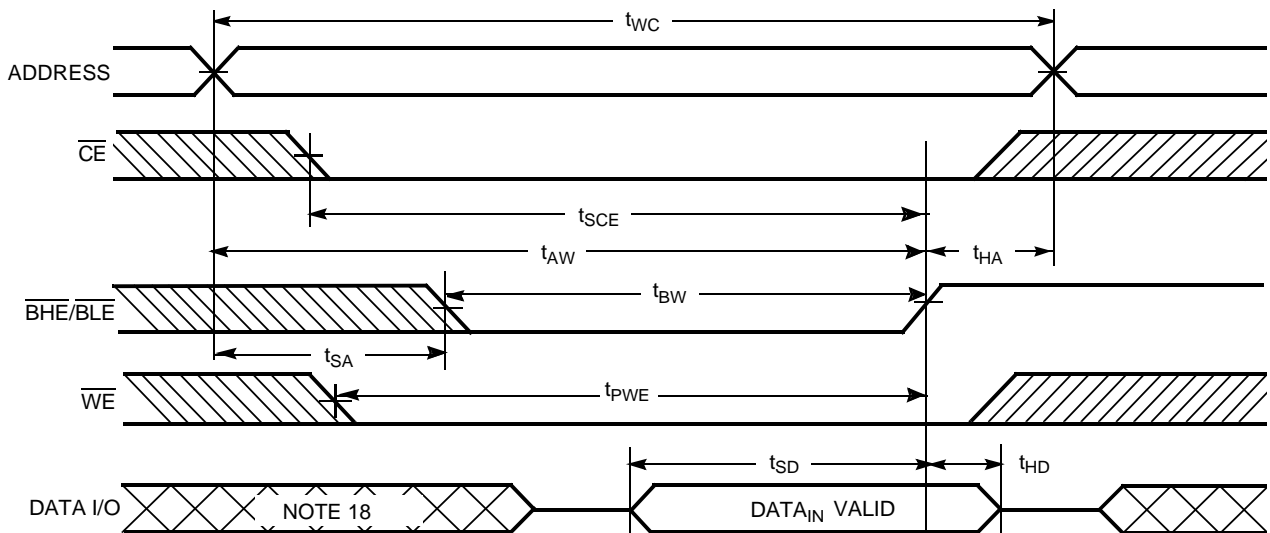
**Switching Waveforms**
**Read Cycle No. 1 (Address Transition Controlled)** <sup>[13, 14]</sup>

**Read Cycle No. 2 ( $\overline{\text{OE}}$  Controlled)** <sup>[14, 15]</sup>

**Notes:**

13. Device is continuously selected.  $\overline{\text{OE}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{\text{IL}}$ .
14. WE is HIGH for read cycle.
15. Address valid prior to or coincident with  $\overline{\text{CE}}$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 (WE Controlled)** <sup>[12, 16, 17]</sup>

**Write Cycle No. 2 ( $\overline{CE}$  Controlled)** <sup>[12, 16, 17]</sup>

**Notes:**

16. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
17. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
18. During this period, the I/Os are in output state and input signals should not be applied.

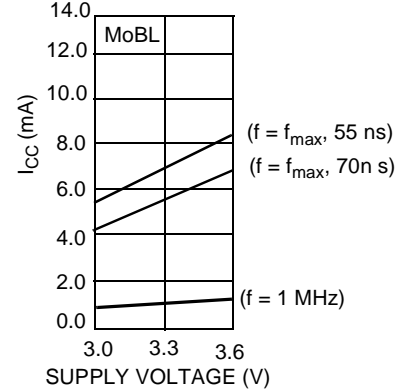
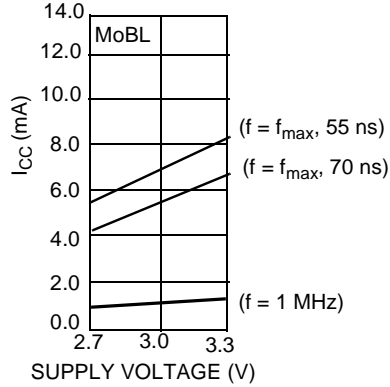
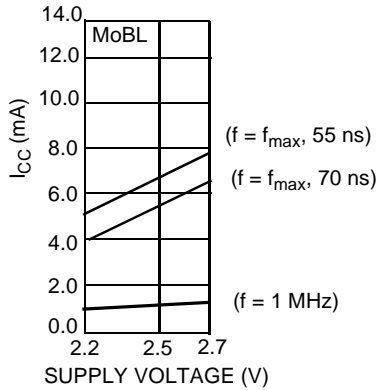


**Switching Waveforms (continued)**
**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[17]</sup>**

**Write Cycle No. 4 ( $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW)<sup>[17]</sup>**


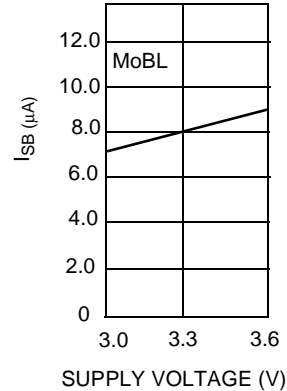
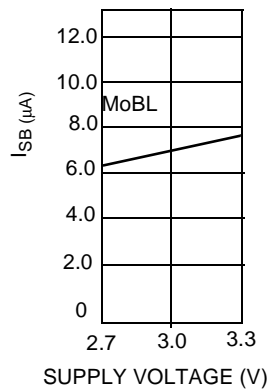
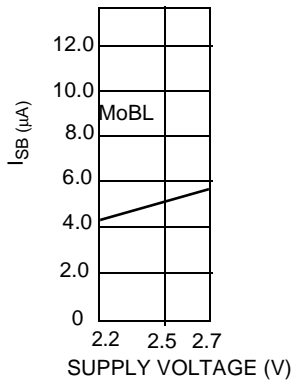
## Typical DC and AC Parameters

(Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ.)}$ ,  $T_A = 25^\circ\text{C}$ .)

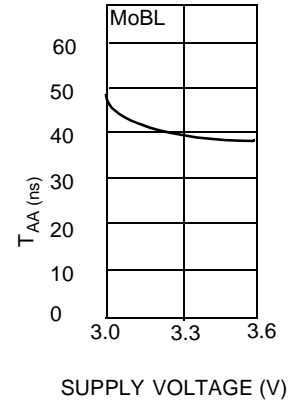
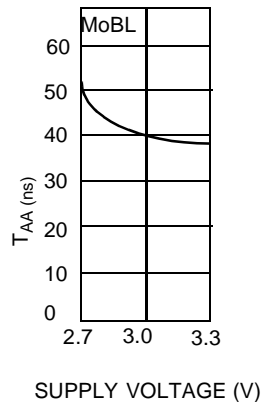
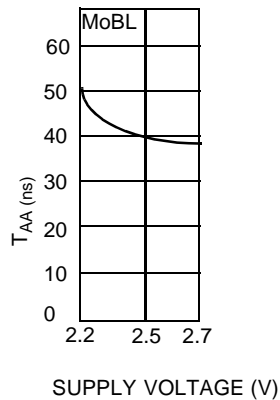
### Operating Current vs. Supply Voltage



### Standby Current vs. Supply Voltage



### Access Time vs. Supply Voltage



**Truth Table**

CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
X	X	X	H	H	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out (I/O <sub>0</sub> –I/O <sub>15</sub> )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out (I/O <sub>0</sub> –I/O <sub>7</sub> ); I/O <sub>8</sub> –I/O <sub>15</sub> in High Z	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out (I/O <sub>8</sub> –I/O <sub>15</sub> ); I/O <sub>0</sub> –I/O <sub>7</sub> in High Z	Read	Active ( $I_{CC}$ )
L	H	H	L	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	L	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In (I/O <sub>0</sub> –I/O <sub>15</sub> )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In (I/O <sub>0</sub> –I/O <sub>7</sub> ); I/O <sub>8</sub> –I/O <sub>15</sub> in High Z	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In (I/O <sub>8</sub> –I/O <sub>15</sub> ); I/O <sub>0</sub> –I/O <sub>7</sub> in High Z	Write	Active ( $I_{CC}$ )

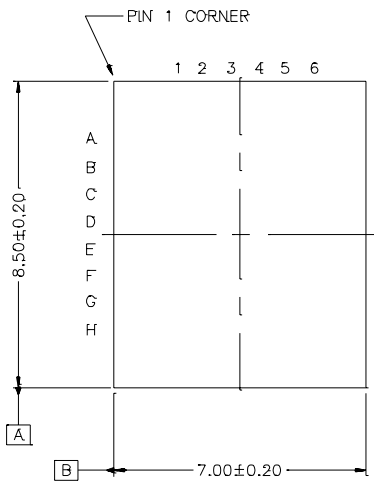
**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62147CV25LL-70BAI	BA48B	48-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	Industrial
	CY62147CV25LL-70BVI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62147CV30LL-70BAI	BA48B	48-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62147CV30LL-70BVI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62147CV33LL-70BAI	BA48B	48-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62147CV33LL-70BVI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
55	CY62147CV25LL-55BAI	BA48B	48-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	Industrial
	CY62147CV25LL-55BVI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62147CV30LL-55BAI	BA48B	48-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62147CV30LL-55BVI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62147CV33LL-55BAI	BA48B	48-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62147CV33LL-55BVI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	

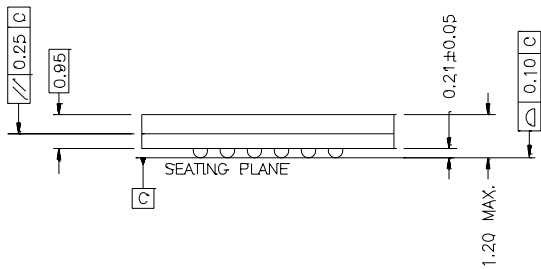
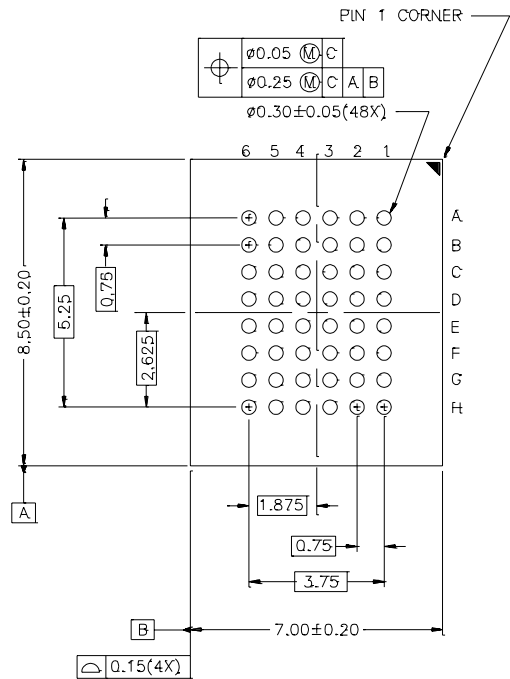
Package Diagrams

48-Ball (7.00 mm x 8.5 mm x 1.2 mm) Thin BGA BA48B

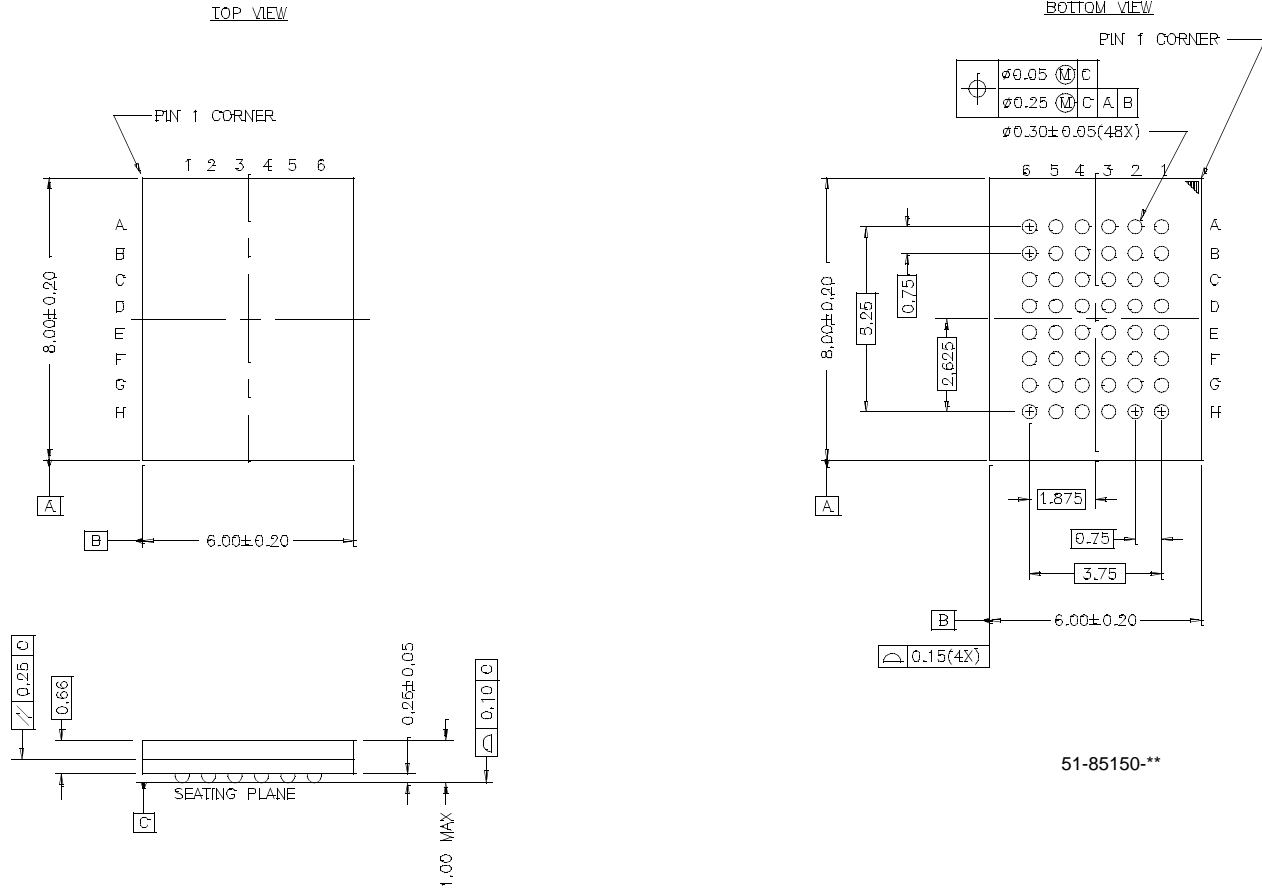
TOP VIEW



BOTTOM VIEW



51-85106-°C

**Package Diagrams (continued)**
**48-Lead VFBGA (6 mm x 8 mm x 1 mm) BV48A**


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<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	112394	01/31/02	GAV	Converted from Spec# 38-01123 to 38-05202. Advance Information to Final
*A	114216	05/01/02	MGN/GUG	Improved Typical & Max Icc values