



# 256K x 16 Static RAM

## Features

- Low voltage range:
  - CY62146V: 2.7V–3.6V
- Ultra-low active, standby power
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected
- CMOS for optimum speed/power

## Functional Description

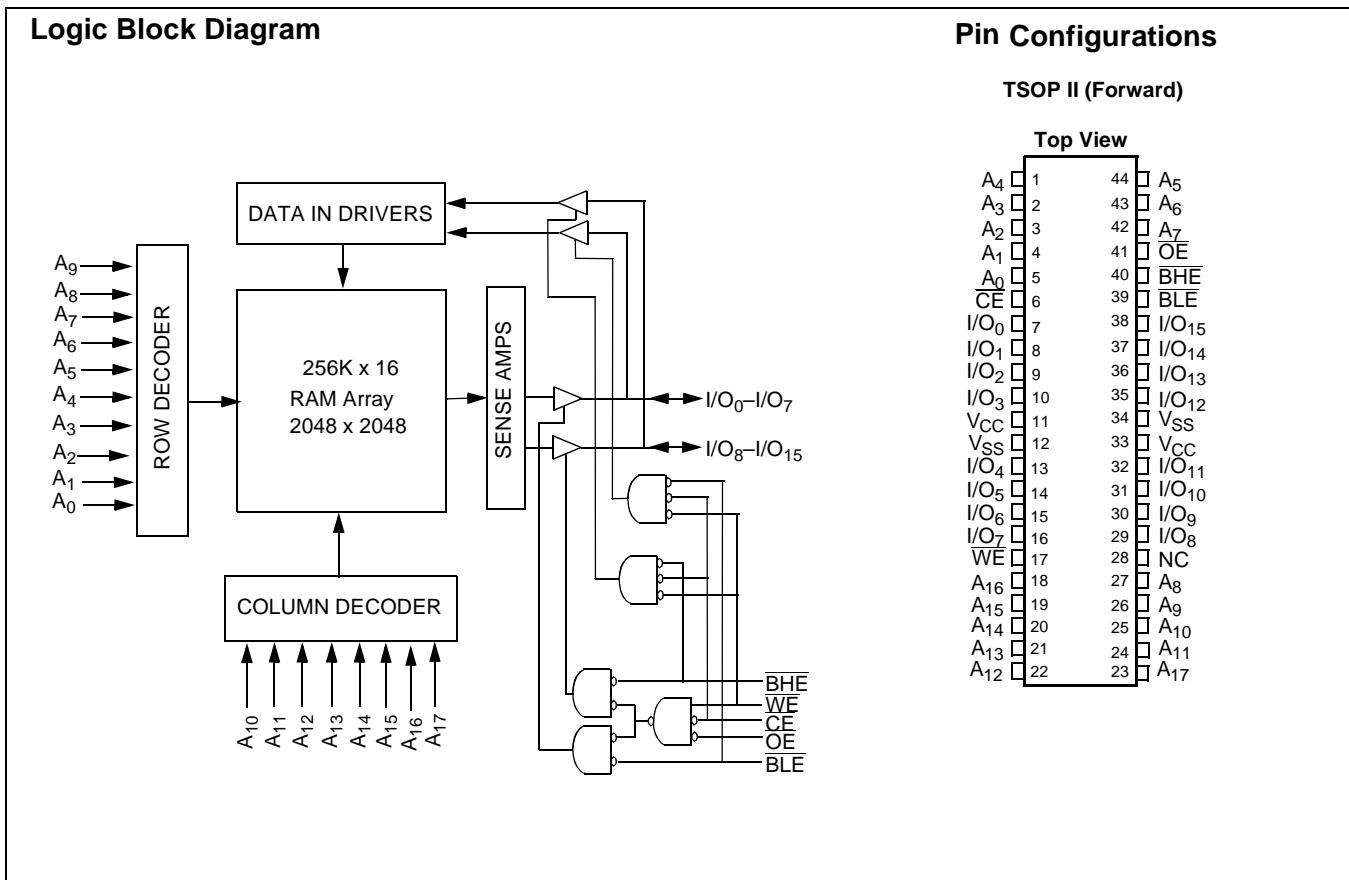
The CY62146V is a high-performance CMOS static RAM organized as 262,144 words by 16 bits. These devices feature advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ( $\overline{CE}$  HIGH). The input/output pins ( $I/O_0$  through

$I/O_{15}$ ) are placed in a high-impedance state when: deselected ( $\overline{CE}$  HIGH), outputs are disabled ( $\overline{OE}$  HIGH),  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

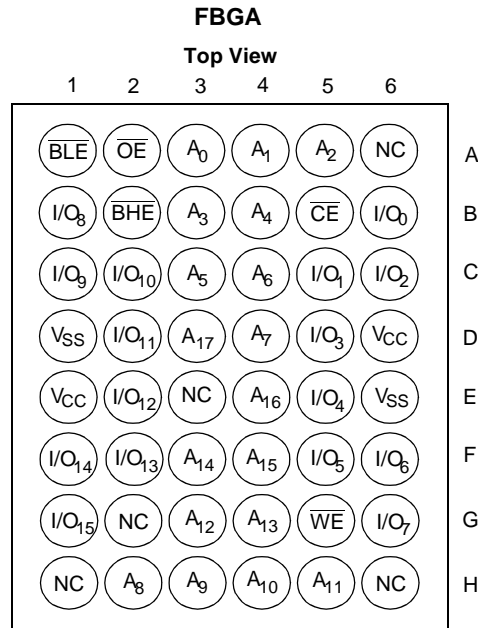
Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from  $I/O$  pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from  $I/O$  pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{17}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . See the truth table at the back of this data sheet for a complete description of read and write modes.

The CY62146V is available in 48-Ball FBGA and standard 44-Pin TSOP Type II (forward pinout) packaging.



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**Pin Configurations (continued)**

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied .....	-55°C to +125°C
Supply Voltage to Ground Potential .....	-0.5V to +4.6V
DC Voltage Applied to Outputs in High Z State <sup>[1]</sup> .....	-0.5V to V <sub>CC</sub> + 0.5V
DC Input Voltage <sup>[1]</sup> .....	-0.5V to V <sub>CC</sub> + 0.5V

Output Current into Outputs (LOW) .....	20 mA
Static Discharge Voltage .....	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current .....	>200 mA

**Operating Range**

Device	Range	Ambient Temperature	V <sub>CC</sub>
CY62146V	Industrial	-40°C to +85°C	2.7V to 3.6V

**Product Portfolio**

Product	V <sub>CC</sub> Range			Power	Power Dissipation (Industrial)			
	V <sub>CC</sub> (min.)	V <sub>CC</sub> (typ.) <sup>[2]</sup>	V <sub>CC</sub> (max.)		Operating (I <sub>CC</sub> )		Standby (I <sub>SB2</sub> )	
					Typ. <sup>[2]</sup>	Maximum	Typ. <sup>[2]</sup>	Maximum
CY62146V	2.7V	3.0V	3.6V	LL	7 mA	15 mA	2 μA	20 μA

**Notes:**

1. V<sub>IL(min.)</sub> = -2.0V for pulse durations less than 20 ns.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(yp.)</sub>; T<sub>A</sub> = 25°C.

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions		CY62146V			Unit
				Min.	Typ. <sup>[2]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 2.7V	2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA	V <sub>CC</sub> = 2.7V			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		V <sub>CC</sub> = 3.6V	2.2		V <sub>CC</sub> + 0.5V	V
V <sub>IL</sub>	Input LOW Voltage		V <sub>CC</sub> = 2.7V	-0.5		0.8	V
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1	±1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1	+1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , CMOS Levels	V <sub>CC</sub> = 3.6V		7	15	mA
		I <sub>OUT</sub> = 0 mA, f = 1 MHz, CMOS Levels			1	2	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , f = f <sub>MAX</sub>			2	20	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , f = 0	V <sub>CC</sub> = 3.6V	LL			

**Capacitance<sup>[3]</sup>**

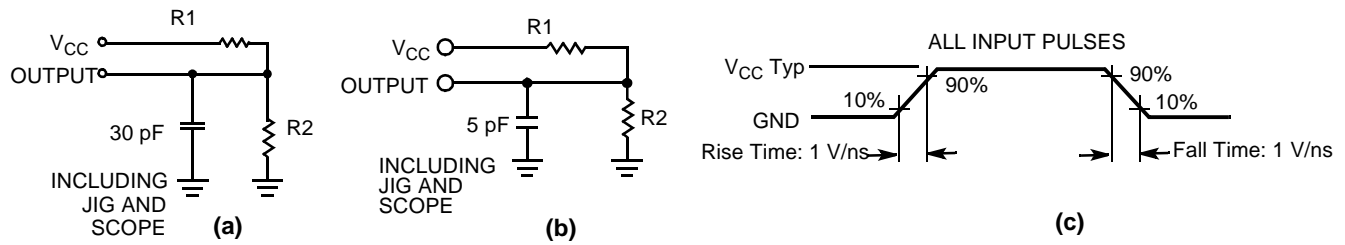
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC</sub> (typ.)	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**Thermal Resistance**

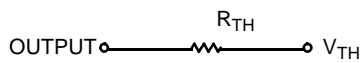
Description	Test Conditions	Symbol	BGA	TSOPII	Unit
Thermal Resistance (Junction to Ambient) <sup>[3]</sup>	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ <sub>JA</sub>	55	60	°C/W
Thermal Resistance (Junction to Case) <sup>[3]</sup>		Θ <sub>JC</sub>	16	22	°C/W

**Note:**

3. Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


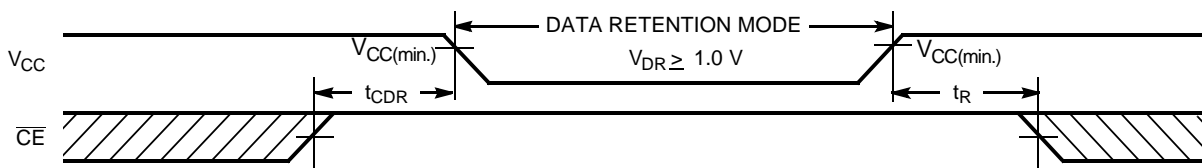
Equivalent to: THÉVENIN EQUIVALENT



Parameter	3.0V	Unit
R1	1105	$\Omega$
R2	1550	$\Omega$
R <sub>TH</sub>	645	$\Omega$
V <sub>TH</sub>	1.75	V

**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions	Min.	Typ. <sup>[2]</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention)		1.0		3.6	V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = 1.0V CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V No input may exceed V <sub>CC</sub> + 0.3V	LL	1	10	$\mu$ A
t <sub>CDR</sub> <sup>[3]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[4]</sup>	Operation Recovery Time		70			ns

**Data Retention Waveform**

**Note:**

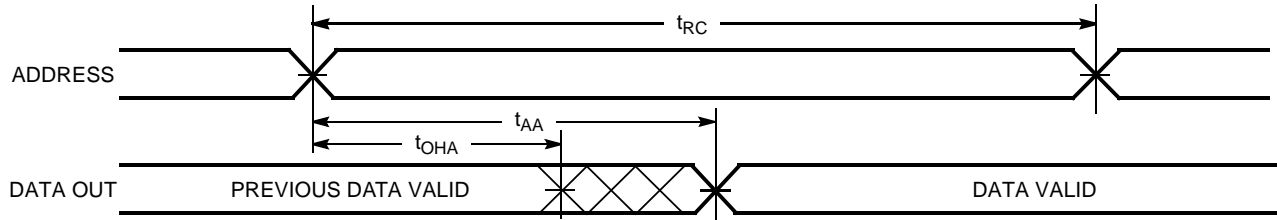
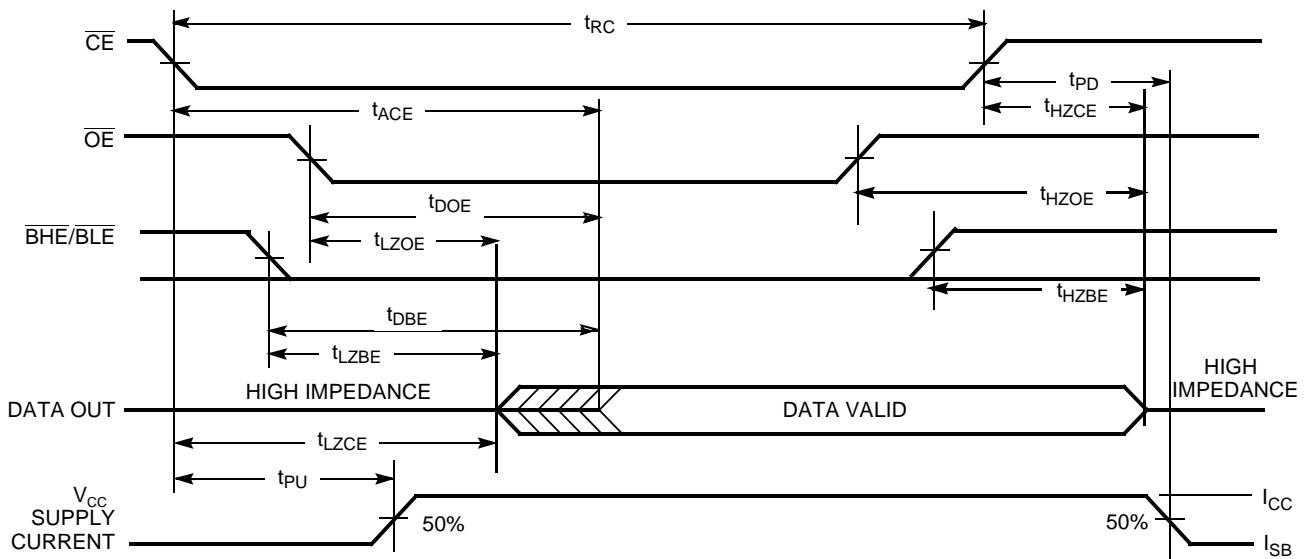
4. Full Device AC operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min.)</sub> ≥ 10  $\mu$ s or stable V<sub>CC(min.)</sub> ≥ 10  $\mu$ s.

**Switching Characteristics** Over the Operating Range<sup>[5]</sup>

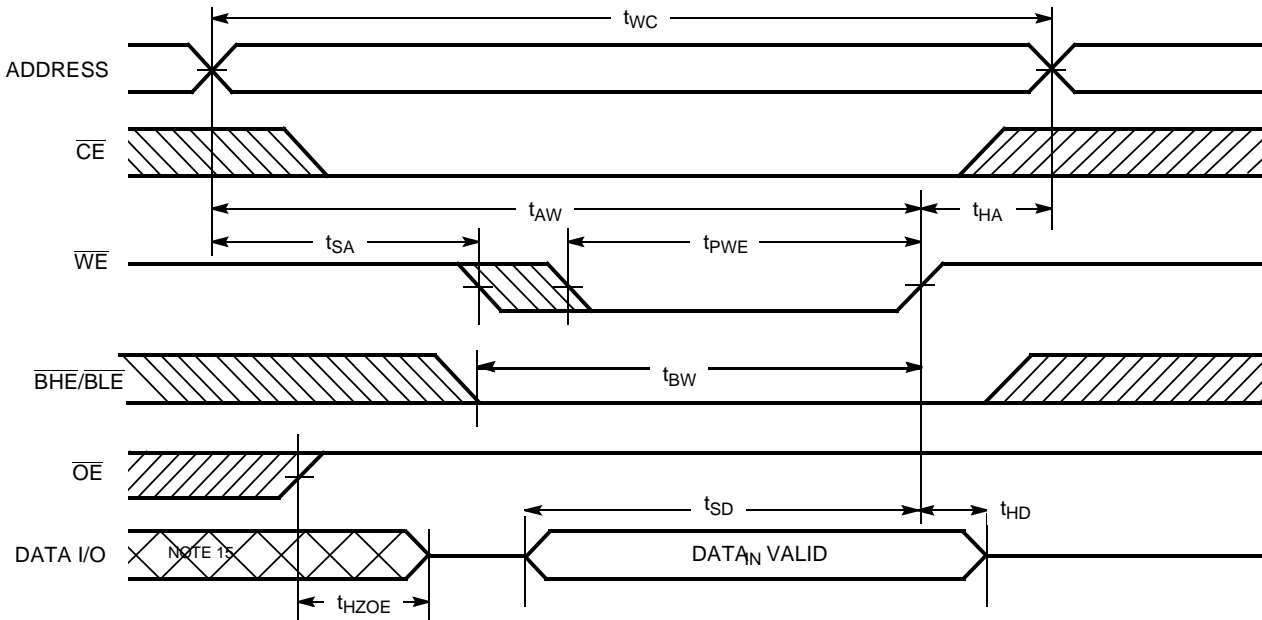
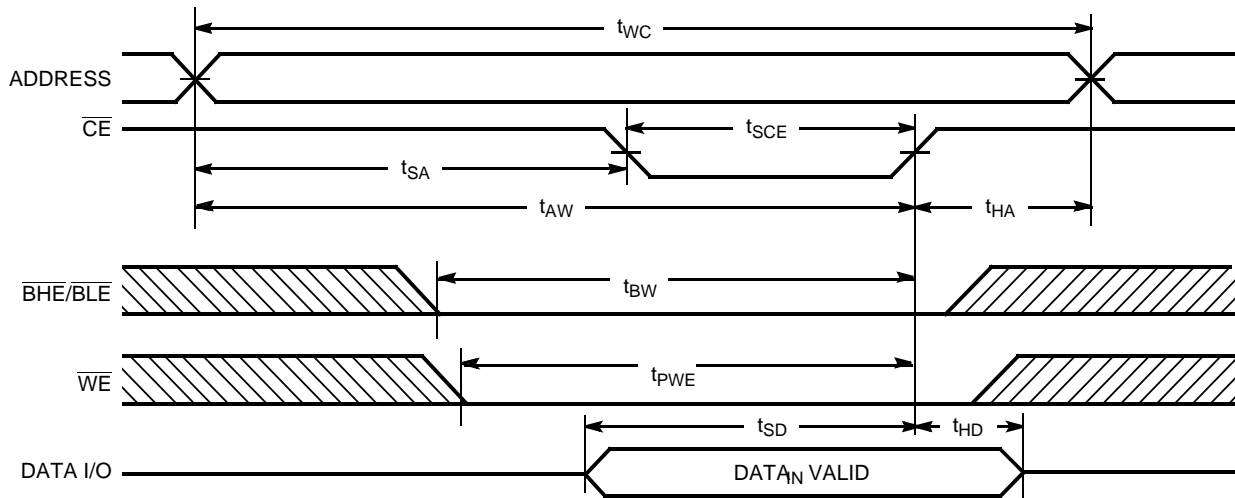
Parameter	Description	70 ns		Unit
		Min.	Max.	
<b>READ CYCLE</b>				
$t_{RC}$	Read Cycle Time	70		ns
$t_{AA}$	Address to Data Valid		70	ns
$t_{OHA}$	Data Hold from Address Change	10		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		70	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		25	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[6, 7]</sup>	5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[7]</sup>		20	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	10		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		20	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		70	ns
$t_{DBE}$	$\overline{BHE} / \overline{BLE}$ LOW to Data Valid		35	ns
$t_{LZBE}$	$\overline{BHE} / \overline{BLE}$ LOW to Low Z	5		ns
$t_{HZBE}$	$\overline{BHE} / \overline{BLE}$ HIGH to High Z		20	ns
<b>WRITE CYCLE<sup>[8, 9]</sup></b>				
$t_{WC}$	Write Cycle Time	70		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	60		ns
$t_{AW}$	Address Set-Up to Write End	60		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Set-Up to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	40		ns
$t_{BW}$	$\overline{BHE} / \overline{BLE}$ Pulse Width	60		ns
$t_{SD}$	Data Set-Up to Write End	30		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		25	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	10		ns

**Notes:**

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle #3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Switching Waveforms**
**Read Cycle No. 1** <sup>[10, 11]</sup>

**Read Cycle No. 2** <sup>[11, 12]</sup>

**Notes:**

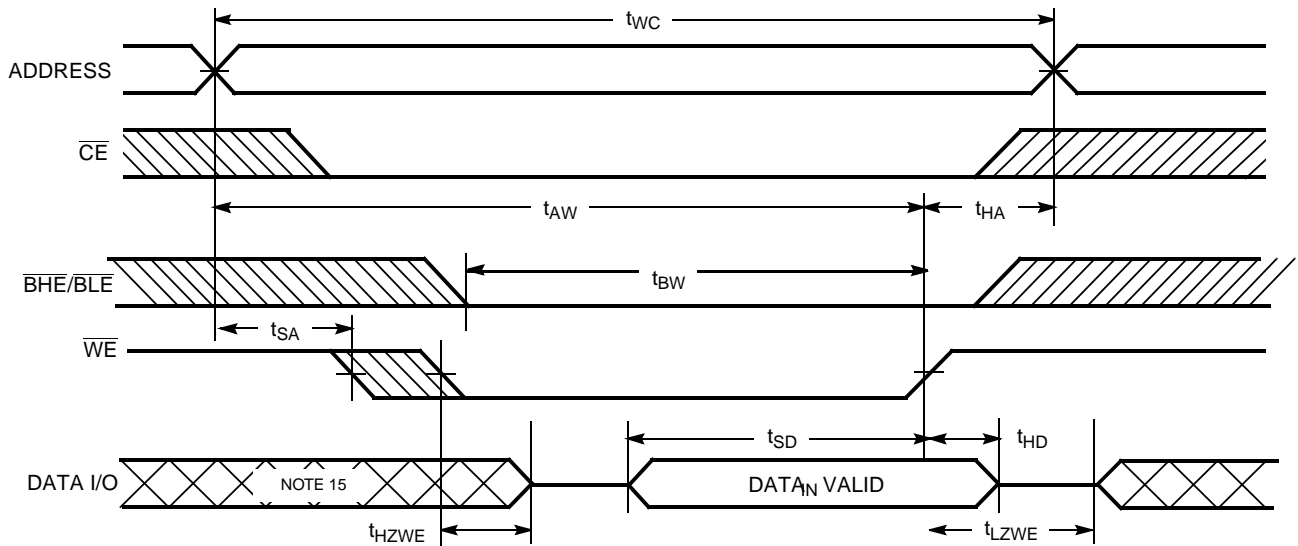
10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
11.  $\overline{WE}$  is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{WE}$  Controlled)** <sup>[8, 13, 14]</sup>

**Write Cycle No. 2 ( $\overline{CE}$  Controlled)** <sup>[8, 13, 14]</sup>

**Notes:**

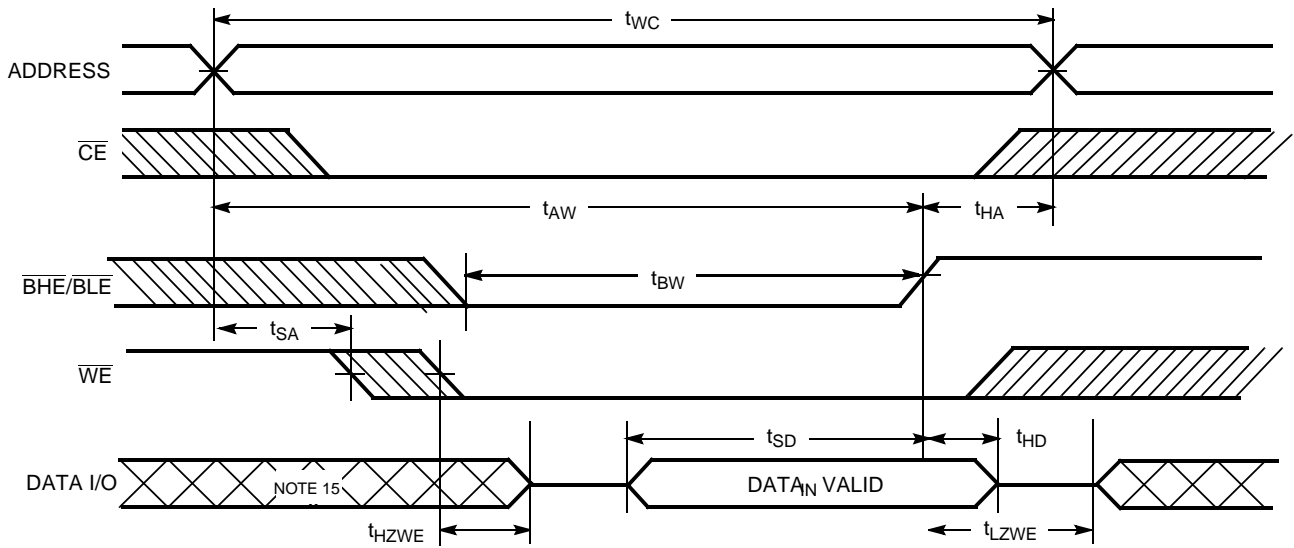
13. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
14. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

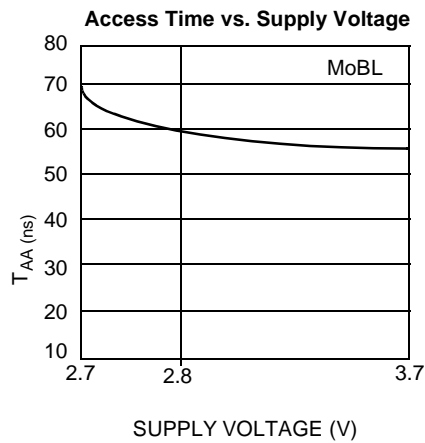
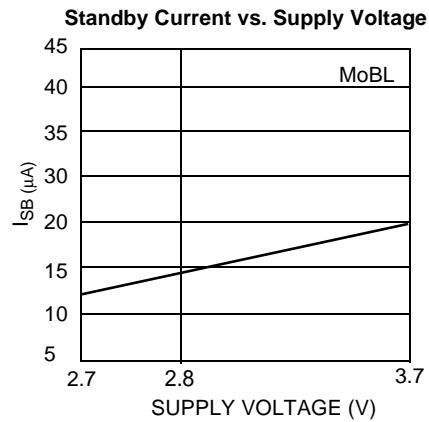
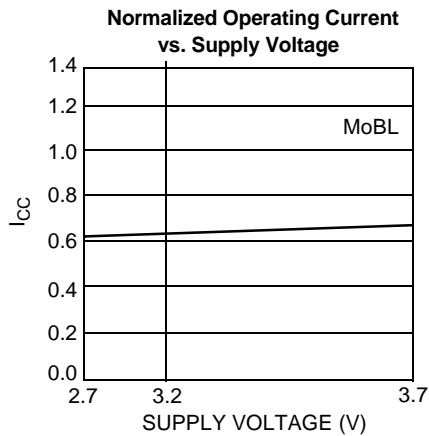
Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[9, 14]</sup>



Write Cycle No. 4 ( $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW)<sup>[15]</sup>





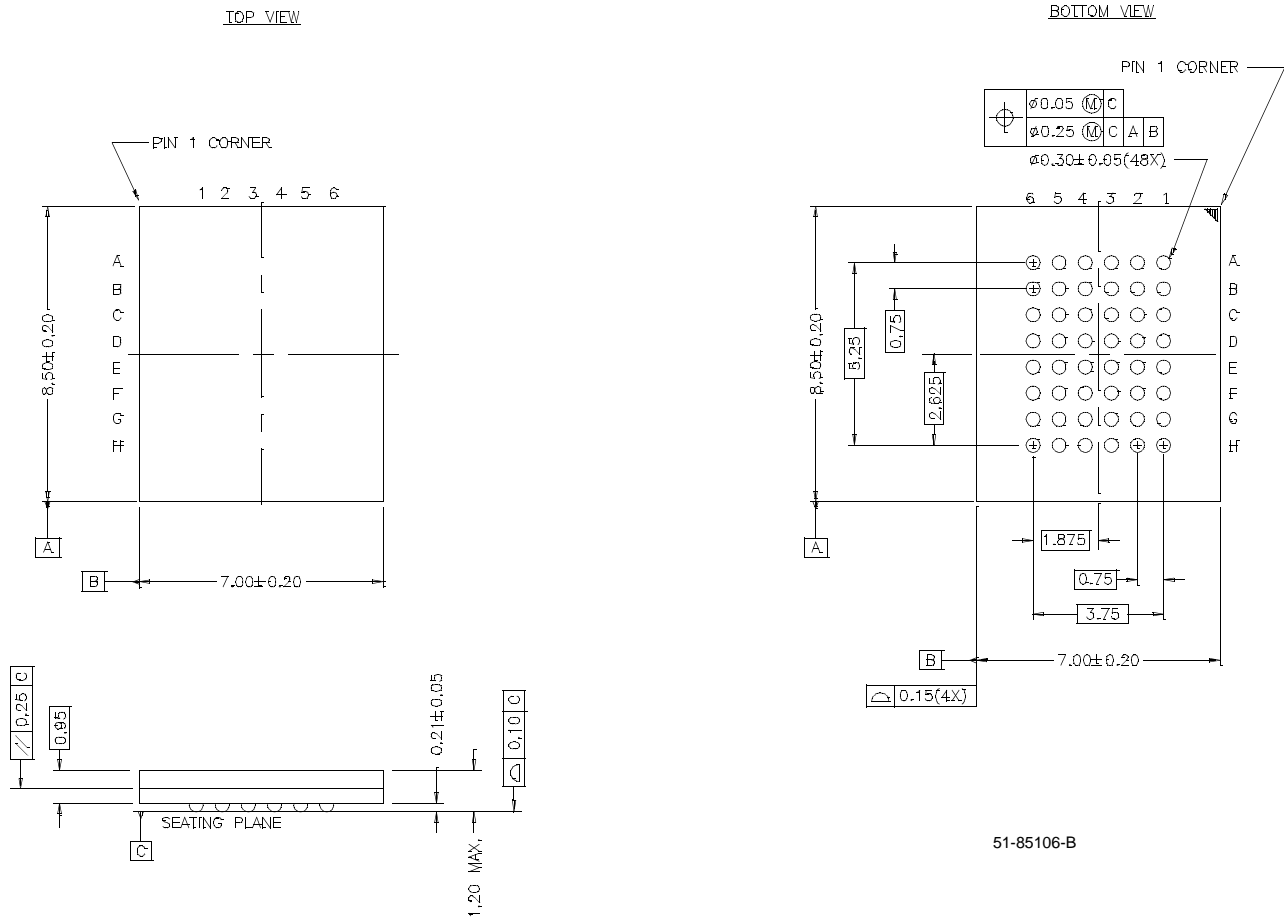
**Typical DC and AC Characteristics**

**Truth Table**

CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out (I/O <sub>0</sub> –I/O <sub>15</sub> )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out (I/O <sub>0</sub> –I/O <sub>7</sub> ); I/O <sub>8</sub> –I/O <sub>15</sub> in High Z	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out (I/O <sub>8</sub> –I/O <sub>15</sub> ); I/O <sub>0</sub> –I/O <sub>7</sub> in High Z	Read	Active ( $I_{CC}$ )
L	H	L	H	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	X	X	High Z	Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In (I/O <sub>0</sub> –I/O <sub>15</sub> )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In (I/O <sub>0</sub> –I/O <sub>7</sub> ); I/O <sub>8</sub> –I/O <sub>15</sub> in High Z	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In (I/O <sub>8</sub> –I/O <sub>15</sub> ); I/O <sub>0</sub> –I/O <sub>7</sub> in High Z	Write	Active ( $I_{CC}$ )
L	L	X	H	H	High Z	Output Disabled	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62146VLL-70ZI	Z44	44-Pin TSOP II	Industrial
	CY62146VLL-70BAI	BA48B	48-Ball Fine Pitch BGA	

Document #: 38-00647-\*E

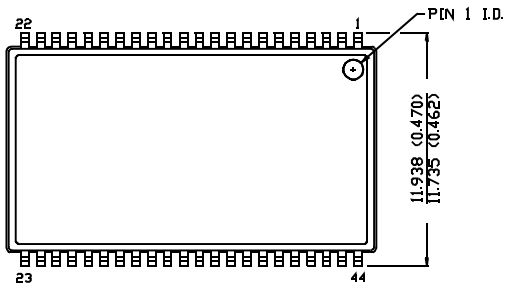
**Package Diagrams**
**48-Ball (7.00 mm x 8.50 mm x 1.20 mm) Fine Pitch BGA BA48B**


51-85106-B

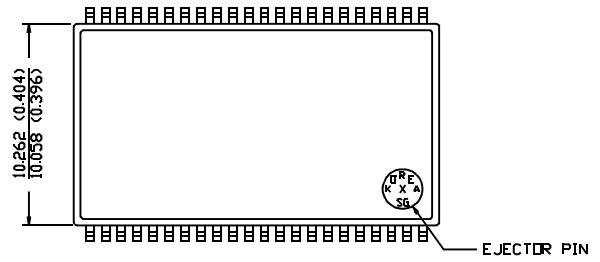
Package Diagrams (continued)

44-Pin TSOP II Z44

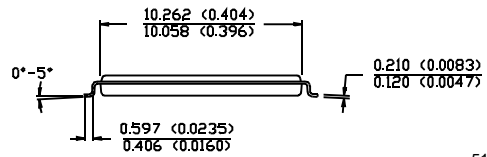
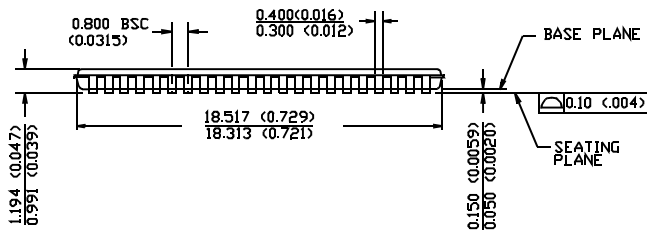
DIMENSION IN MM (INCH)  
MAX  
MIN.



TOP VIEW



BOTTOM VIEW



51-85087-A

**Revision History**

Document Title: CY62146V MoBL Document Number: 38-00647				
REV.	ECN NO.	ISSUE DATE	ORIG. OF CHANGE	DESCRIPTION OF CHANGE
**	2056	12/01/98	SKX	1. New Data Sheet
*A	2518	2/24/99	SKX	1. Changed the voltage range to 1.8V–3.6V 2. Removed the shading on LL version.
*B	2656	8/27/99	SKX	1. Split part into 62146V & 62146V18; shaded 62146V18 part 2. Speed bin 70 ns only 3. Make final
*C	2855	1/12/00	CXV	1. Add thermal resistance table 2. Change graphs on last page to include: I <sub>SS</sub> , I <sub>CC</sub> , T <sub>AA</sub> only
*D	3162	7/24/00	CXV	1. Separating MoBL/MoBL 2 2. Added 85 ns bin 3. Added Std. power bin
*E	3618	3/26/01	BCX	1. Package name change from BA49-BA48B 2. Dimension change from 7x 8.5 x 1.1 to 7 x 8.5 x 1.2 3. Typical DC and AC graphs changed