

256K x 16 Static RAM

Features

- **High speed:**
 - 55 ns and 70 ns availability
- **Voltage range:**
 - CY62146CV30: 2.7V – 3.3V
- **Pin compatible with CY62146V**
- **Ultra-low active power**
 - Typical active current: 1.5 mA @ f = 1 MHz
 - Typical active current: 5.5 mA @ f = f_{max} (70 ns speed)
- **Low standby power**
- **Easy memory expansion with \overline{CE} and \overline{OE} features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

Functional Description

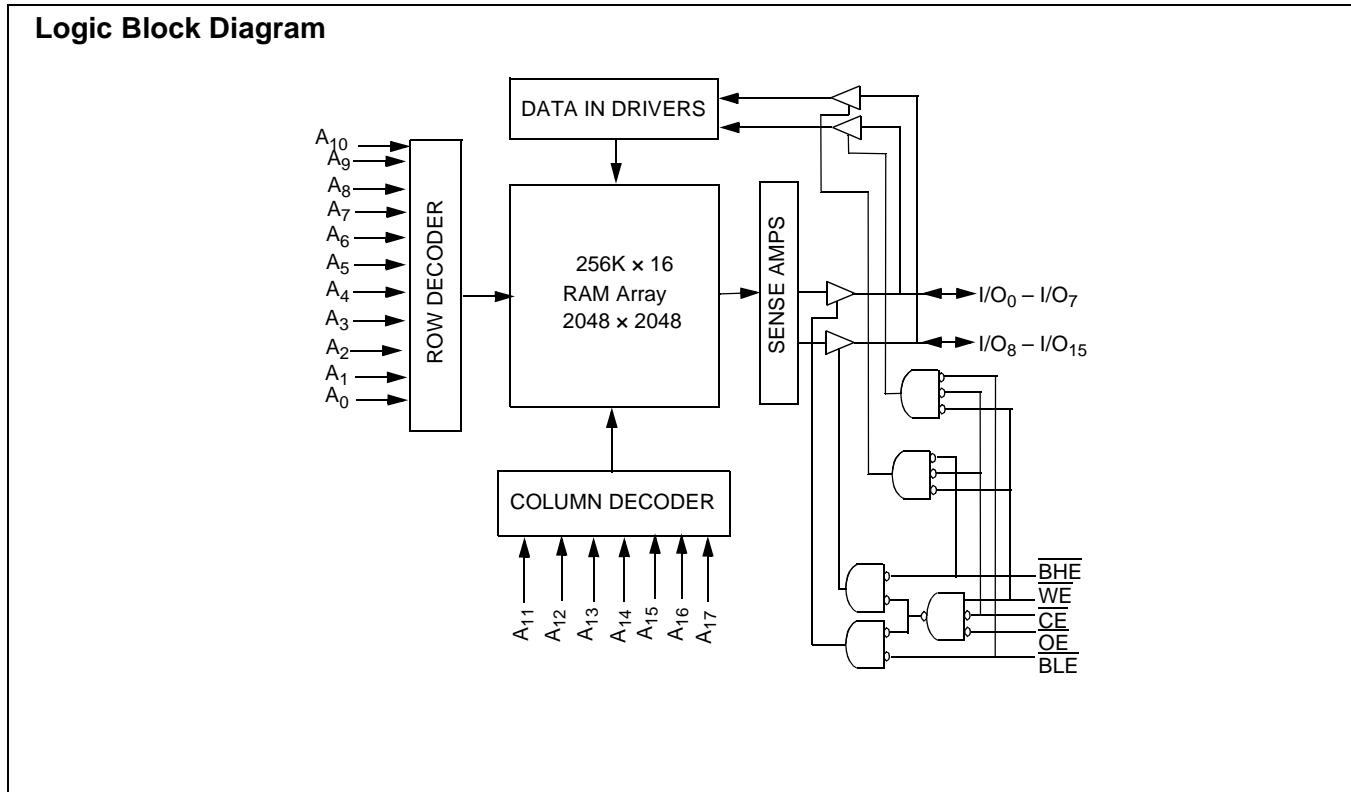
The CY62146CV30 is a high-performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces

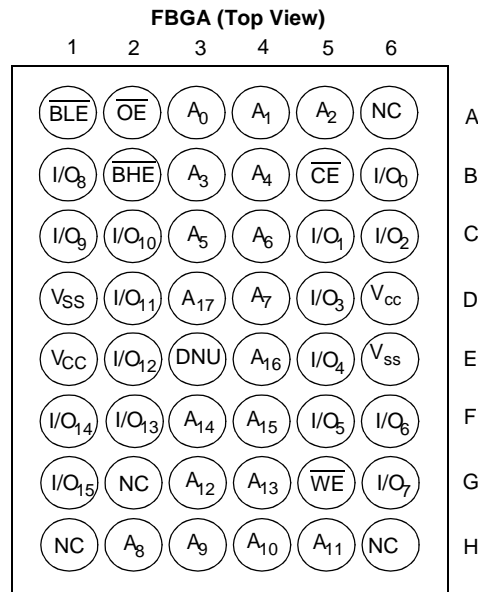
power consumption by 80% when addresses are not toggling. The device can also be put into standby mode reducing power consumption by 99% when deselected (\overline{CE} HIGH). The input/output pins (I/O_0 – I/O_{15}) are placed in a high-impedance state when: deselected (\overline{CE} HIGH), outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a Write operation (\overline{CE} LOW and \overline{WE} LOW).

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_0 – I/O_7), is written into the location specified on the address pins (A_0 – A_{17}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_8 – I/O_{15}) is written into the location specified on the address pins (A_0 – A_{17}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 – I/O_7 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the Truth Table on page 9 for a complete description of Read and Write modes.

The CY62146CV30 is available in 48-ball FBGA packaging.



Pin Configuration^[1,2]

Product Portfolio

Product	V _{CC} Range			Speed	Power Dissipation (Industrial)					
					Operating, I _{CC}				Standby (I _{SB2})	
	f = 1 MHz		f = f _{max}		Typ. ^[3]	Max.				
	Typ. ^[3]	Max.	Typ. ^[3]				Max.	Typ. ^[3]	Max.	
CY62146CV30	2.7V	3.0V	3.3V	55 ns	1.5 mA	3 mA	7 mA	15 mA	7 μA	15 μA
				70 ns	1.5 mA	3 mA	5.5 mA	12 mA		

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied..... -55°C to +125°C

Supply Voltage to Ground Potential ... -0.5V to V_{CCmax} + 0.5V

DC Voltage Applied to Outputs

in High-Z State^[4] -0.5V to V_{CC} + 0.5V

DC Input Voltage^[4]..... -0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage > 2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current > 200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC}
CY62146CV30	Industrial	-40°C to +85°C	2.7V to 3.3V

Notes:

1. NC pins are not connected to the die.
2. E3 (DNU) can be left as NC or V_{SS} to ensure proper application.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25°C.
4. V_{IL(min.)} = -2.0V for pulse durations less than 20 ns.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62146CV30-55			CY62146CV30-70			Unit
			Min.	Typ. ^[3]	Max.	Min.	Typ. ^[3]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -1.0 mA V _{CC} = 2.7V	2.4			2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 2.1mA V _{CC} = 2.7V			0.4			0.4	V
V _{IH}	Input HIGH Voltage		2.2		V _{CC} + 0.3V	1.8		V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage		-0.3		0.8	-0.3		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-1		+1	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC} V _{CC} = 3.3V I _{OUT} = 0 mA CMOS Levels		7	15		5.5	12	mA
		f = 1 MHz		1.5	3		1.5	3	
I _{SB1}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = f _{max} (Address and Data Only), f=0 (OE, WE, BHE and BLE)		7	15		7	15	μA
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = 0, V _{CC} =3.3V							

Capacitance^[5]

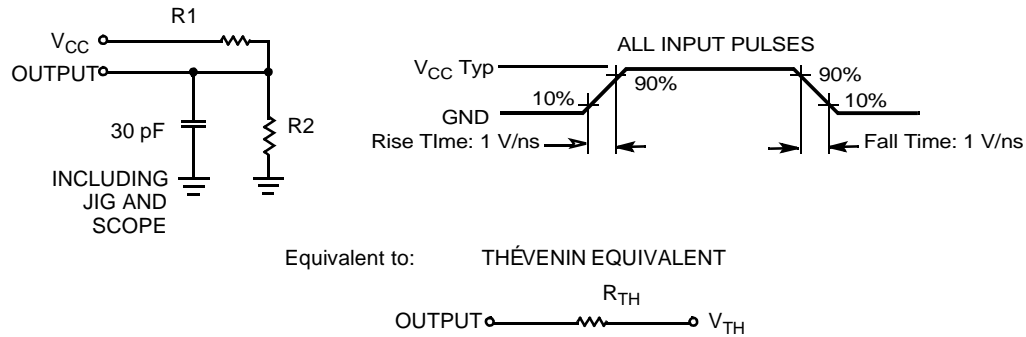
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC} (typ.)	6	pF
C _{OUT}	Output Capacitance		8	pF

Thermal Resistance

Description	Test Conditions	Symbol	BGA	Units
Thermal Resistance (Junction to Ambient) ^[5]	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	Θ _{JA}	55	°C/W
Thermal Resistance (Junction to Case) ^[5]		Θ _{JC}	16	°C/W

Note:

- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms


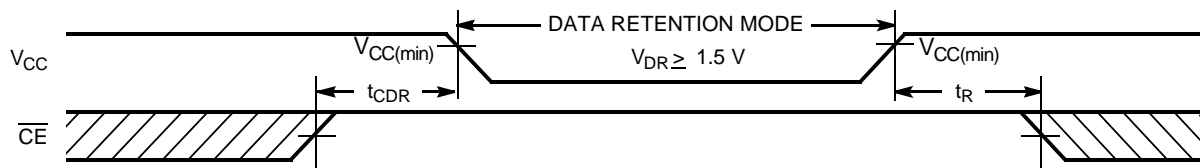
Parameters	3.0V	Unit
R1	1.105	K Ohms
R2	1.550	K Ohms
R _{TH}	0.645	K Ohms
V _{TH}	1.75V	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[3]	Max.	Unit
V _{DR}	V _{CC} for Data Retention		1.5		V _{CCmax}	V
I _{CCDR}	Data Retention Current	V _{CC} = 1.5V CE ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V		3	10	μA
t _{CDR} ^[5]	Chip Deselect to Data Retention Time		0			ns
t _R ^[6]	Operation Recovery Time		t _{RC}			ns

Note:

6. Full device AC operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min.)} > 100 μs or stable at V_{CC(min.)} > 100 μs.

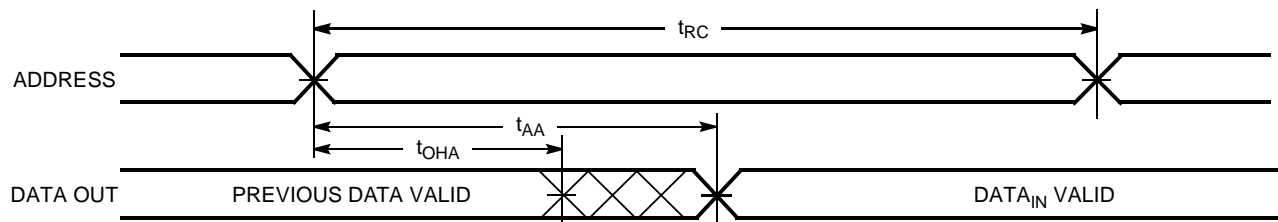
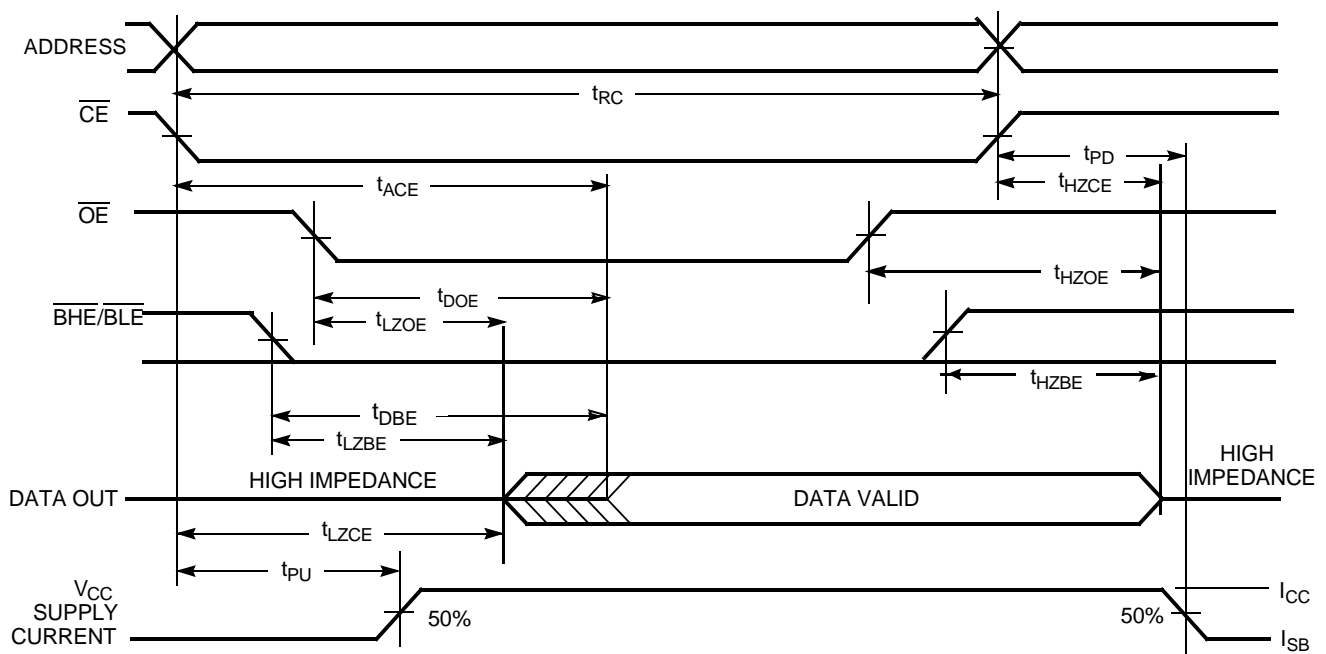
Data Retention Waveform


Switching Characteristics Over the Operating Range^[7]

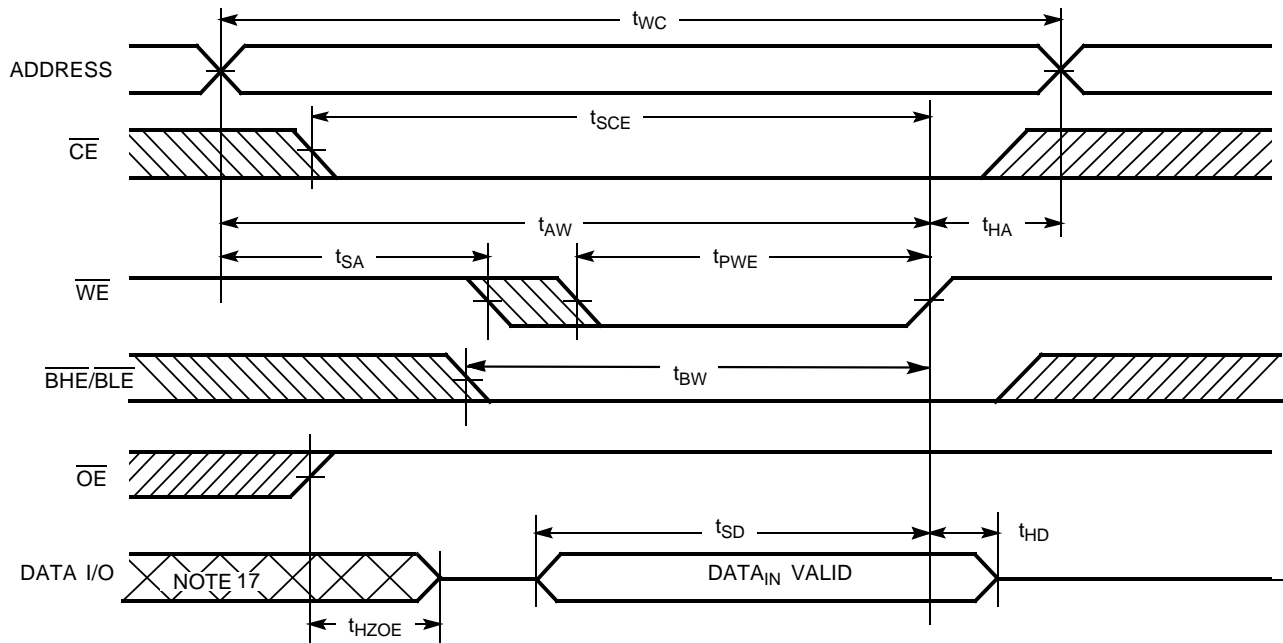
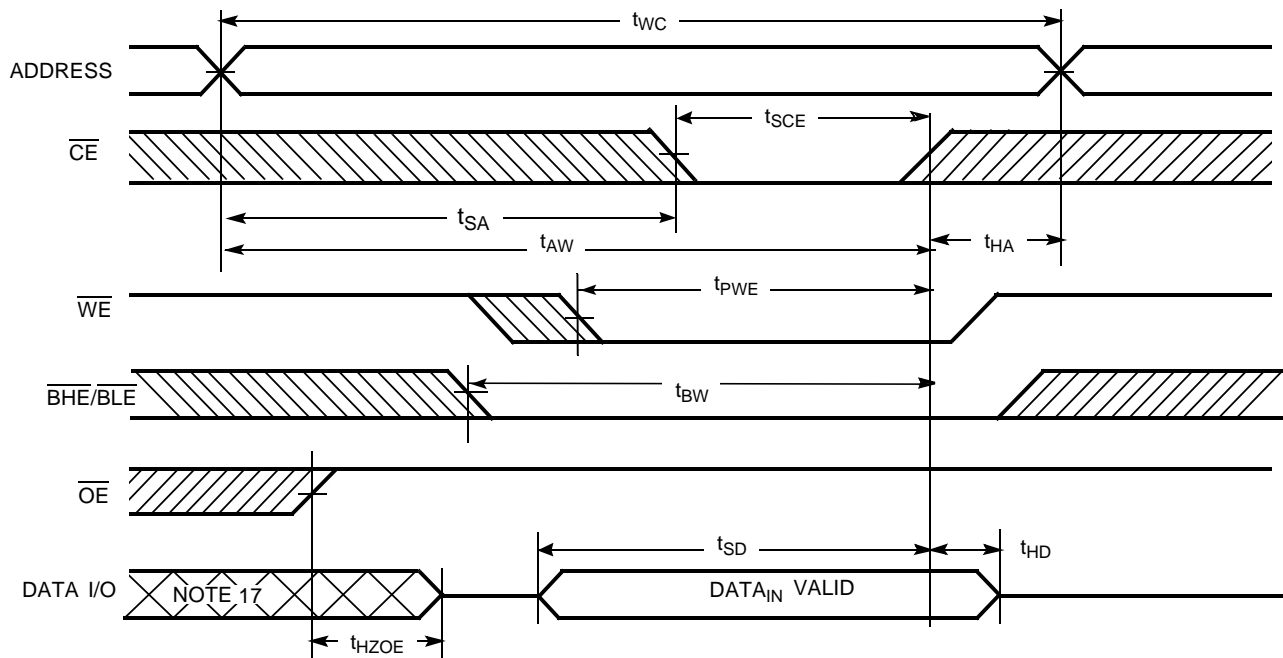
Parameter	Description	55		70		Unit
		Min	Max	Min	Max	
READ CYCLE						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	\overline{CE} LOW to Data Valid		55		70	ns
t_{DOE}	\overline{OE} LOW to Data Valid		25		35	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[8]	5		5		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[8,10]		20		25	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[8]	10		10		ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[8,10]		20		25	ns
t_{PU}	\overline{CE} LOW to Power-Up	0		0		ns
t_{PD}	\overline{CE} HIGH to Power-Down		55		70	ns
t_{DBE}	$\overline{BHE}/\overline{BLE}$ LOW to Data Valid		25		35	ns
$t_{LZBE}^{[9]}$	$\overline{BHE}/\overline{BLE}$ LOW to Low Z	5		5		ns
t_{HZBE}	$\overline{BHE}/\overline{BLE}$ HIGH to High Z		20		25	ns
WRITE CYCLE^[11]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	\overline{CE} LOW to Write End	45		60		ns
t_{AW}	Address Set-Up to Write End	45		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	\overline{WE} Pulse Width	45		50		ns
t_{BW}	$\overline{BHE}/\overline{BLE}$ Pulse Width	50		60		ns
t_{SD}	Data Set-Up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[8,10]		20		25	ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[8]	5		5		ns

Notes:

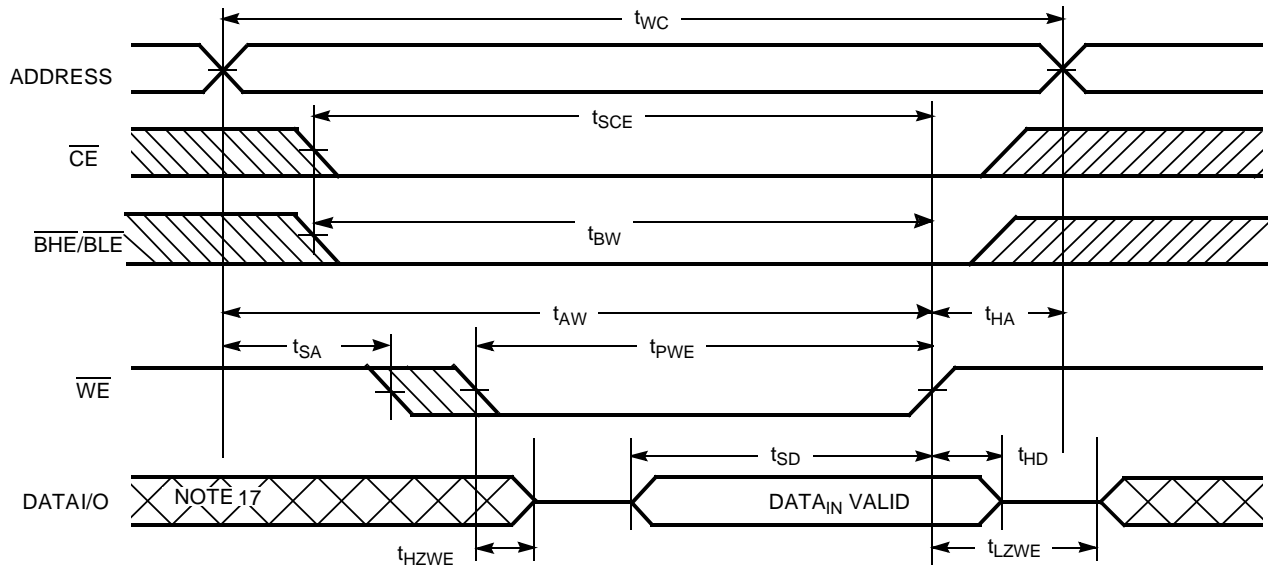
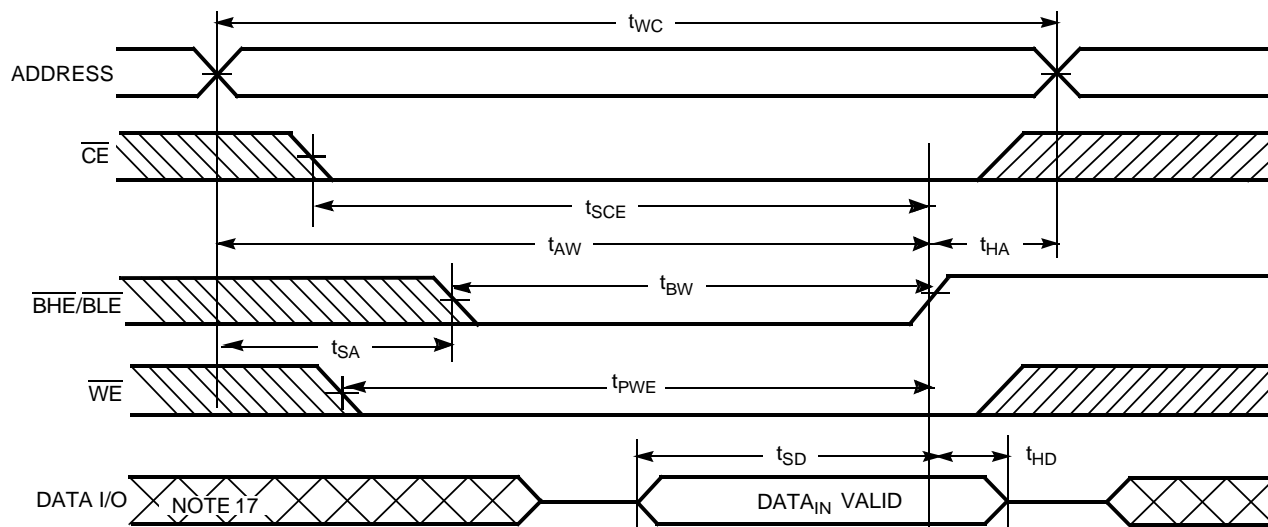
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- If both byte enables are toggled together, this value is 10 ns.
- t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
- The internal Write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a Write and any of these signals can terminate a Write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the Write.

Switching Waveforms
Read Cycle 1 (Address Transition Controlled) [12,13]

Read Cycle 2 ($\overline{\text{OE}}$ Controlled) [13,14]

Notes:

12. Device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}} = V_{\text{IL}}$, $\overline{\text{BHE}}$, $\overline{\text{BLE}} = V_{\text{IL}}$.
13. WE is HIGH for Read cycle.
14. Address valid prior to or coincident with $\overline{\text{CE}}$, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$ transition LOW.

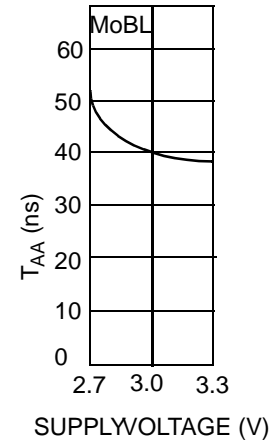
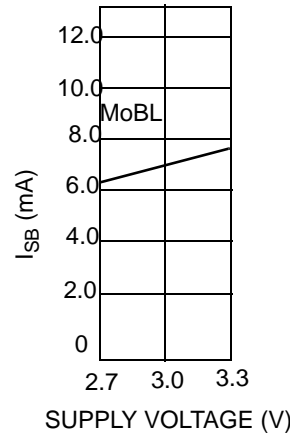
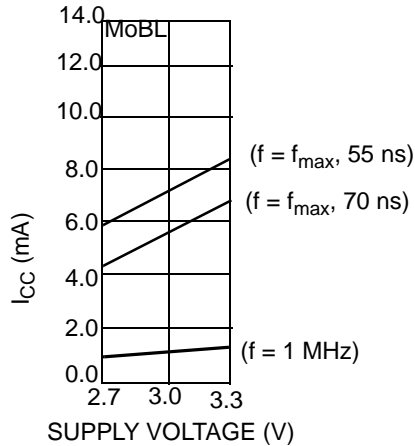
Switching Waveforms (continued)
Write Cycle 1 ($\overline{\text{WE}}$ Controlled) ^[11, 15, 16]

Write Cycle 2 ($\overline{\text{CE}}$ Controlled) ^[11, 15, 16]

Notes:

15. Data I/O is high-impedance if $\overline{\text{OE}} = V_{\text{IH}}$.
16. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)
Write Cycle 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[16]

Write Cycle 4 ($\overline{\text{BHE/BLE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[16]


Typical DC and AC Parameters

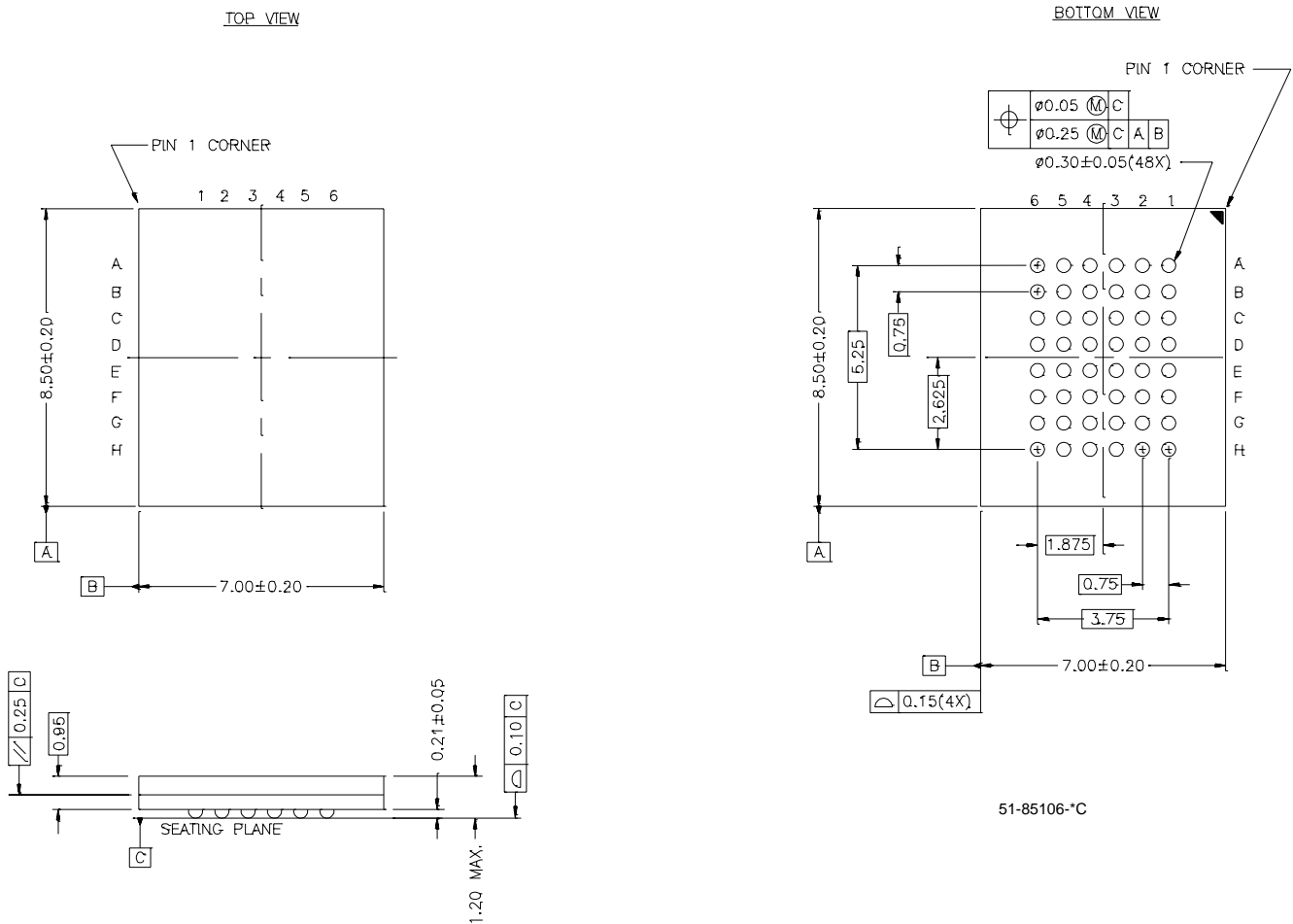
(Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25^\circ\text{C}$.)

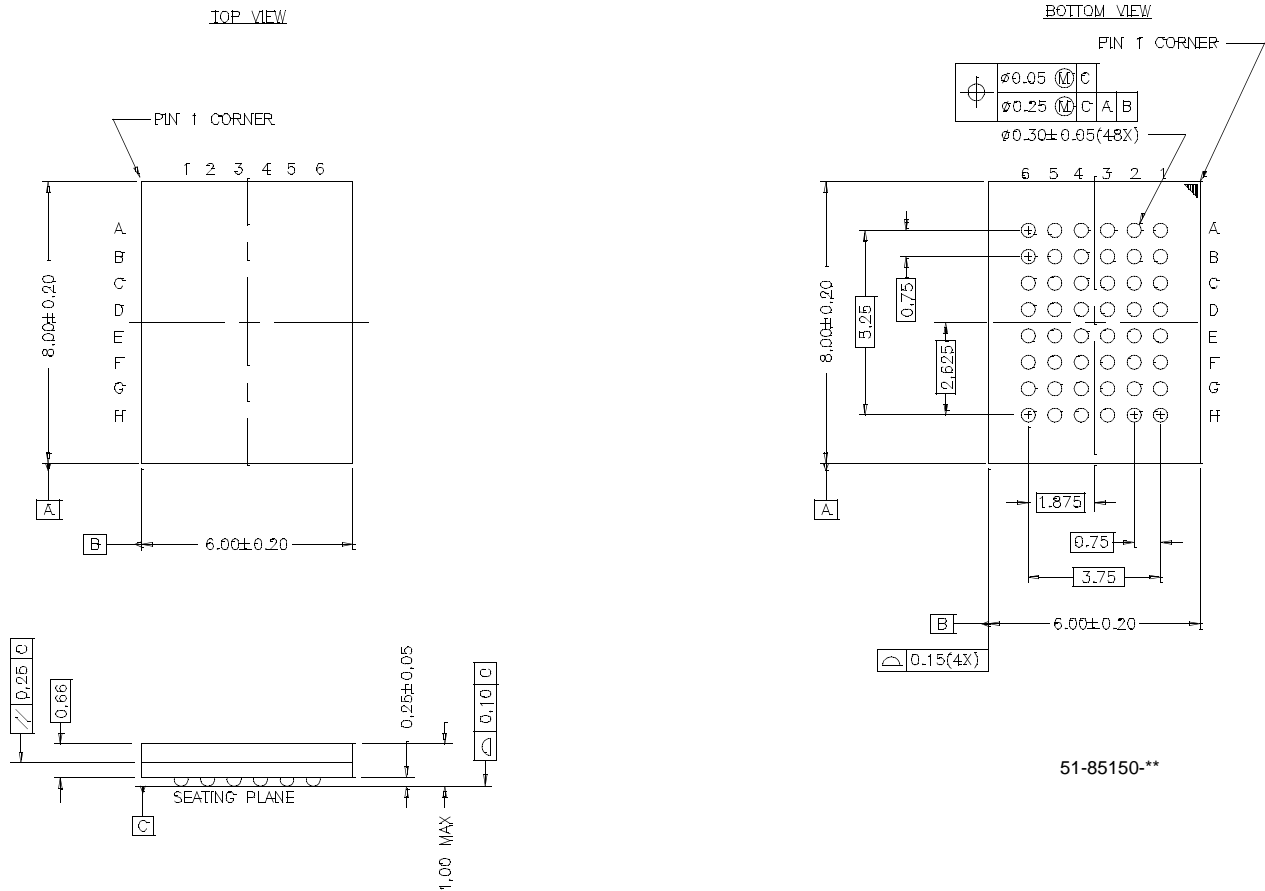
Operating Current vs. Supply Voltage Standby Current vs. Supply Voltage Access Time vs. Supply Voltage

Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	X	X	H	H	High Z	Output Disabled	Active (I_{CC})
L	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62146CV30LL-70BAI	BA48B	48-ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	Industrial
	CY62146CV30LL-70BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
55	CY62146CV30LL-55BAI	BA48B	48-ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62146CV30LL-55BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	

Package Diagrams
48-Ball (7.00 mm x 8.5 mm x 1.2 mm) Thin BGA BA48B


Package Diagrams (continued)
48-ball (6.0 mm × 8.0 mm × 1.0 mm) Fine Pitch BGA BV48A


51-85150-**

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Document Title: CY62146CV30 MoBL™ 256K x 16 Static RAM Document Number: 38-05203				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	112395	01/18/02	GAV	New Data Sheet
*A	114217	05/01/02	MGN/ GUG	Improved Typical & Max Icc values.