



2M (256K x 8) Static RAM

Features

- **Very high speed: 55 ns and 70 ns**
- **Voltage range:**
 - CY62138CV25: 2.2V–2.7V
 - CY62138CV30: 2.7V–3.3V
 - CY62138CV33: 3.0V–3.6V
 - CY62138CV: 2.7V–3.6V
- **Pin-compatible with CY62138V**
- **Ultra low active power**
 - Typical active current: 1.5 mA @ f = 1 MHz
 - Typical active current: 5.5 mA @ f = f_{max} (70-ns speed)
- **Low standby power**
- **Easy memory expansion with \overline{CE}_1 , \overline{CE}_2 , and \overline{OE} features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Packages offered in a 36-ball FBGA**

Functional Description^[1]

The CY62138CV25/30/33 and CY62138CV are high-performance CMOS static RAMs organized as 256K words by eight

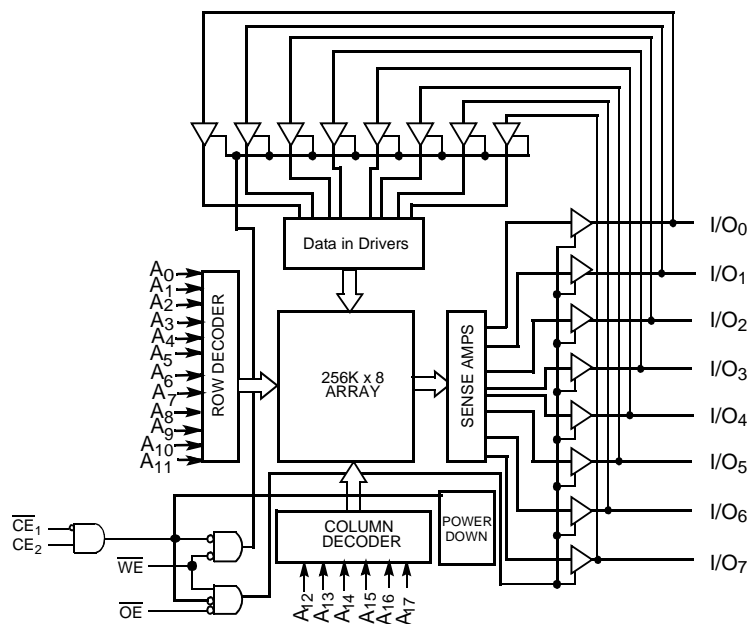
bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL[®]) in portable applications. The device also has an automatic power-down feature that significantly reduces power consumption by 80% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected (\overline{CE}_1 HIGH or \overline{CE}_2 LOW).

Writing to the device is accomplished by taking Chip Enable 1 (\overline{CE}_1) and Write Enable (\overline{WE}) inputs LOW and Chip Enable 2 (\overline{CE}_2) HIGH. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₇).

Reading from the device is accomplished by taking Chip Enable 1 (\overline{CE}_1) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) and Chip Enable 2 (\overline{CE}_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

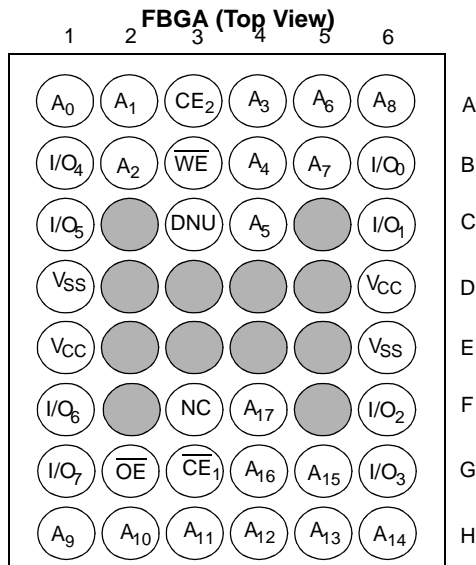
The eight input/output pins (I/O₀ through I/O₇) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 HIGH or \overline{CE}_2 LOW), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE}_1 LOW, \overline{CE}_2 HIGH and \overline{WE} LOW). See the truth table at the back of this data sheet for a complete description of read and write modes.

Logic Block Diagram



Note:

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Pin Configuration ^[2, 3]

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied 55°C to +125°C

Supply Voltage to Ground Potential ... -0.5V V_{CCMAX} + 0.5V

DC Voltage Applied to Outputs in High-Z State^[4] 0.5V to V_{CC} + 0.3V

DC Input Voltage^[4] -0.5V to V_{CC} + 0.3V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current > 200 mA

Operating Range

Product	Range	Ambient Temperature T _A	V _{CC}
CY62138CV25	Industrial	-40°C to +85°C	2.2V to 2.7V
CY62138CV30			2.7V to 3.3V
CY62138CV33			3.0V to 3.6V
CY62138CV			2.7V to 3.6V

Product Portfolio

Product	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating, I _{CC} (mA)				Standby, I _{SB2} (μA)	
	Min.	Typ. ^[5]	Max.		f = 1 MHz		f = f _{max}		Typ. ^[5]	Max.
					Typ. ^[5]	Max.	Typ. ^[5]	Max.		
CY62138CV25LL	2.2	2.5	2.7	55	1.5	3	7	15	2	10
				70	1.5	3	5.5	12		
CY62138CV30LL	2.7	3.0	3.3	55	1.5	3	7	15	2	10
				70	1.5	3	5.5	12		
CY62138CV33LL	3.0	3.3	3.6	55	1.5	3	7	15	5	15
				70	1.5	3	5.5	12		
CY62138CVLL	2.7	3.3	3.6	70	1.5	3	5.5	12	5	15

Notes:

2. NC pins are not connected to the die.
3. C3 (DNU) can be left as NC or V_{SS} to ensure proper application.
4. V_{L(min.)} = -2.0V for pulse durations less than 20 ns.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25°C.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62138CV25-55			CY62138CV25-70			Unit
			Min.	Typ. ^[5]	Max.	Min.	Typ. ^[5]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA V _{CC} = 2.2V	2.0			2.0			V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA V _{CC} = 2.2V			0.4			0.4	V
V _{IH}	Input HIGH Voltage		1.8		V _{CC} + 0.3V	1.8		V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage		-0.3		0.6	-0.3		0.6	V
I _{Ix}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-1		+1	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC}		7	15		5.5	12	mA
		f = 1 MHz		1.5	3		1.5	3	
I _{SB1}	Automatic CE Power-down Current — CMOS Inputs	CE ₁ ≥ V _{CC} - 0.2V or CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = f _{max} (Address and Data Only), f = 0 (OE, WE)		2	10		2	10	μA
I _{SB2}	Automatic CE Power-down Current — CMOS Inputs	CE ₁ ≥ V _{CC} - 0.2V or CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0, V _{CC} = 2.7V							

Parameter	Description	Test Conditions	CY62138CV30-55			CY62138CV30-70			Unit
			Min.	Typ. ^[5]	Max.	Min.	Typ. ^[5]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -1.0 mA V _{CC} = 2.7V	2.4			2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA V _{CC} = 2.7V			0.4			0.4	V
V _{IH}	Input HIGH Voltage		2.2		V _{CC} + 0.3V	2.2		V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage		-0.3		0.8	-0.3		0.8	V
I _{Ix}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-1		+1	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC}		7	15		5.5	12	mA
		f = 1 MHz		1.5	3		1.5	3	
I _{SB1}	Automatic CE Power-down Current — CMOS Inputs	CE ₁ ≥ V _{CC} - 0.2V or CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = f _{max} (Address and Data Only), f = 0 (OE, WE)		2	10		2	10	μA
I _{SB2}	Automatic CE Power-down Current — CMOS Inputs	CE ₁ ≥ V _{CC} - 0.2V or CE ₂ ≤ 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0, V _{CC} = 3.3V							

Electrical Characteristics Over the Operating Range

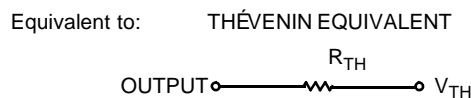
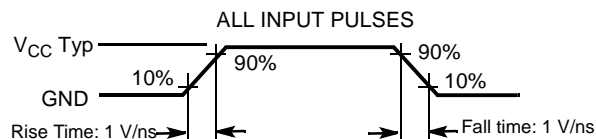
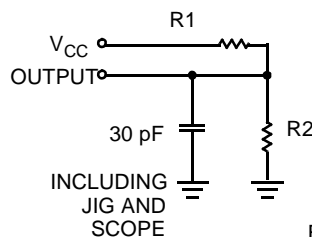
Parameter	Description	Test Conditions	CY62138CV33-55			CY62138CV33-70 CY62138CV-70			Unit
			Min.	Typ. ^[5]	Max.	Min.	Typ. ^[5]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -1.0 mA	V _{CC} = 3.0V	2.4			2.4		V
			V _{CC} = 2.7V				2.4		V
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA	V _{CC} = 3.0V			0.4			V
			V _{CC} = 2.7V					0.4	V
V _{IH}	Input HIGH Voltage		2.2		V _{CC} + 0.3V	2.2		V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage		-0.3		0.8	-0.3		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-1		+1	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC}	V _{CC} = 3.6V I _{OUT} = 0 mA CMOS Levels	7	15	5.5	12	mA	
		f = 1 MHz		1.5	3				1.5
I _{SB1}	Automatic CE Power-down Current—CMOS Inputs	CE ₁ ≥ V _{CC} - 0.2V or CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = f _{max} (Address and Data Only), f = 0 (OE,WE)		5	15		5	15	μA
I _{SB2}	Automatic CE Power-down Current—CMOS Inputs	CE ₁ ≥ V _{CC} - 0.2V or CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0, V _{CC} = 3.6V							

Capacitance^[6]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC(typ.)}	6	pF
C _{OUT}	Output Capacitance		8	pF

Thermal Resistance

Parameter	Description	Test Conditions	BGA	Unit
Θ _{JA}	Thermal Resistance ^[6] (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	55	°C/W
Θ _{JC}	Thermal Resistance ^[6] (Junction to Case)		16	°C/W

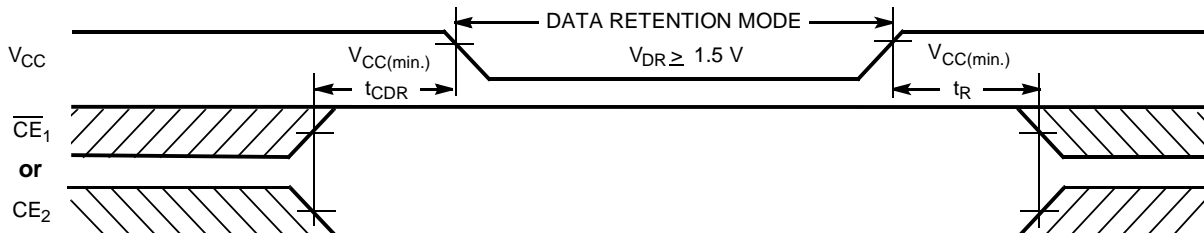
AC Test Loads and Waveforms

Note:

6. Tested initially and after any design or process changes that may affect these parameters.

Parameters	2.5V	3.0V	3.3V	Unit
R1	16600	1105	1216	Ω
R2	15400	1550	1374	Ω
R _{TH}	8000	645	645	Ω
V _{TH}	1.20	1.75	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[5]	Max.	Unit
V _{DR}	V _{CC} for Data Retention		1.5		V _{CC(max.)}	V
I _{CCDR}	Data Retention Current	V _{CC} = 1.5V CE ₁ ≥ V _{CC} - 0.2V or CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V		1	6	μ A
t _{CDR} ^[6]	Chip Deselect to Data Retention Time		0			ns
t _R ^[7]	Operation Recovery Time		t _{RC}			ns

Data Retention Waveform

Switching Characteristics Over the Operating Range^[8]

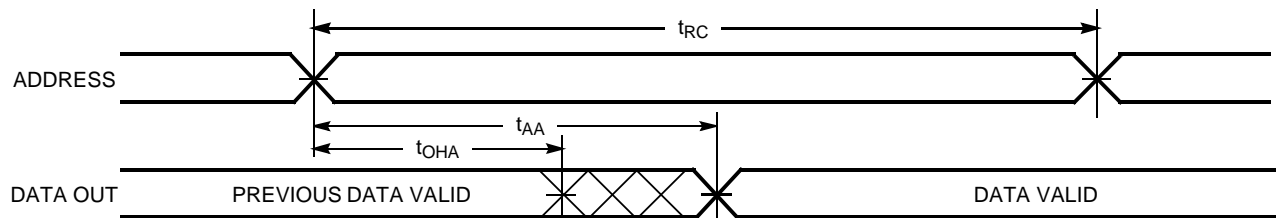
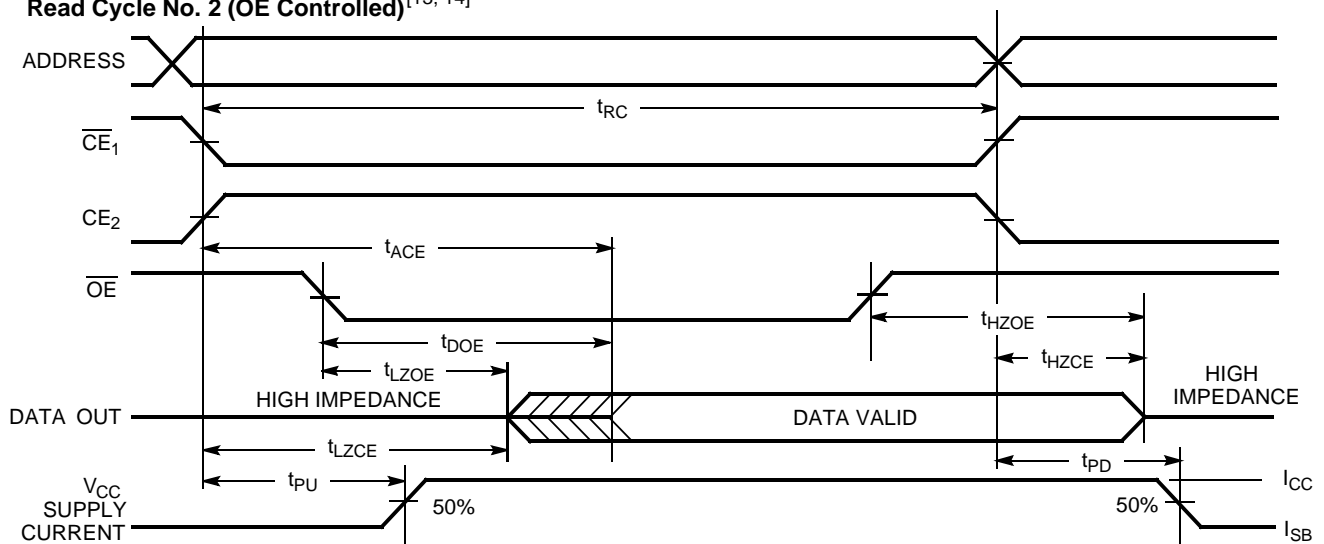
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	10		10		ns
t _{ACE}	CE ₁ LOW and CE ₂ HIGH to Data Valid		55		70	ns
t _{DOE}	OE LOW to Data Valid		25		35	ns
t _{LZOE}	OE LOW to Low-Z ^[9]	5		5		ns
t _{HZOE}	OE HIGH to High-Z ^[9, 10]		20		25	ns
t _{LZCE}	CE ₁ LOW and CE ₂ HIGH to Low-Z ^[9]	10		10		ns
t _{HZCE}	CE ₁ HIGH or CE ₂ LOW to High-Z ^[9, 10]		20		25	ns
t _{PU}	CE ₁ LOW and CE ₂ HIGH to Power-up	0		0		ns
t _{PD}	CE ₁ HIGH or CE ₂ LOW to Power-down		55		70	ns
Write Cycle^[11]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	CE ₁ LOW and CE ₂ HIGH to Write End	45		60		ns

Notes:

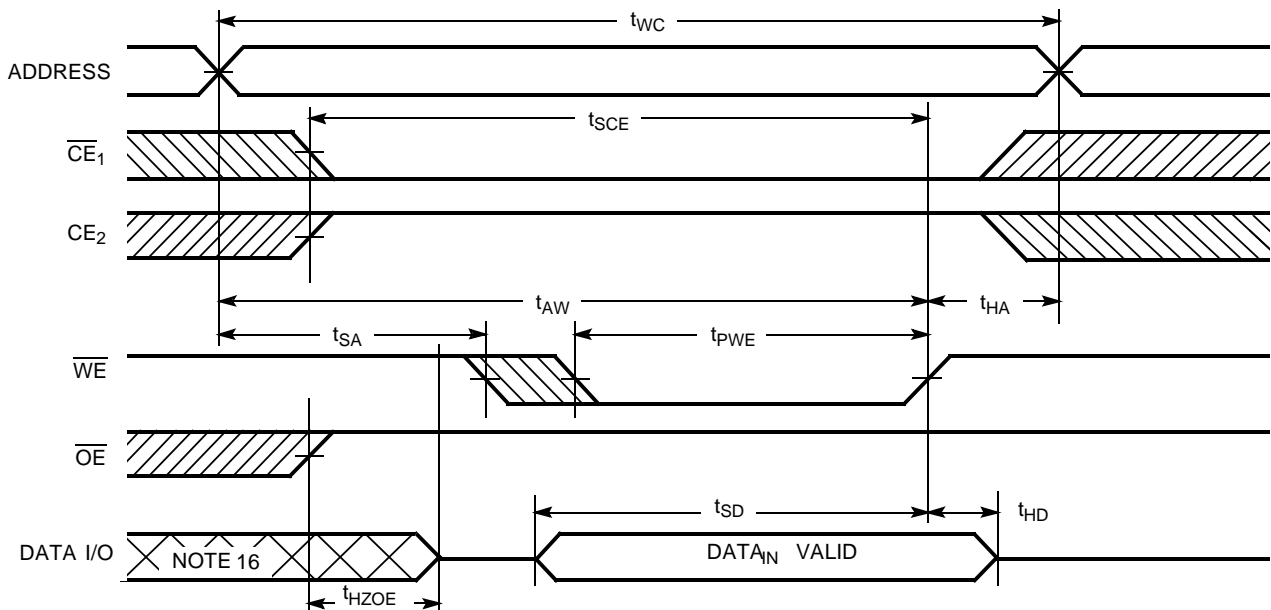
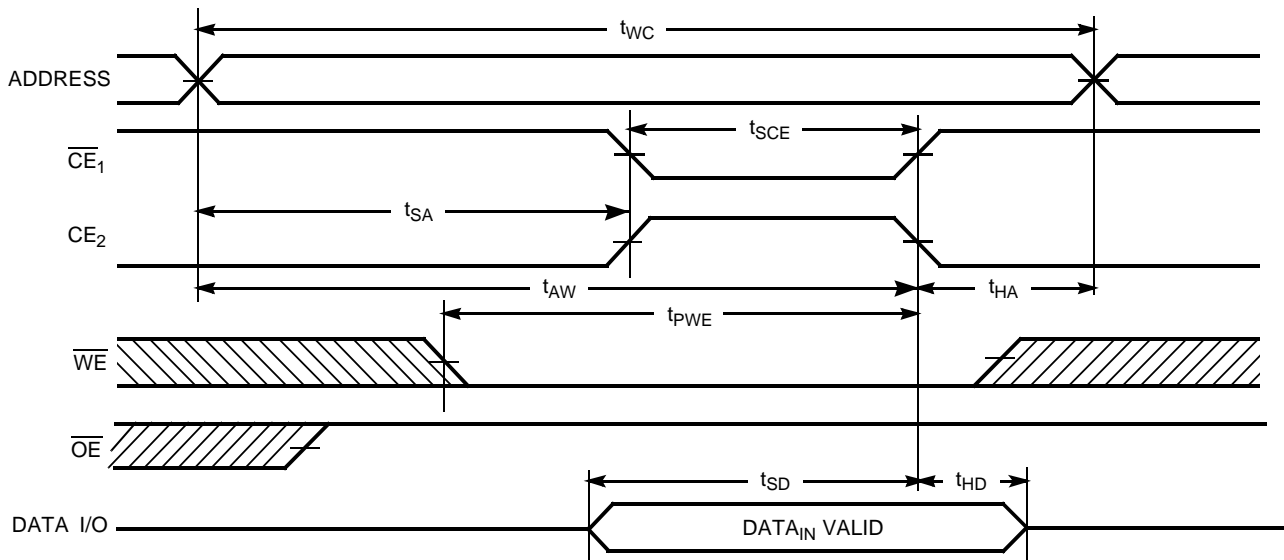
- Full-device AC operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min.)} ≥ 100 μ s or stable at V_{CC(min.)} ≥ 100 μ s.
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of V_{CC(typ.)}/2, input pulse levels of 0 to V_{CC(typ.)}, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
- The internal write time of the memory is defined by the overlap of WE, CE₁ = V_{IL}, and CE₂ = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range^[8] (continued)

Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
t_{AW}	Address Set-up to Write End	45		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	\overline{WE} Pulse Width	40		45		ns
t_{SD}	Data Set-up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	\overline{WE} LOW to High-Z ^[9, 10]		20		25	ns
t_{LZWE}	\overline{WE} HIGH to Low-Z ^[9]	10		10		ns

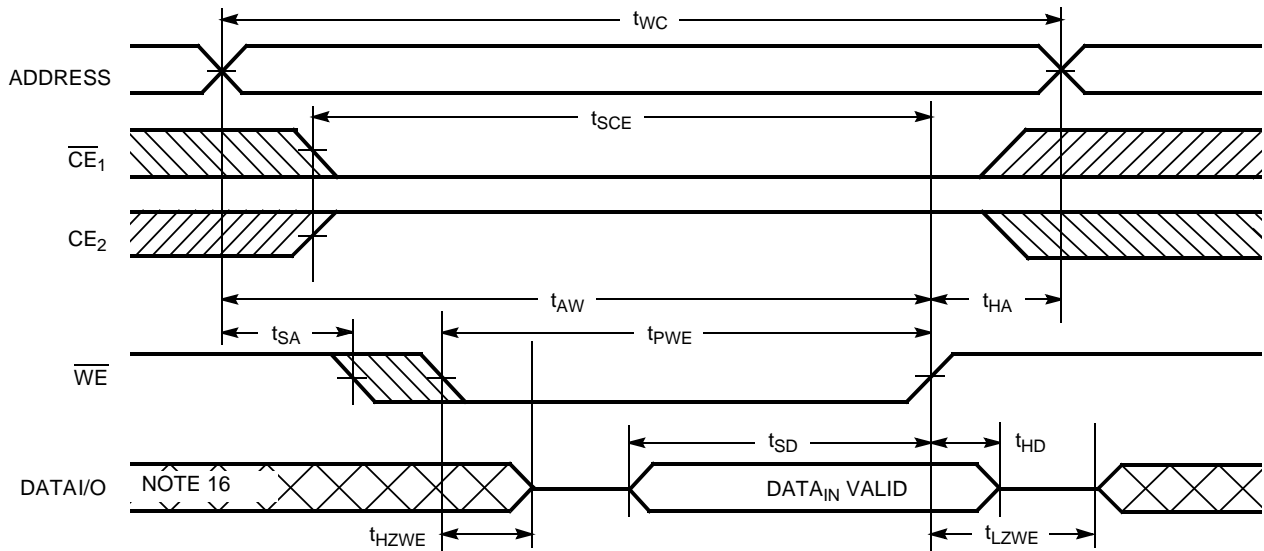
Switching Waveforms
Read Cycle No. 1 (Address Transition Controlled) ^[12, 13]

Read Cycle No. 2 (\overline{OE} Controlled) ^[13, 14]

Notes:

12. Device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
13. \overline{WE} is HIGH for read cycle.
14. Address valid prior to or coincident with \overline{CE}_1 transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)
Write Cycle No. 1 (\overline{WE} Controlled)^[11, 15, 17]

Write Cycle No. 2 (\overline{CE}_1 or CE_2 Controlled)^[11, 15, 17]

Notes:

15. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
16. During this period, the I/Os are in output state and input signals should not be applied.
17. If \overline{CE}_1 goes HIGH or CE_2 goes LOW simultaneously with \overline{WE} HIGH, the output remains in high-impedance state.

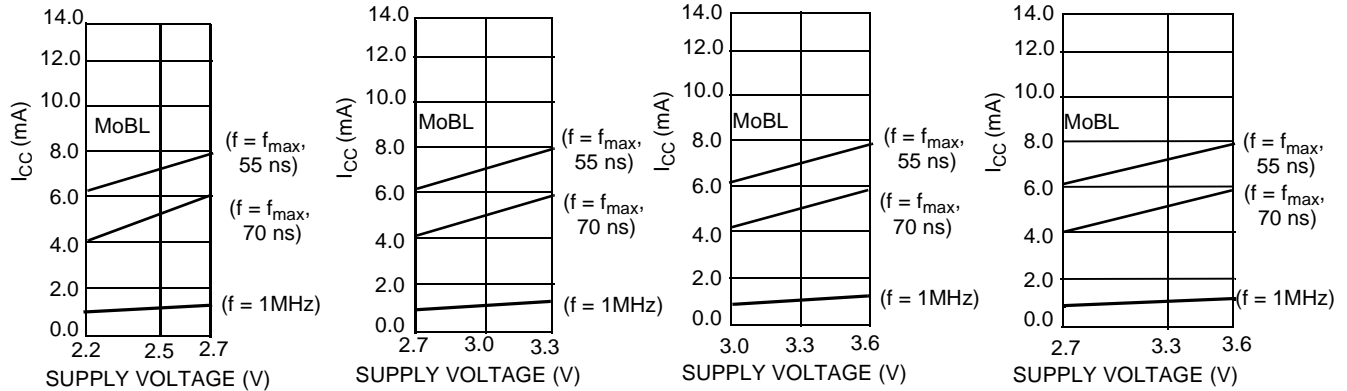
Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[17]


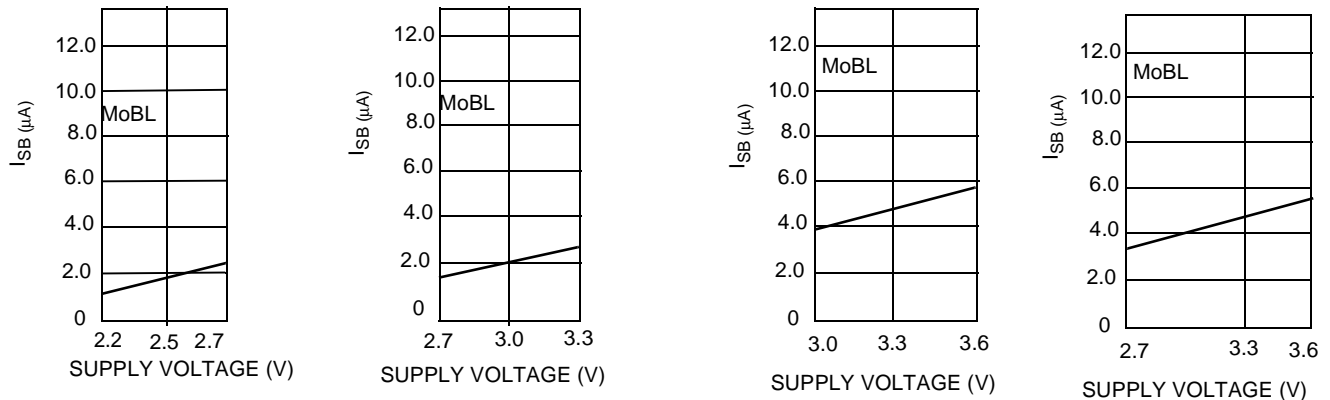
Typical DC and AC Parameters

(Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25^\circ\text{C}$)

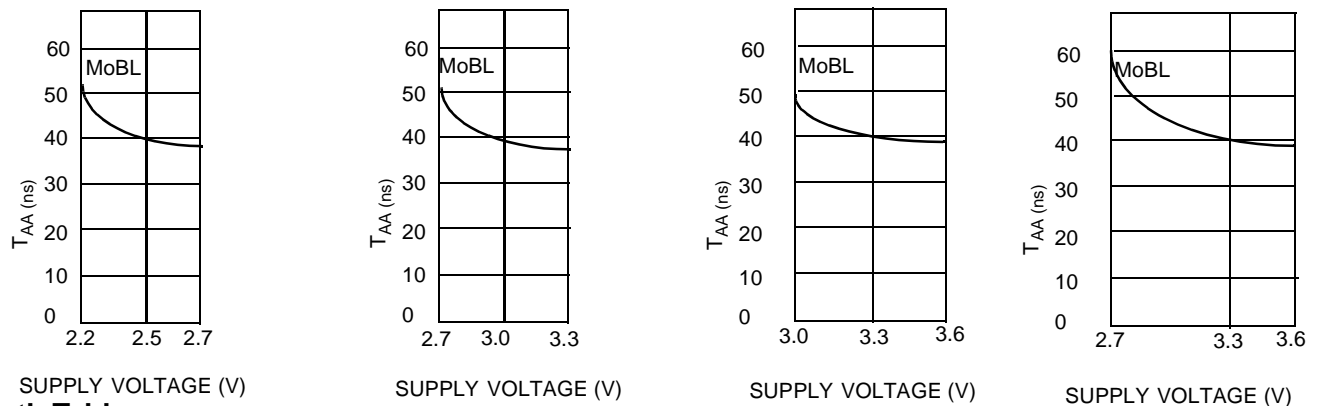
Operating Current vs. Supply Voltage



Standby Current vs. Supply Voltage



Access Time vs. Supply Voltage



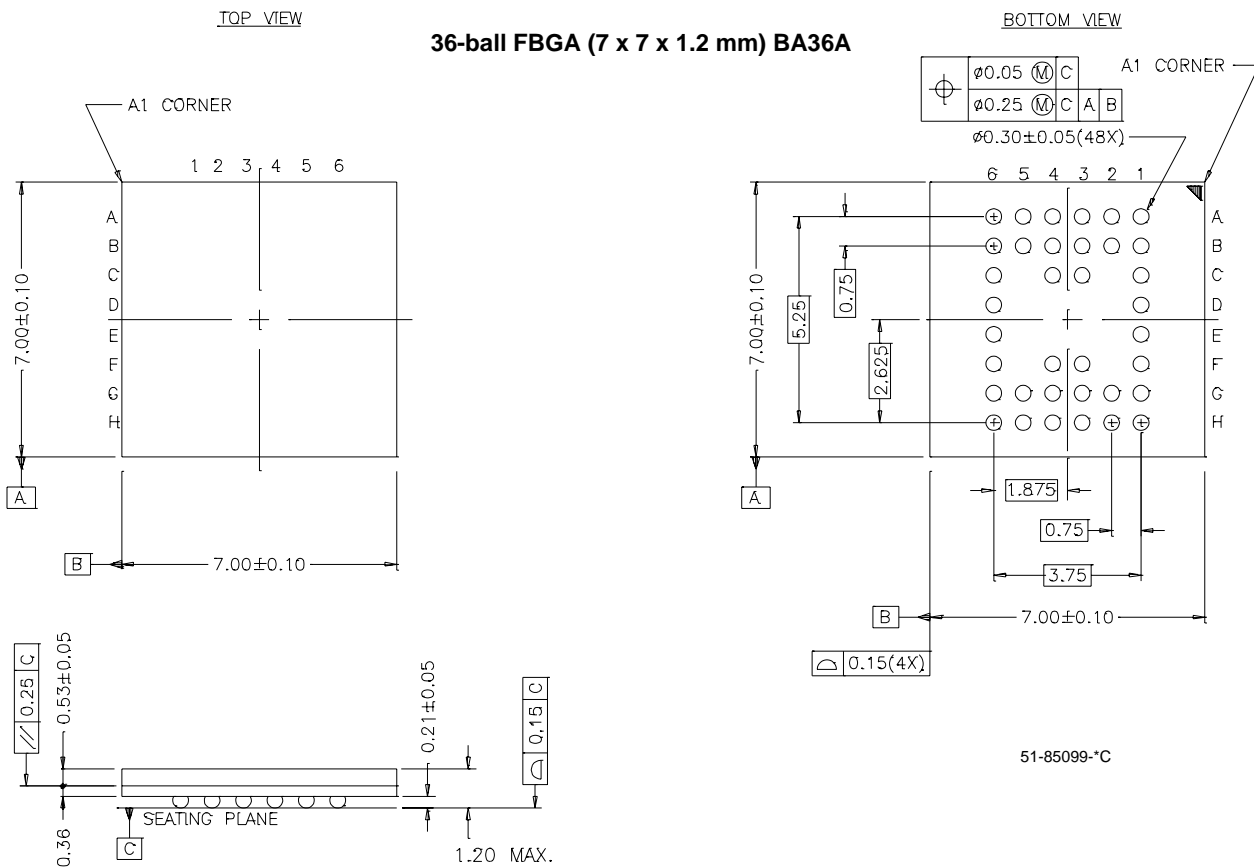
Truth Table

$\overline{\text{CE}}_1$	$\overline{\text{CE}}_2$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Inputs/Outputs	Mode	Power
H	X	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})
X	L	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	Data Out (I/O_0 - I/O_7)	Read	Active (I_{CC})
L	H	H	H	High-Z	Output Disabled	Active (I_{CC})
L	H	L	X	Data in (I/O_0 - I/O_7)	Write	Active (I_{CC})

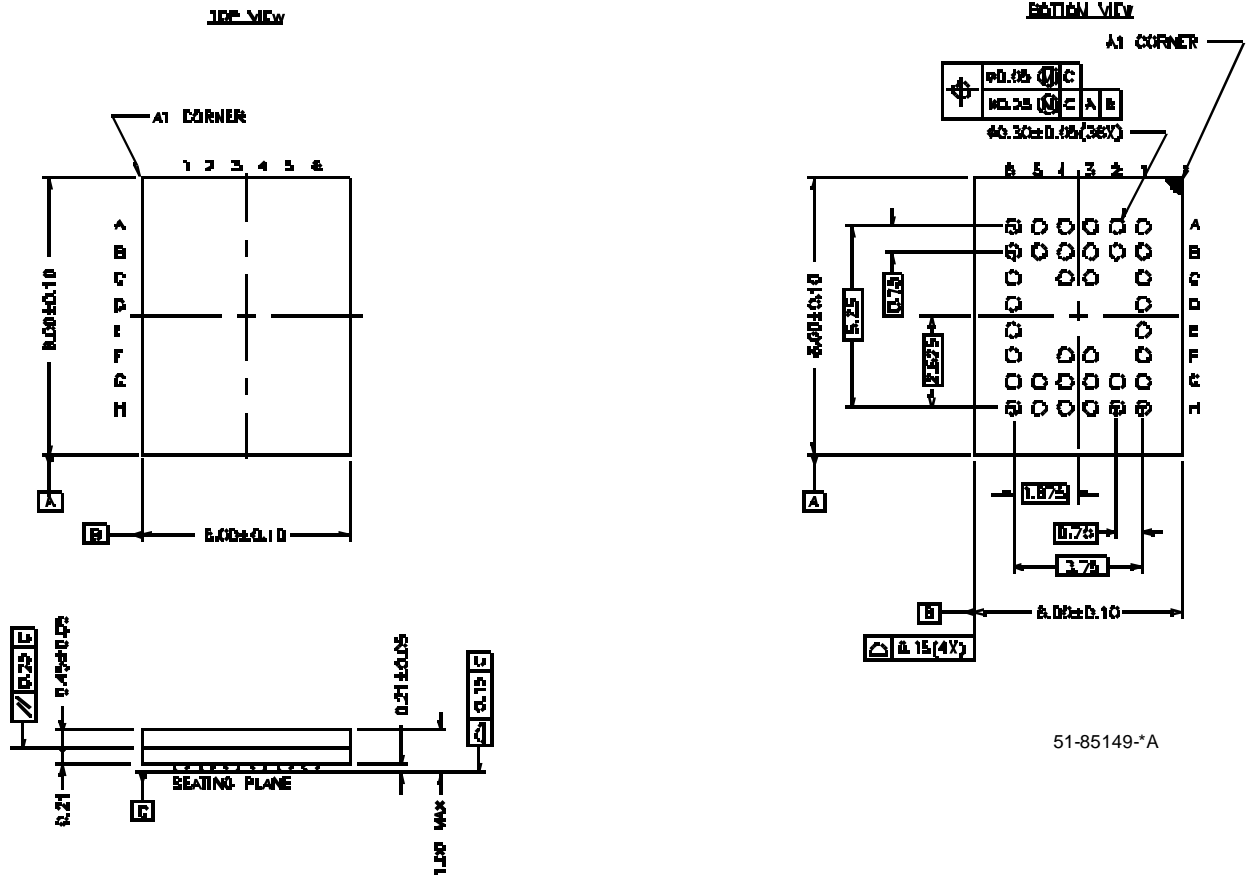
Ordering Information

Speed (ns)	Ordering Code	Voltage Range (V)	Package Name	Package Type	Operating Range
70	CY62138CV25LL-70BAI	2.2–2.7	BA36A	36-ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm)	Industrial
	CY62138CV25LL-70BVI	2.2–2.7	BV36A	36-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62138CV30LL-70BAI	2.7–3.3	BA36A	36-ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm)	
	CY62138CV30LL-70BVI	2.7–3.3	BV36A	36-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62138CV33LL-70BAI	3.0–3.6	BA36A	36-ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm)	
	CY62138CV33LL-70BVI	3.0–3.6	BV36A	36-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62138CVLL-70BAI	2.7–3.6	BA36A	36-ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm)	
	CY62138CVLL-70BVI	2.7–3.6	BV36A	36-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
55	CY62138CV25LL-55BAI	2.2–2.7	BA36A	36-ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm)	Industrial
	CY62138CV25LL-55BVI	2.2–2.7	BV36A	36-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62138CV30LL-55BAI	2.7–3.3	BA36A	36-ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm)	
	CY62138CV30LL-55BVI	2.7–3.3	BV36A	36-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62138CV33LL-55BAI	3.0–3.6	BA36A	36-ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm)	
	CY62138CV33LL-55BVI	3.0–3.6	BV36A	36-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	

Package Diagrams



Package Diagrams (continued)

36-Lead VFBGA (6 x 8 x 1 mm) BV36A


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Document History Page

Document Title: CY62138CV25/30/33 MoBL [®] /CY62138CV MoBL [®] 2M (256K x 8) Static RAM				
Document Number: 38-05200				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	112381	02/19/02	GAV	New Data Sheet (advance information)
*A	114024	04/25/02	JUI	Added BV package diagram Changed from Advance Information to Preliminary
*B	117062	07/12/02	MGN	Added Second Chip Enable Changed from Preliminary to Final
*C	118123	09/09/02	MGN	Added new part number: CY62138CV with wider voltage (2.7V – 3.6V) For T _{AA} = 55 ns, improved t _{PWE} min. from 45 ns to 40 ns For T _{AA} = 70 ns, improved t _{PWE} min. from 60 ns to 45 ns For T _{AA} = 70 ns, improved t _{LZWE} min. from 5 ns to 10 ns
*D	118760	09/23/02	MGN	Improved Typ. I _{CC} spec. to 7 mA (for 55 ns) and 5.5 mA (for 70 ns). Improved Max I _{CC} spec. to 15 mA (for 55 ns) and 12 mA (for 70 ns). For T _{AA} = 55 ns, improved t _{LZWE} min. from 5 ns to 10 ns. Changed upper spec. for Supply Voltage to Ground Potential to V _{CCMAX} + 0.5V. Changed upper spec for DC Voltage Applied to Ouputs in High-Z State and DC Input Voltage to V _{CC} + 0.3V.