

## 2-Mbit (128K x 16) Static RAM

### Features

- **High Speed**
  - 55 ns
- **Temperature Ranges**
  - Industrial: -40°C to 85°C
  - Automotive: -40°C to 125°C
- **Wide voltage range: 2.7V – 3.6V**
- **Ultra-low active, standby power**
- **Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in Pb-free and non Pb-free standard 44-pin TSOP Type II package**

### Functional Description<sup>[1]</sup>

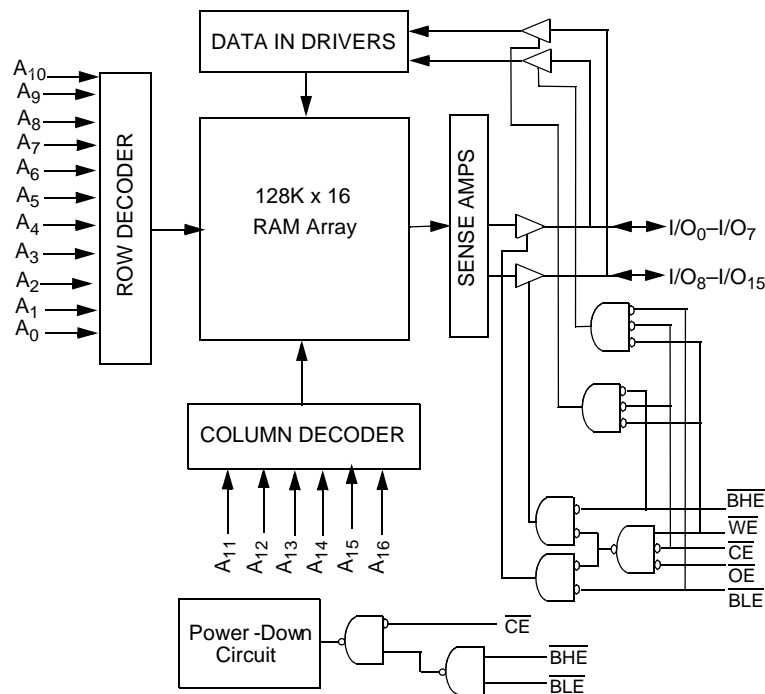
The CY62137V is a high-performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL<sup>®</sup>) in

portable applications such as cellular telephones. The device also has an automatic power-down feature that reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ( $\overline{CE}$  HIGH) or when  $\overline{CE}$  is LOW and both  $\overline{BLE}$  and  $\overline{BHE}$  are HIGH. The input/output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high-impedance state when: deselected ( $\overline{CE}$  HIGH), outputs are disabled ( $\overline{OE}$  HIGH),  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . See the truth table at the back of this data sheet for a complete description of read and write modes.

### Logic Block Diagram



**Note:**

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>

**Product Portfolio**

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Grades	Power Dissipation			
	Min.	Typ. <sup>[2]</sup>	Max.			Operating, I <sub>CC</sub> (mA)		Standby, I <sub>SB2</sub> (μA)	
						Typ. <sup>[2]</sup>	Max.	Typ. <sup>[2]</sup>	Max.
CY62137VLL	2.7	3.0	3.6	55	Industrial	7	20	1	15
				70		7	15	1	15
				70	Automotive	7	15	1	20

**Pin Configurations<sup>[3]</sup>**
**TSOP II (Forward)  
Top View**

A <sub>4</sub>	1	44	A <sub>5</sub>
A <sub>3</sub>	2	43	A <sub>6</sub>
A <sub>2</sub>	3	42	A <sub>7</sub>
A <sub>1</sub>	4	41	$\overline{\text{OE}}$
A <sub>0</sub>	5	40	$\overline{\text{BHE}}$
$\overline{\text{CE}}$	6	39	$\overline{\text{BLE}}$
I/O <sub>0</sub>	7	38	I/O <sub>15</sub>
I/O <sub>1</sub>	8	37	I/O <sub>14</sub>
I/O <sub>2</sub>	9	36	I/O <sub>13</sub>
I/O <sub>3</sub>	10	35	I/O <sub>12</sub>
V <sub>CC</sub>	11	34	V <sub>SS</sub>
V <sub>SS</sub>	12	33	V <sub>CC</sub>
I/O <sub>4</sub>	13	32	I/O <sub>11</sub>
I/O <sub>5</sub>	14	31	I/O <sub>10</sub>
I/O <sub>6</sub>	15	30	I/O <sub>9</sub>
I/O <sub>7</sub>	16	29	I/O <sub>8</sub>
$\overline{\text{WE}}$	17	28	NC
A <sub>16</sub>	18	27	A <sub>8</sub>
A <sub>15</sub>	19	26	A <sub>9</sub>
A <sub>14</sub>	20	25	A <sub>10</sub>
A <sub>13</sub>	21	24	A <sub>11</sub>
A <sub>12</sub>	22	23	NC

**Pin Definitions**

Pin Number	Type	Description
1–5, 18–22, 24–27, 42–45	Input	<b>A<sub>0</sub>–A<sub>16</sub></b> . Address Inputs
7–10, 13–16, 29–32, 35–38	Input/Output	<b>I/O<sub>0</sub>–I/O<sub>15</sub></b> . Data lines. Used as input or output lines depending on operation
23	No Connect	<b>NC</b> . This pin is not connected to the die
17	Input/Control	<b><math>\overline{\text{WE}}</math></b> . When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted
6	Input/Control	<b><math>\overline{\text{CE}}</math></b> . When LOW, selects the chip. When HIGH, deselects the chip
40, 39	Input/Control	<b><math>\overline{\text{BHE}}</math>, <math>\overline{\text{BLE}}</math></b> . <b><math>\overline{\text{BHE}}</math></b> = LOW selects higher order byte WRITES or READs on the SRAM <b><math>\overline{\text{BLE}}</math></b> = LOW selects lower order byte WRITES or READs on the SRAM
41	Input/Control	<b><math>\overline{\text{OE}}</math></b> . Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are Tri-stated, and act as input data pins
12, 34	Ground	<b>V<sub>SS</sub></b> . Ground for the device
11, 33	Power Supply	<b>V<sub>CC</sub></b> . Power supply for the device

**Notes:**

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(TYP)</sub>, T<sub>A</sub> = 25°C.
- NC pins are not connected on the die.

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied.....	-55°C to +125°C
Supply Voltage to Ground Potential .....	-0.5V to +4.6V
DC Voltage Applied to Outputs in High-Z State <sup>[4]</sup> .....	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage <sup>[4]</sup> .....	-0.5V to $V_{CC} + 0.5V$

Output Current into Outputs (LOW).....	20 mA
Static Discharge Voltage.....	> 2001V (per MIL-STD-883, Method 3015)
Latch-up Current.....	> 200 mA

### Operating Range

Range	Ambient Temperature	$V_{CC}$
Industrial	-40°C to +85°C	2.7V to 3.6V
Automotive	-40°C to +125°C	2.7V to 3.6V

### Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62137V-55			CY62137V-70			Unit	
			Min.	Typ. <sup>[2]</sup>	Max.	Min.	Typ. <sup>[2]</sup>	Max.		
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -1.0 \text{ mA}$ , $V_{CC} = 2.7V$	2.4			2.4			V	
$V_{OL}$	Output LOW Voltage	$I_{OL} = 2.1 \text{ mA}$ , $V_{CC} = 2.7V$			0.4			0.4	V	
$V_{IH}$	Input HIGH Voltage		2.2		$V_{CC} + 0.5V$	2.2		$V_{CC} + 0.5V$	V	
$V_{IL}$	Input LOW Voltage		-0.5		0.8	-0.5		0.8	V	
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	-1		+1	$\mu A$	
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-1		+1	-1		+1	$\mu A$	
$I_{CC}$	$V_{CC}$ Operating Supply Current	$I_{OUT} = 0 \text{ mA}$ , $f = f_{Max} = 1/t_{RC}$ , CMOS Levels		7	20		7	15	mA	
		$I_{OUT} = 0 \text{ mA}$ , $f = 1\text{MHz}$ , CMOS Levels		1	2		1	2	mA	
$I_{SB1}$	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , $f = f_{Max}$			100			100	$\mu A$	
$I_{SB2}$	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , $f = 0$	$V_{CC} = 3.6V$ Industrial		1	15		1	15	$\mu A$
			$V_{CC} = 3.6V$ Automotive					1	20	

### Capacitance<sup>[5]</sup>

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ C$ , $f = 1 \text{ MHz}$ , $V_{CC} = V_{CC}(typ)$	6	pF
$C_{OUT}$	Output Capacitance		8	pF

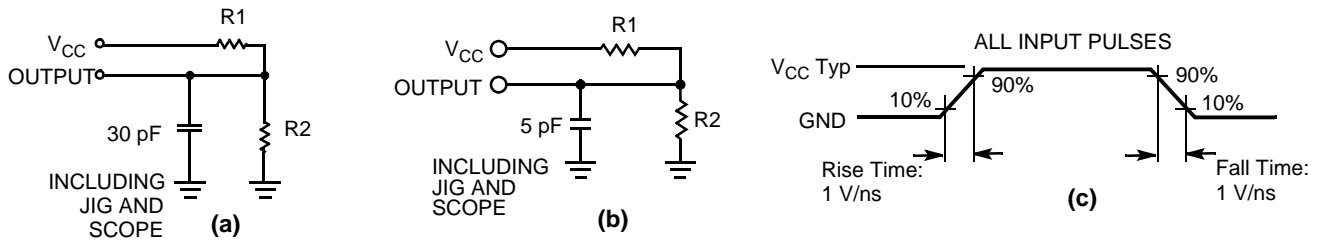
### Thermal Resistance<sup>[5]</sup>

Parameter	Description	Test Conditions	TSOPII	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 2-layer printed circuit board	60	$^\circ C/W$
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		22	$^\circ C/W$

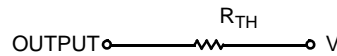
#### Notes:

- $V_{IL}(\text{min.}) = -2.0V$  for pulse durations less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

### AC Test Loads and Waveforms



Equivalent to: THEVENIN EQUIVALENT

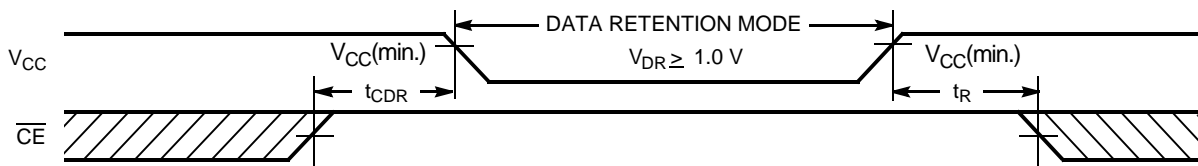


Parameters	3.0V	Unit
R1	1105	Ohms
R2	1550	Ohms
$R_{TH}$	645	Ohms
$V_{TH}$	1.75	Volts

### Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. <sup>[2]</sup>	Max.	Unit	
$V_{DR}$	$V_{CC}$ for Data Retention		1.0			V	
$I_{CCDR}$	Data Retention Current	$V_{CC} = 1.0V, \overline{CE} \geq V_{CC} - 0.3V,$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V,$ No input may exceed $V_{CC} + 0.3V$	Industrial		0.5	7.5	$\mu A$
			Automotive			10	
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time		0			ns	
$t_R$	Operation Recovery Time		70			ns	

### Data Retention Waveform



**Switching Characteristics** Over the Operating Range <sup>[6]</sup>

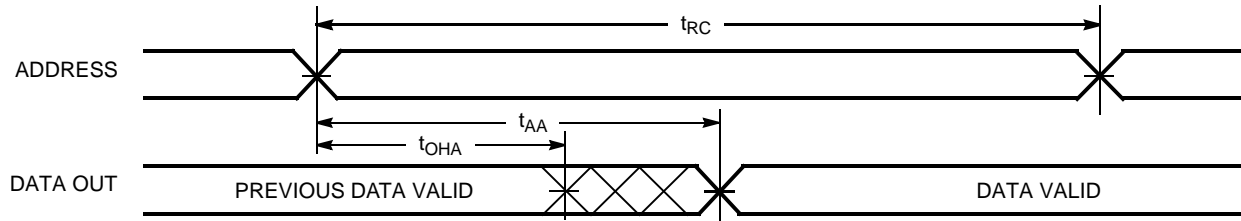
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
t <sub>RC</sub>	Read Cycle Time	55		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		ns
t <sub>ACE</sub>	$\overline{\text{CE}}$ LOW to Data Valid		55		70	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ LOW to Data Valid		25		35	ns
t <sub>LZOE</sub>	$\overline{\text{OE}}$ LOW to Low-Z <sup>[7]</sup>	5		5		ns
t <sub>HZOE</sub>	$\overline{\text{OE}}$ HIGH to High-Z <sup>[7, 8]</sup>		25		25	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}$ LOW to Low-Z <sup>[7]</sup>	10		10		ns
t <sub>HZCE</sub>	$\overline{\text{CE}}$ HIGH to High-Z <sup>[7, 8]</sup>		25		25	ns
t <sub>PU</sub>	$\overline{\text{CE}}$ LOW to Power-up	0		0		ns
t <sub>PD</sub>	$\overline{\text{CE}}$ HIGH to Power-down		55		70	ns
t <sub>DBE</sub>	$\overline{\text{BHE}}/\overline{\text{BLE}}$ LOW to Data Valid		55		70	ns
t <sub>LZBE</sub> <sup>[9]</sup>	$\overline{\text{BHE}}/\overline{\text{BLE}}$ LOW to Low-Z	5		5		ns
t <sub>HZBE</sub>	$\overline{\text{BHE}}/\overline{\text{BLE}}$ HIGH to High-Z		25		25	ns
<b>Write Cycle</b> <sup>[10, 11]</sup>						
t <sub>WC</sub>	Write Cycle Time	55		70		ns
t <sub>SCE</sub>	$\overline{\text{CE}}$ LOW to Write End	45		60		ns
t <sub>AW</sub>	Address Set-up to Write End	45		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ Pulse Width	40		50		ns
t <sub>SD</sub>	Data Set-up to Write End	25		30		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{\text{WE}}$ LOW to High-Z <sup>[7, 8]</sup>		20		25	ns
t <sub>LZWE</sub>	$\overline{\text{WE}}$ HIGH to Low-Z <sup>[7]</sup>	5		10		ns
t <sub>BW</sub>	$\overline{\text{BHE}}/\overline{\text{BLE}}$ LOW to End of Write	50		60		ns

**Notes:**

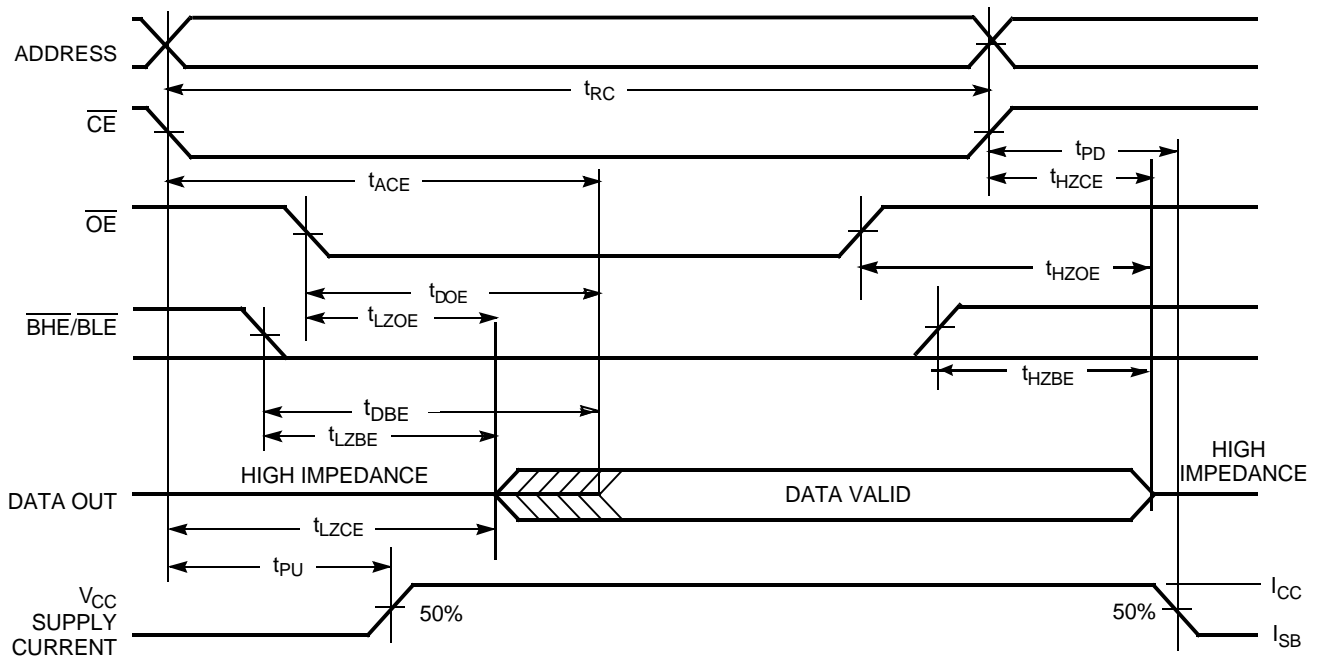
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to V<sub>CC</sub> typ., and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
7. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
8. t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. If both byte enables are toggled together this value is 10 ns.
10. The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for write cycle #3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

### Switching Waveforms

#### Read Cycle No. 1 (Address Transition Controlled)<sup>[12, 13]</sup>



#### Read Cycle No. 2 ( $\overline{\text{OE}}$ Controlled)<sup>[13, 14]</sup>

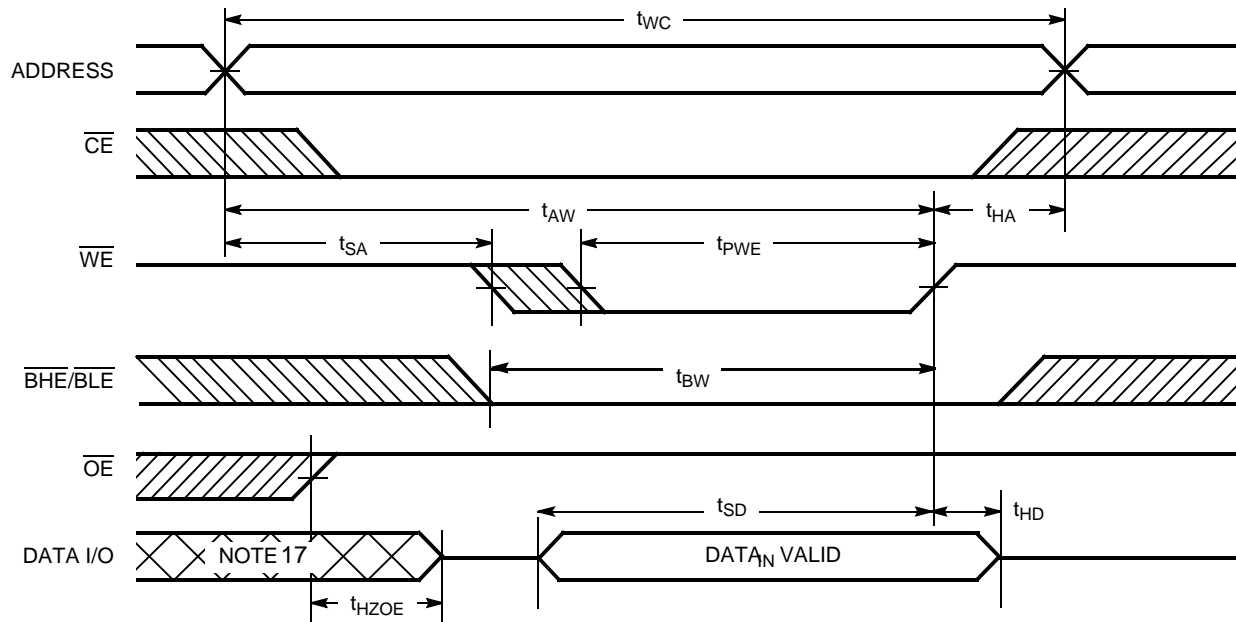


**Notes:**

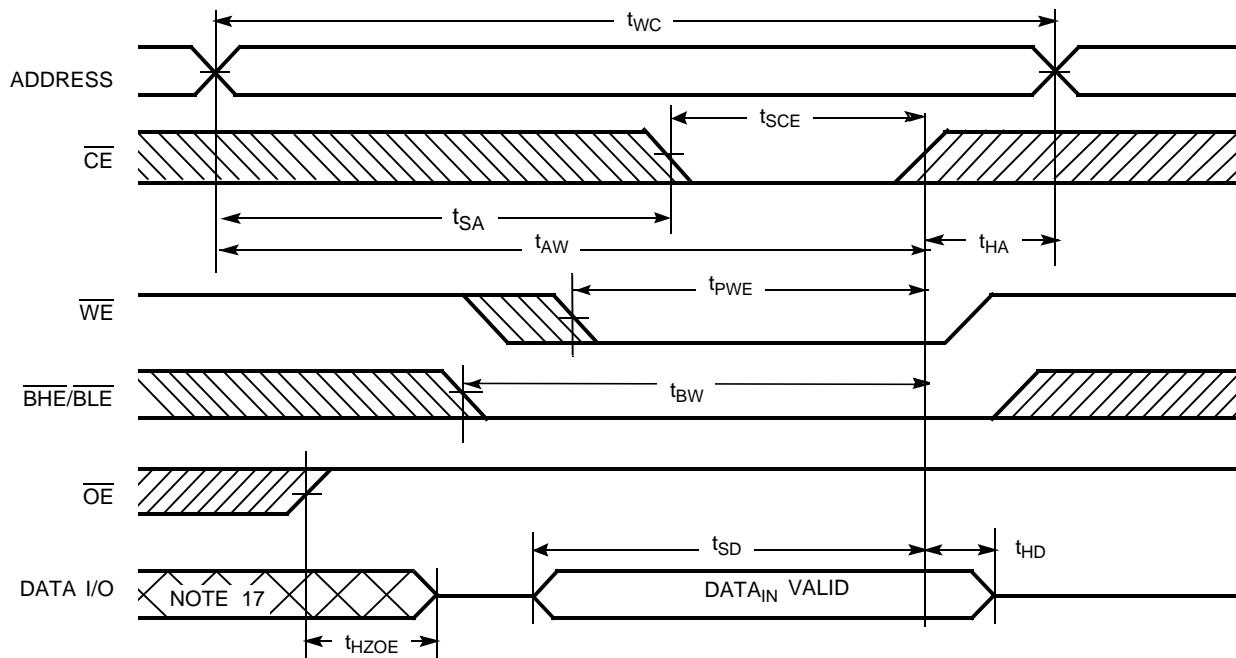
- 12. Device is continuously selected.  $\overline{\text{OE}}, \overline{\text{CE}} = V_{\text{IL}}$ .
- 13.  $\overline{\text{WE}}$  is HIGH for read cycle.
- 14. Address valid prior to or coincident with  $\overline{\text{CE}}$  transition LOW.

**Switching Waveforms** (continued)

**Write Cycle No. 1 (WE Controlled)**<sup>[10, 15, 16]</sup>



**Write Cycle No. 2 (CE Controlled)**<sup>[10, 15, 16]</sup>

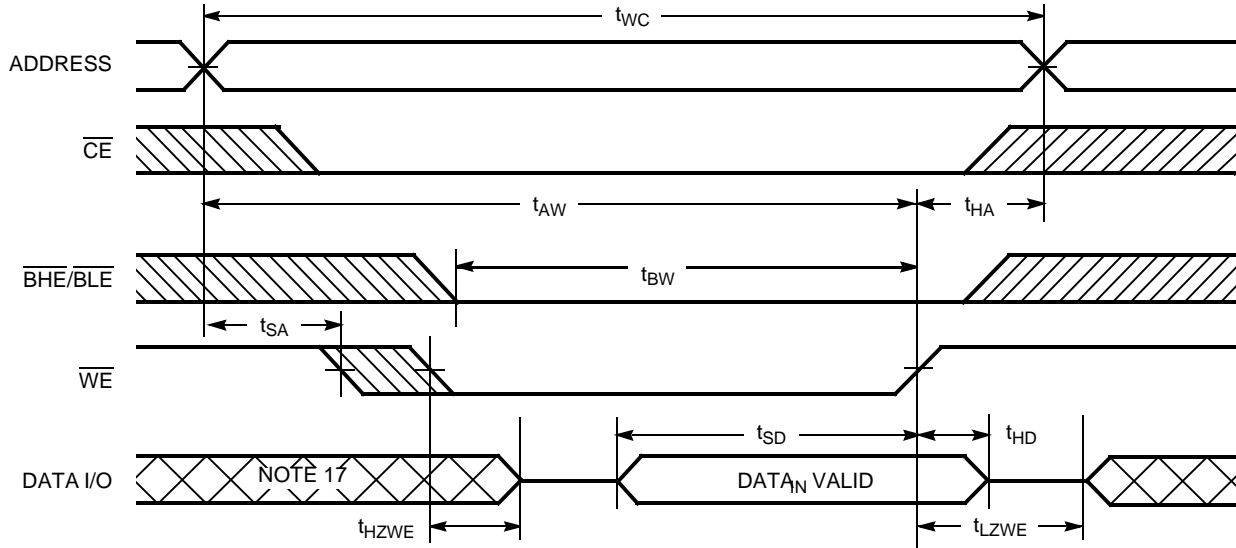


**Notes:**

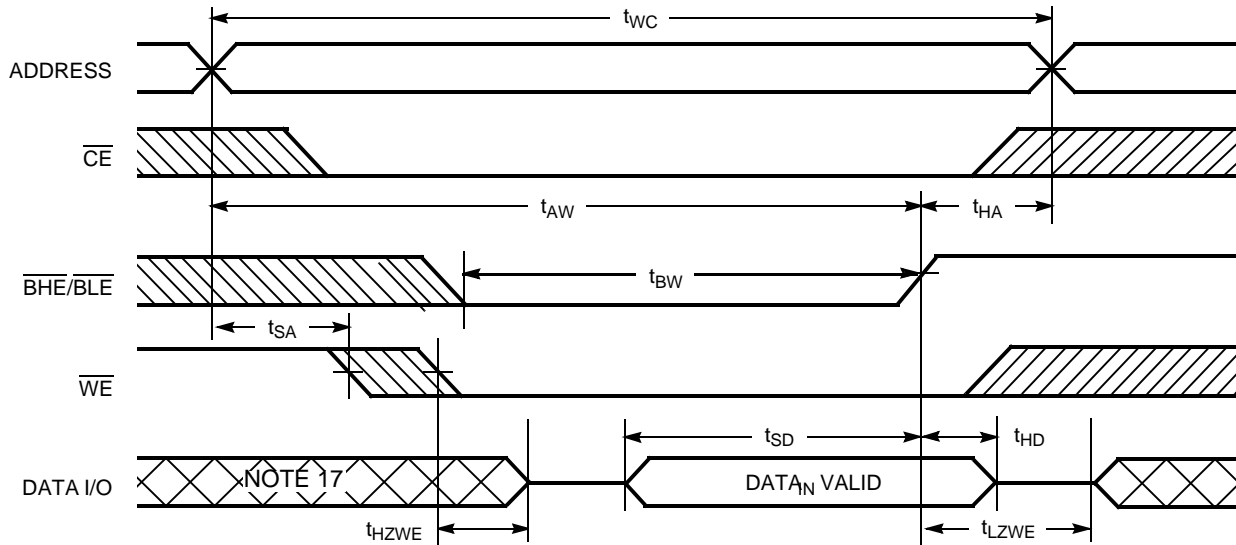
- 15. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$
- 16. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.
- 17. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

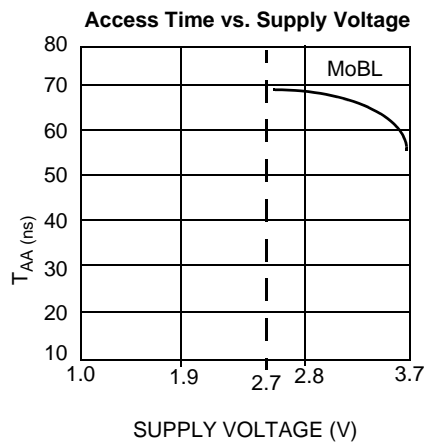
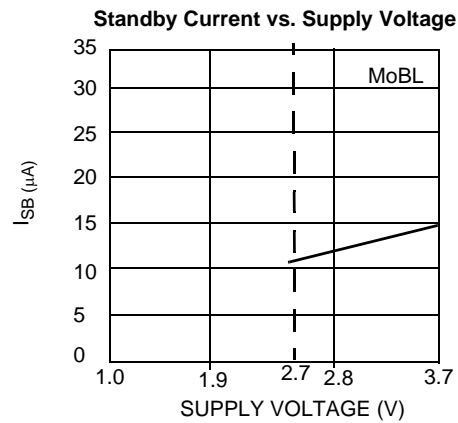
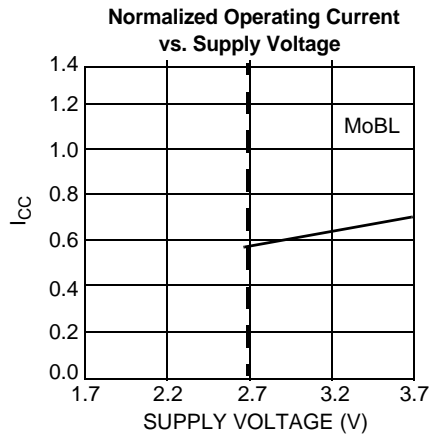
Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[11, 16]</sup>



Write Cycle No. 4 ( $\overline{BHE/BLE}$  Controlled,  $\overline{OE}$  LOW)<sup>[17]</sup>





**Typical DC and AC Characteristics**

**Truth Table**

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	X	X	H	H	High-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out (I/O <sub>0</sub> -I/O <sub>15</sub> )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	High-Z (I/O <sub>8</sub> -I/O <sub>15</sub> ); Data Out (I/O <sub>0</sub> -I/O <sub>7</sub> )	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out (I/O <sub>8</sub> -I/O <sub>15</sub> ); High-Z (I/O <sub>0</sub> -I/O <sub>7</sub> )	Read	Active ( $I_{CC}$ )
L	L	X	L	L	Data In (I/O <sub>0</sub> -I/O <sub>15</sub> )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	High-Z (I/O <sub>8</sub> -I/O <sub>15</sub> ); Data In (I/O <sub>0</sub> -I/O <sub>7</sub> )	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In (I/O <sub>8</sub> -I/O <sub>15</sub> ); High-Z (I/O <sub>0</sub> -I/O <sub>7</sub> )	Write	Active ( $I_{CC}$ )
L	H	H	L	L	High-Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	High-Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	H	H	L	H	High-Z	Deselect/Output Disabled	Active ( $I_{CC}$ )

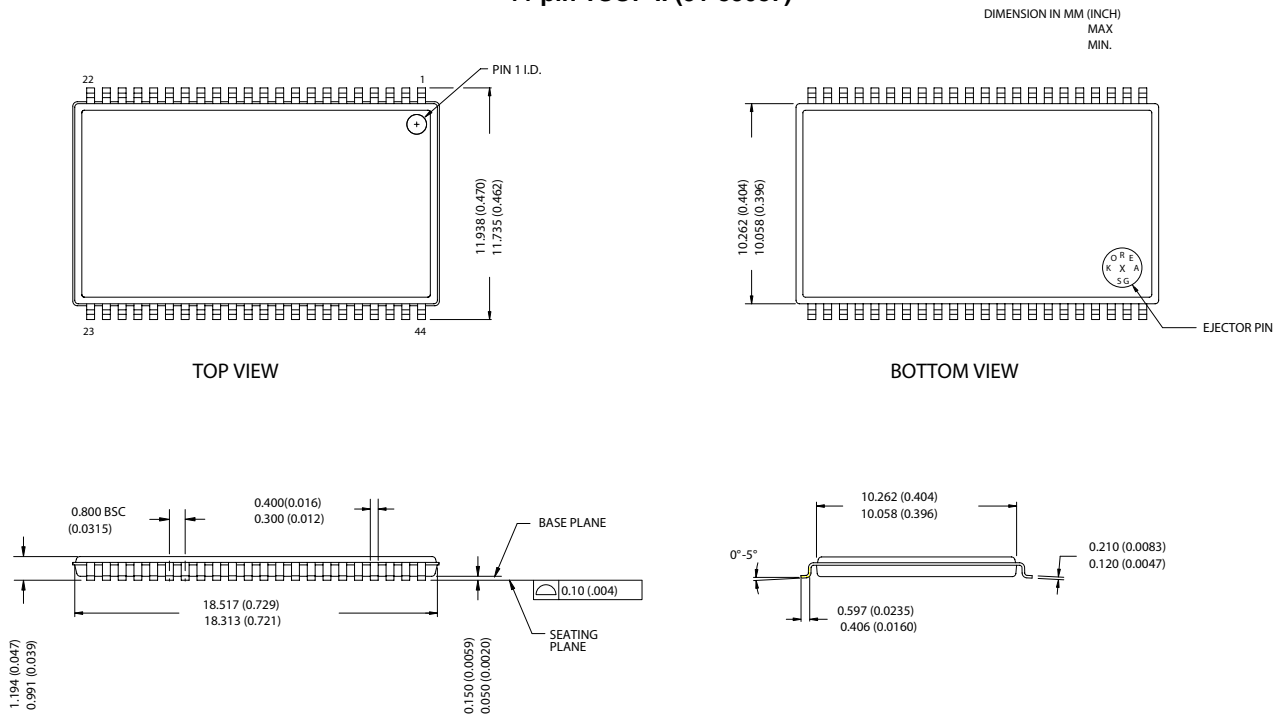
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62137VLL-55ZI	51-85087	44-pin TSOP II	Industrial
	CY62137VLL-55ZXI		44-pin TSOP II (Pb-free)	
70	CY62137VLL-70ZI		44-pin TSOP II	Automotive
	CY62137VLL-70ZXI		44-pin TSOP II (Pb-free)	
	CY62137VLL-70ZE		44-pin TSOP II	
	CY62137VLL-70ZXE		44-pin TSOP II (Pb-free)	
	CY62137VLL-70ZSXE		44-pin TSOP II (Pb-free)	

Please contact your local Cypress sales representative for availability of these parts

**Package Diagrams**

**44-pin TSOP II (51-85087)**



51-85087-A

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**Document History Page**

<b>Document Title: CY62137V MoBL® 2M (128K x 16) Static RAM</b>				
<b>Document Number: 38-05051</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	109960	10/03/01	SZV	Changed from Spec number: 38-00738 to 38-05051
*A	116788	09/04/02	GBI	Added footnote number one Added SL power bin Deleted fBGA package; replacement fBGA package is available in CY62137CV30
*B	237428	See ECN	AJU	Added Automotive product information
*C	329640	See ECN	AJU	Changed TSOPII package name from Z44 to ZS44 Added Pb-free ordering information
*D	372074	See ECN	SYT	Added Pb-free ordering information for Automotive
*E	486789	See ECN	VKN	Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Removed SL Power Bin Updated Ordering Information Table