# CY62137CV30/33 MoBL®
# CY62137CV MoBL®

## 2-Mbit (128K x 16) Static RAM

## Features

- Very high speed: 55 ns
- Temperature ranges
  - Industrial: –40°C to +85°C
  - Automotive-E: –40°C to +125°C
- Pin compatible with CY62137V
- Ultra low active power
  - Typical active current: 1.5 mA at f = 1 MHz
  - Typical active current: 7 mA at f = $f_{MAX}$ (55 ns speed)
- Low and ultra low standby power
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in Pb-free and non Pb-free 48-ball FBGA package

## Functional Description

The CY62137CV30/33 and CY62137CV are high-performance CMOS static RAMs organized as 128K words by 16 bits. These devices feature advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life (MoBL) in portable applications such as cellular telephones. These devices also have an automatic power down feature that significantly reduces power consumption by 80 percent when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected; Chip Enable ($\overline{CE}$) HIGH or both Byte Low Enable ($\overline{BLE}$) and Byte High Enable ($\overline{BHE}$) are HIGH. The input and output pins ($IO_0$ through $IO_{15}$) are placed in a high-impedance state in the following conditions:

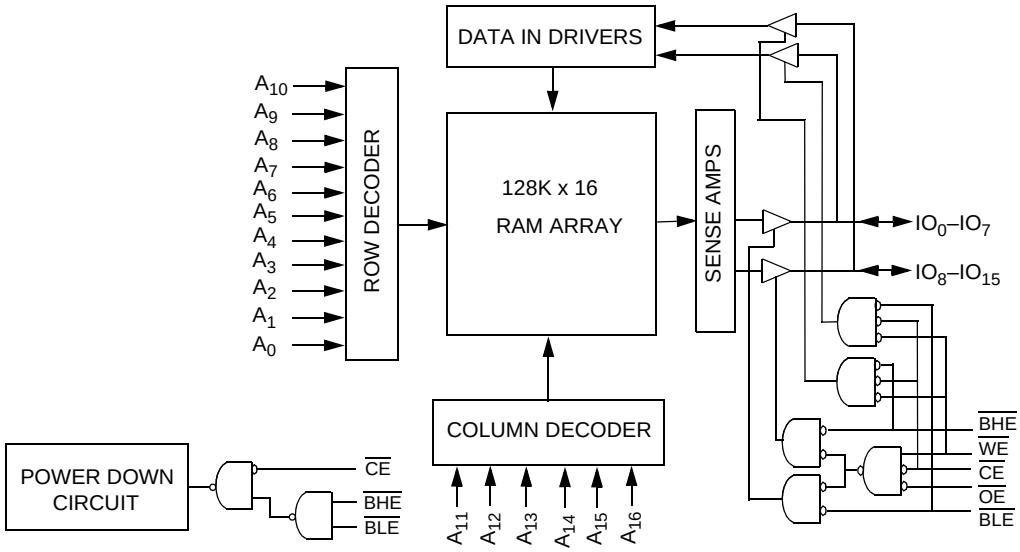
- Deselected ($\overline{CE}$ HIGH)
- Outputs are disabled ($\overline{OE}$ HIGH)
- Both BHE and BLE are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH)
- Write operation is active ($\overline{CE}$ LOW and Write Enable ($\overline{WE}$) LOW)

Write to the device by taking $\overline{CE}$ and $\overline{WE}$ inputs LOW. If $\overline{BLE}$ is LOW, then data from the IO pins ($IO_0$ through $IO_7$) is written into the location specified on the address pins ($A_0$ through $A_{16}$). If $\overline{BHE}$ is LOW, then data from the IO pins ($IO_8$ through $IO_{15}$) is written into the location specified on the address pins ($A_0$ through $A_{16}$).

Read from the device by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW, while forcing the Write Enable ($\overline{WE}$) HIGH. If $\overline{BLE}$ is LOW, then data from the memory location specified by the address pins appear on $IO_0$ to $IO_7$. If $\overline{BHE}$ is LOW, then data from memory appears on $IO_8$ to $IO_{15}$. See the "Truth Table" on page 10 for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note *AN1064, SRAM System Guidelines*.

## Logic Block Diagram

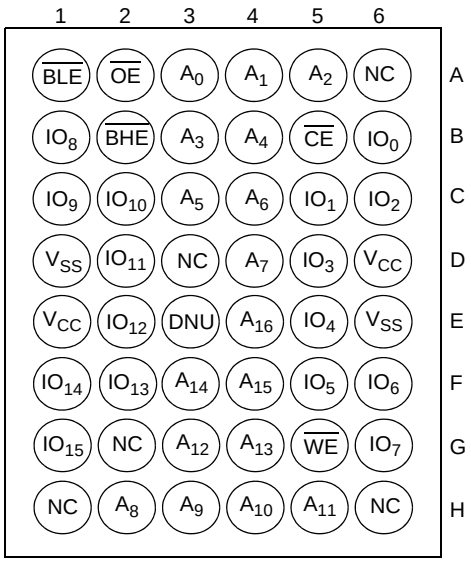


## Product Portfolio

| Product | Range | $V_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Operating $I_{CC}$ (mA) | | | | Standby $I_{SB2}$ (µA) | |
| | | | | | | f = 1 MHz | | f = $f_{MAX}$ | | | |
| | | Min | Typ [1] | Max | | Typ [1] | Max | Typ [1] | Max | Typ [1] | Max |
| CY62137CV30LL | Industrial | 2.7 | 3.0 | 3.3 | 55 | 1.5 | 3 | 7 | 15 | 2 | 10 |
| | | | | | 70 | 1.5 | 3 | 5.5 | 12 | | |
| CY62137CV30LL | Automotive | 2.7 | 3.0 | 3.3 | 70 | 1.5 | 3 | 5.5 | 15 | 2 | 15 |
| CY62137CV33LL | Industrial | 3.0 | 3.3 | 3.6 | 55 | 1.5 | 3 | 7 | 15 | 5 | 15 |
| CY62137CVSL | Industrial | 2.9 | 3.3 | 3.6 | 70 | 1.5 | 3 | 5.5 | 12 | 1 | 5 |

## Pin Configuration

**Figure 1. 48-Ball FBGA Pinout** [2, 3]




**Notes**
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = $V_{CC(Typ)}$, $T_A$ = 25°C.
2. NC pins are not connected on the die.
3. To ensure proper operation, leave floating E3 (DNU) pin or tie to $V_{SS}$.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65°C to + 150°C

Ambient Temperature with Power Applied ..... –55°C to + 125°C

Supply Voltage to Ground Potential..... – 0.5V to $V_{CC(Max)}$ + 0.5V

DC Voltage Applied to Outputs in High-Z State [4]..... –0.5V to $V_{CC}$ + 0.3V

DC Input Voltage [4] ..... –0.5V to $V_{CC}$ + 0.3V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (MIL–STD–883, Method 3015)

Latch up Current .....> 200 m

## Operating Range

| Device | Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|---|
| CY62137CV30 | Industrial | –40°C to +85°C | 2.7V to 3.3V |
| CY62137CV33 | | | 3.0V to 3.6V |
| CY62137CV | | | 2.9V to 3.6V |
| CY62137CV30 | Automotive | –40°C to +125°C | 2.7V to 3.3V |

## Electrical Characteristics

Over the operating range

| Parameter | Description | Test Conditions | | CY62137CV30-55 | | | CY62137CV30-70 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | Min | Typ[1] | Max | |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –1.0 mA | | 2.4 | | | 2.4 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 2.1 mA | | | | 0.4 | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2.2 | | $V_{CC}$ + 0.3 | 2.2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage | | | –0.3 | | 0.8 | –0.3 | | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$ | Ind'l | –1 | | +1 | –1 | | +1 | µA |
| | | | Auto | | | | –2 | | +2 | |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_O$ ≤ $V_{CC}$, output disabled | Ind'l | –1 | | +1 | –1 | | +1 | µA |
| | | | Auto | | | | –2 | | +2 | |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | f = $f_{MAX}$ = 1/$t_{RC}$; $V_{CC}$ = $V_{CC(Max)}$, $I_{OUT}$ = 0 mA CMOS levels | Ind'l | | 7 | 15 | | 5.5 | 12 | mA |
| | | | Auto | | | | | 5.5 | 15 | |
| | | f = 1 MHz | Ind'l | | 1.5 | 3 | | 1.5 | 3 | |
| | | | Auto | | | | | 1.5 | 3 | |
| $I_{SB1}$ | Automatic CE Power Down Current – CMOS Inputs | $\overline{CE}$ ≥ $V_{CC}$ – 0.2V, $V_{IN}$ ≥ $V_{CC}$ – 0.2V or $V_{IN}$ ≤ 0.2V f = $f_{MAX}$ (address and data only), f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$, and $\overline{BLE}$), | Ind'l | | 2 | 10 | | 2 | 10 | µA |
| | | | Auto | | | | | 2 | 15 | |
| $I_{SB2}$ | Automatic CE Power Down Current – CMOS Inputs | $\overline{CE}$ ≥ $V_{CC}$ – 0.2V, $V_{IN}$ ≥ $V_{CC}$ – 0.2V or $V_{IN}$ ≤ 0.2V, f = 0, $V_{CC}$ = 3.3V | Ind'l | | 2 | 10 | | 2 | 10 | µA |
| | | | Auto | | | | | 2 | 15 | |

**Note**

4. $V_{IL(Min)}$ = –2.0V for pulse durations less than 20 ns.

## Electrical Characteristics (Continued)

Over the operating range

| Parameter | Description | Test Conditions | | | CY62137CV33-55 | | | CY62137CV-70 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ[1] | Max | Min | Typ[1] | Max | |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –1.0 mA | $V_{CC}$ = 3.0V | | 2.4 | | | 2.4 | | | V |
| | | | $V_{CC}$ = 2.9V | | | | | 2.4 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 2.1 mA | $V_{CC}$ = 3.0V | | | | 0.4 | | | 0.4 | V |
| | | | $V_{CC}$ = 2.9V | | | | | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | | | 2.2 | | $V_{CC}$ + 0.3 | 2.2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage | | | | –0.3 | | 0.8 | –0.3 | | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$ | | | –1 | | +1 | –1 | | +1 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_O$ ≤ $V_{CC}$, output disabled | | | –1 | | +1 | –1 | | +1 | µA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | f = $f_{MAX}$ = 1/$t_{RC}$<br>f = 1 MHz | $V_{CC}$ = $V_{CC(Max)}$<br>$I_{OUT}$ = 0 mA<br>CMOS levels | | | 7 | 15 | | 5.5 | 12 | mA |
| | | | | | | 1.5 | 3 | | 1.5 | 3 | |
| $I_{SB1}$ | Automatic CE Power Down Current – CMOS Inputs | $\overline{CE}$ ≥ $V_{CC}$ – 0.2V,<br>$V_{IN}$ ≥ $V_{CC}$ – 0.2V or $V_{IN}$ ≤ 0.2V<br>f = $f_{MAX}$(address and data only),<br>f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$, and $\overline{BLE}$), | | | | 5 | 15 | | 5 | 15 | µA |
| $I_{SB2}$ | Automatic CE Power Down Current – CMOS Inputs | $\overline{CE}$ ≥ $V_{CC}$ – 0.2V,<br>$V_{IN}$ ≥ $V_{CC}$ – 0.2V or $V_{IN}$ ≤ 0.2V,<br>f = 0, $V_{CC}$ = 3.6V | | LL | | 5 | 15 | | | | µA |
| | | | | SL | | | | | 1 | 5 | |

## Capacitance

Tested initially and after any design or process changes that may affect these parameters

| Parameter | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz,<br>$V_{CC}$ = $V_{CC(Typ)}$ | 6 | pF |
| $C_{OUT}$ | Output Capacitance | | 8 | pF |

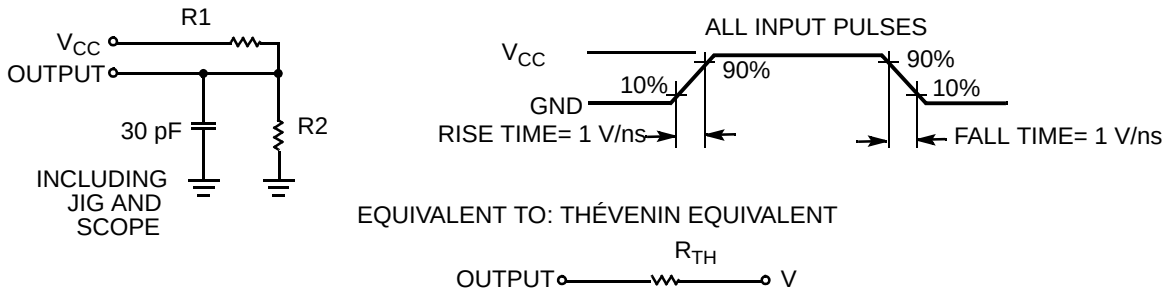
## Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters

| Parameter | Description | Test Conditions | FBGA | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, two layer printed circuit board | 55 | °C/W |
| $\Theta_{JC}$ | Thermal Resistance (junction to case) | | 16 | °C/W |

## AC Test Loads and Waveforms

**Figure 2. AC Test Loads and Waveform**




| Parameters | 3.0V | 3.3V | Unit |
|---|---|---|---|
| R1 | 1105 | 1216 | Ω |
| R2 | 1550 | 1374 | Ω |
| $R_{TH}$ | 645 | 645 | Ω |
| $V_{TH}$ | 1.75 | 1.75 | V |

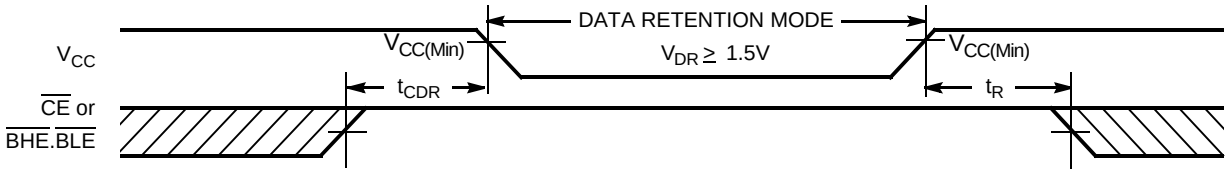
## Data Retention Characteristics

Over the operating range

| Parameter | Description | Conditions | | | Min | Typ [1] | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | | | | 1.5 | | | V |
| $I_{CCDR}$ | Data Retention Current | $V_{CC}$ = 1.5V, $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ | LL | Ind'l | | 1 | 6 | µA |
| | | | | Auto | | | 8 | |
| | | | SL | Ind'l | | | 4 | |
| $t_{CDR}$ [5] | Chip Deselect to Data Retention Time | | | | 0 | | | ns |
| $t_R$ [6] | Operation Recovery Time | | | | $t_{RC}$ | | | ns |

## Data Retention Waveform

**Figure 3. Data Retention Waveform [7]**




**Notes**

5. Tested initially and after any design or process changes that may affect these parameters.
6. Full device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(Min)}$ > 100 µs or stable at $V_{CC(Min)}$ > 100 µs.
7. $\overline{BHE}$. $\overline{BLE}$ is the AND of $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling chip enable signals or by disabling $\overline{BHE}$ and $\overline{BLE}$.

## Switching Characteristics

Over the operating range [8]

| Parameter | Description | 55 ns | | 70 ns | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| **Read Cycle** | | | | | | |
| $t_{RC}$ | Read Cycle Time | 55 | | 70 | | ns |
| $t_{AA}$ | Address to Data Valid | | 55 | | 70 | ns |
| $t_{OHA}$ | Data Hold From Address Change | 10 | | 10 | | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to Data Valid | | 55 | | 70 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 25 | | 35 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low-Z [9] | 5 | | 5 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High-Z [9, 10] | | 20 | | 25 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to Low-Z [9] | 10 | | 10 | | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to High-Z [9, 10] | | 20 | | 25 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to Power Up | 0 | | 0 | | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to Power Down | | 55 | | 70 | ns |
| $t_{DBE}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to Data Valid | | 55 | | 70 | ns |
| $t_{LZBE}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to Low-Z [9, 11] | 5 | | 5 | | ns |
| $t_{HZBE}$ | $\overline{BLE}$/$\overline{BHE}$ HIGH to High-Z [9, 10] | | 20 | | 25 | ns |
| **Write Cycle** [12] | | | | | | |
| $t_{WC}$ | Write Cycle Time | 55 | | 70 | | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to Write End | 45 | | 60 | | ns |
| $t_{AW}$ | Address Setup to Write End | 45 | | 60 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | 0 | | ns |
| $t_{SA}$ | Address Setup to Write Start | 0 | | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 40 | | 45 | | ns |
| $t_{BW}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to Write End | 50 | | 60 | | ns |
| $t_{SD}$ | Data Setup to Write End | 25 | | 30 | | ns |
| $t_{HD}$ | Data Hold From Write End | 0 | | 0 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High-Z [9, 10] | | 20 | | 25 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low-Z [9] | 10 | | 10 | | ns |

**Notes**

8. Test conditions assume signal transition time of 5 ns or less, timing reference levels of $V_{CC(Typ)}/2$, input pulse levels of 0 to $V_{CC(Typ)}$, and output loading of the specified $I_{OL}/I_{OH}$ and 30 pF load capacitance.
9. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any given device.
10. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the output enters a high-impedance state.
11. If both byte enables are toggled together, this value is 10 ns.
12. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$, and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing are referenced to the edge of the signal that terminates the write.

## Switching Waveforms

**Figure 4. Read Cycle 1: Address Transition Controlled** [13, 14]

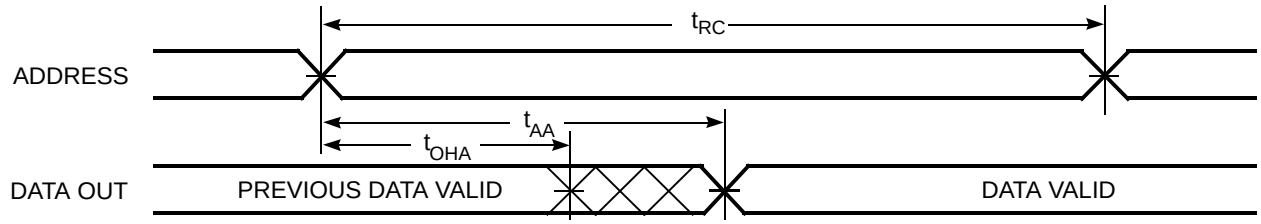
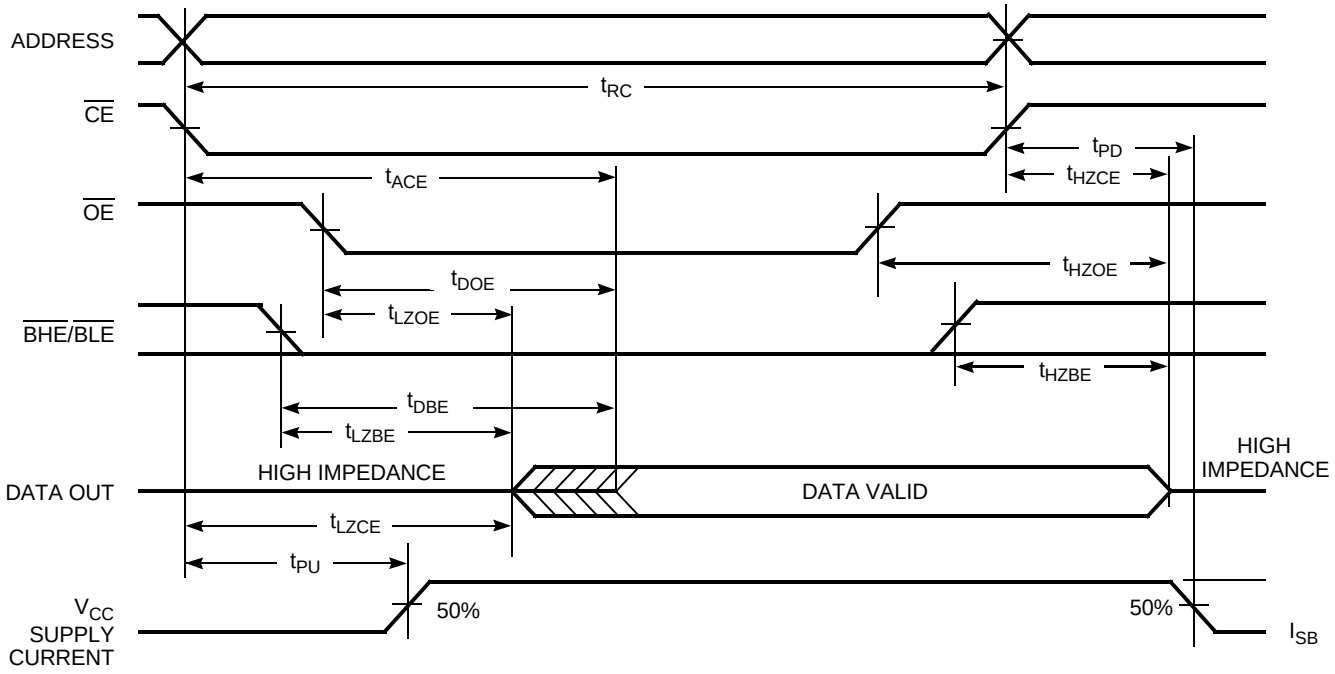



**Figure 5. Read Cycle 2: $\overline{OE}$ Controlled** [14, 15]




**Notes**
13. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE}$ = $V_{IL}$.
14. $\overline{WE}$ is HIGH for read cycle.
15. Address valid before or similar to $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

## Switching Waveforms (continued)

**Figure 6. Write Cycle 1: $\overline{WE}$ Controlled** [12, 16, 17]

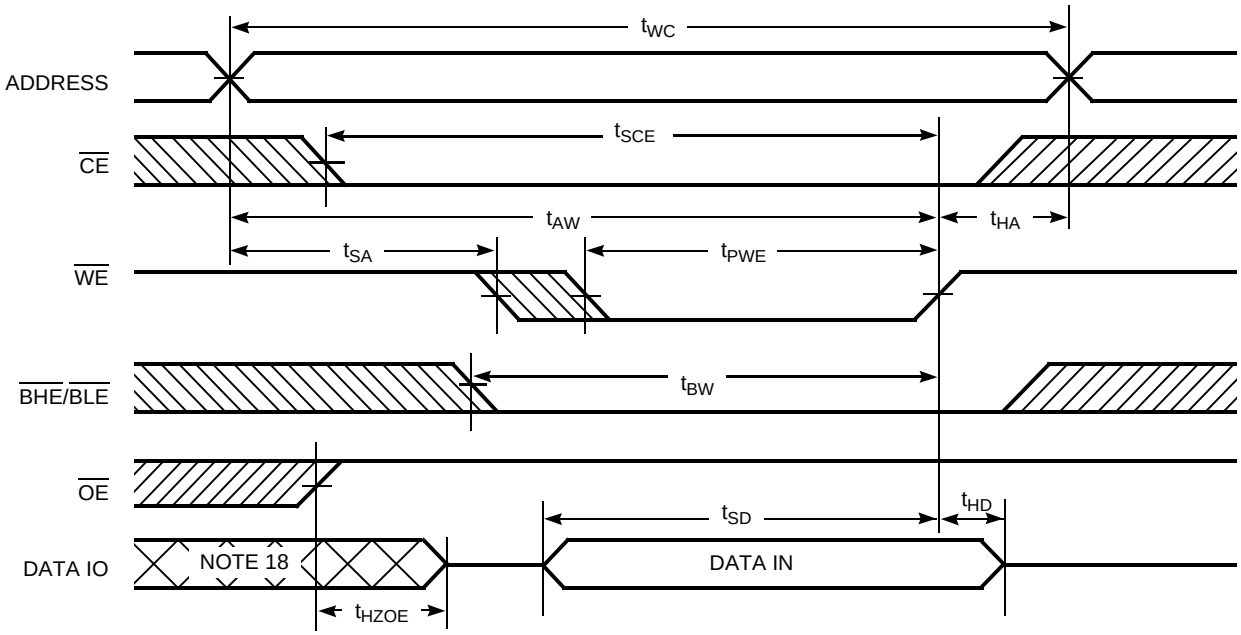
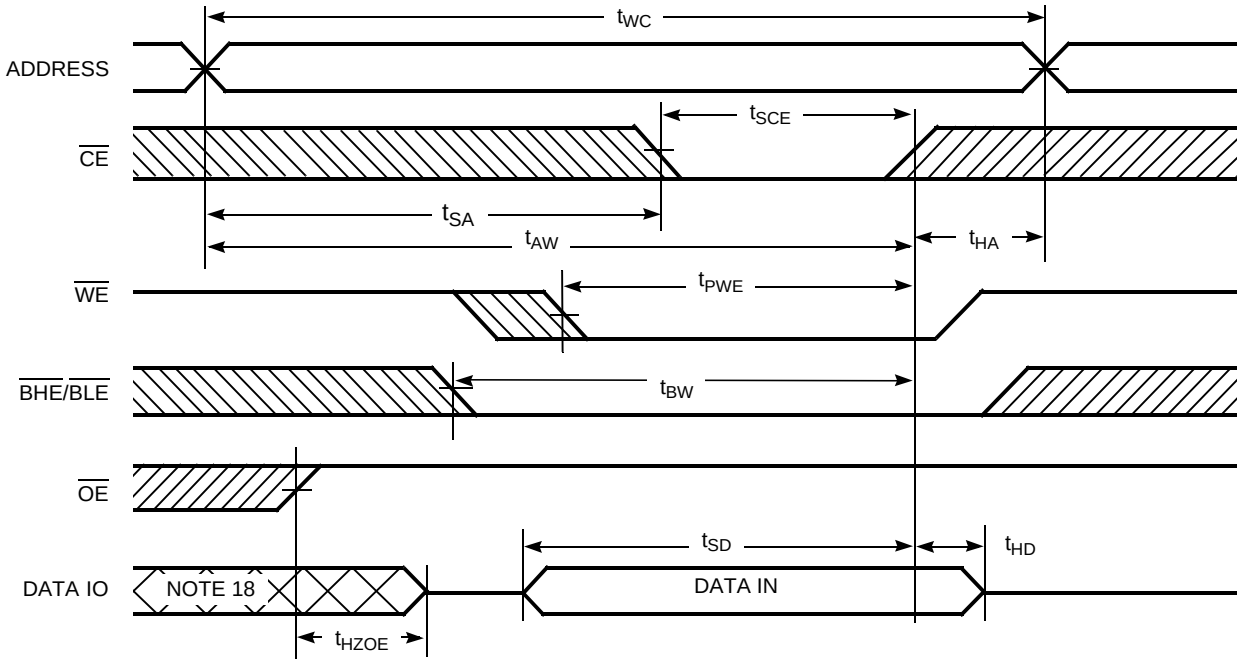



**Figure 7. Write Cycle 2: $\overline{CE}$ Controlled** [12, 16, 17]




**Notes**
16. Data IO is high impedance if $\overline{OE}$ = $V_{IH}$.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = $V_{IH}$, the output remains in a high-impedance state.
18. During this period, the IOs are in an output state. Do not apply input signals.

## Switching Waveforms (continued)

**Figure 8. Write Cycle 3: $\overline{WE}$ Controlled, $\overline{OE}$ LOW [17]**

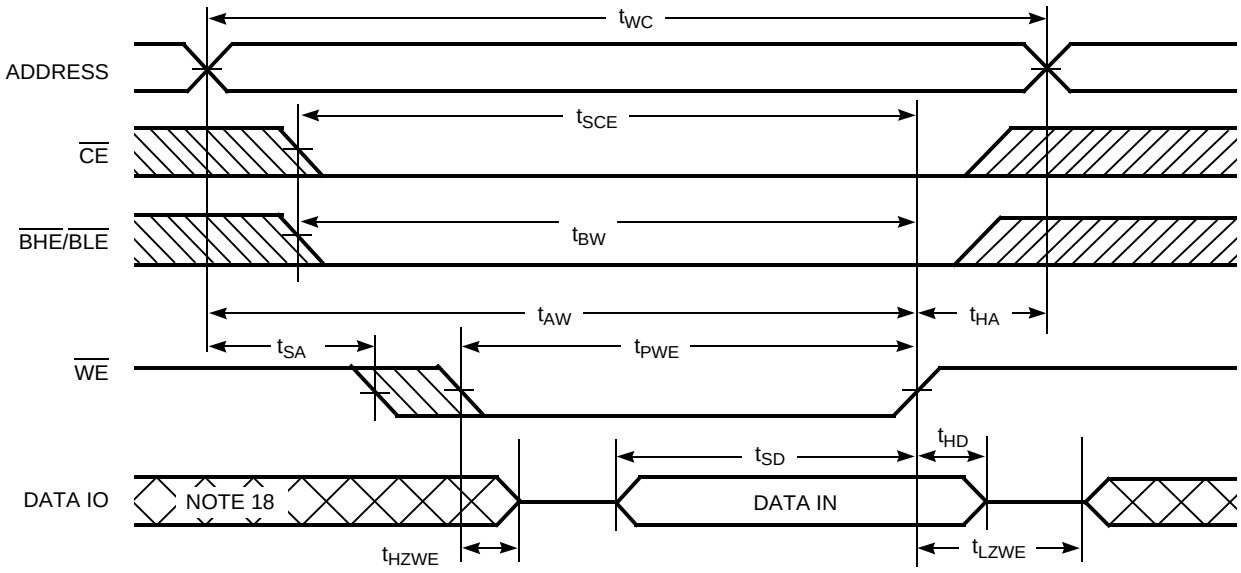
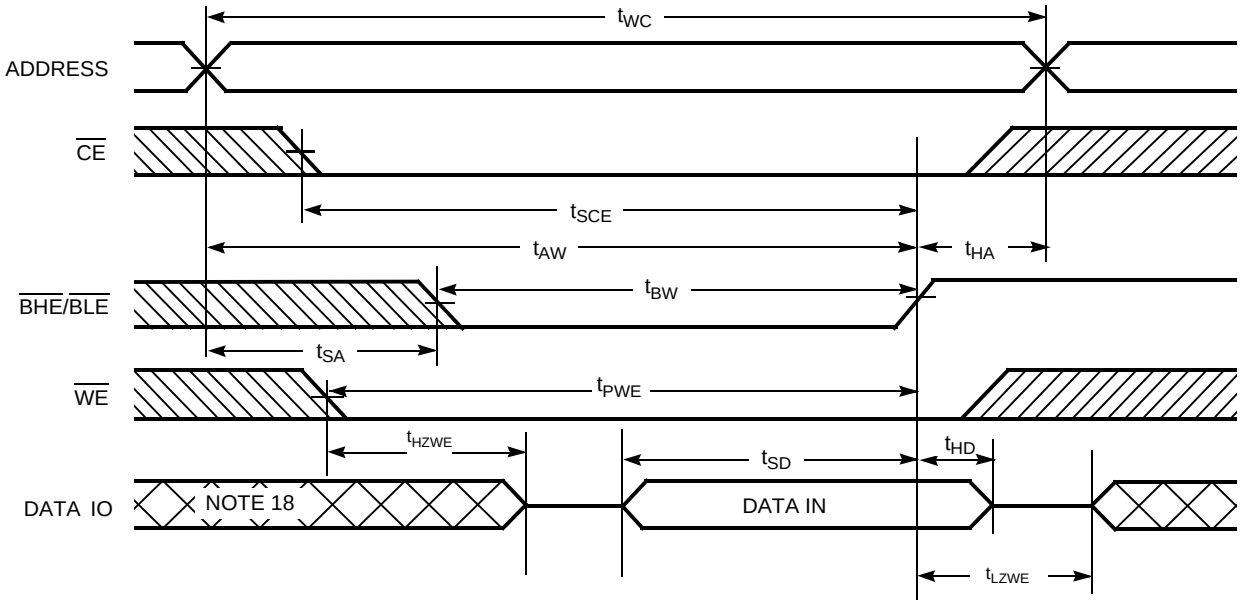



**Figure 9. Write Cycle 4: $\overline{BHE}$/$\overline{BLE}$ Controlled, $\overline{OE}$ LOW [17]**



## Truth Table

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs or Outputs | Mode | Power |
|---|---|---|---|---|---|---|---|
| H | X | X | X | X | High-Z | Deselect or Power Down | Standby ($I_{SB}$) |
| X | X | X | H | H | High-Z | Deselect or Power Down | Standby ($I_{SB}$) |
| L | H | L | L | L | Data Out ($IO_0$–$IO_{15}$) | Read | Active ($I_{CC}$) |
| L | H | L | H | L | Data Out ($IO_0$–$IO_7$); $IO_8$–$IO_{15}$ in High-Z | Read | Active ($I_{CC}$) |
| L | H | L | L | H | Data Out ($IO_8$–$IO_{15}$); $IO_0$–$IO_7$ in High- Z | Read | Active ($I_{CC}$) |
| L | H | H | L | L | High-Z | Output Disabled | Active ($I_{CC}$) |
| L | H | H | H | L | High-Z | Output Disabled | Active ($I_{CC}$) |
| L | H | H | L | H | High-Z | Output Disabled | Active ($I_{CC}$) |
| L | L | X | L | L | Data In ($IO_0$–$IO_{15}$) | Write | Active ($I_{CC}$) |
| L | L | X | H | L | Data In ($IO_0$–$IO_7$); $IO_8$–$IO_{15}$ in High-Z | Write | Active ($I_{CC}$) |
| L | L | X | L | H | Data In ($IO_8$–$IO_{15}$); $IO_0$–$IO_7$ in High-Z | Write | Active ($I_{CC}$) |

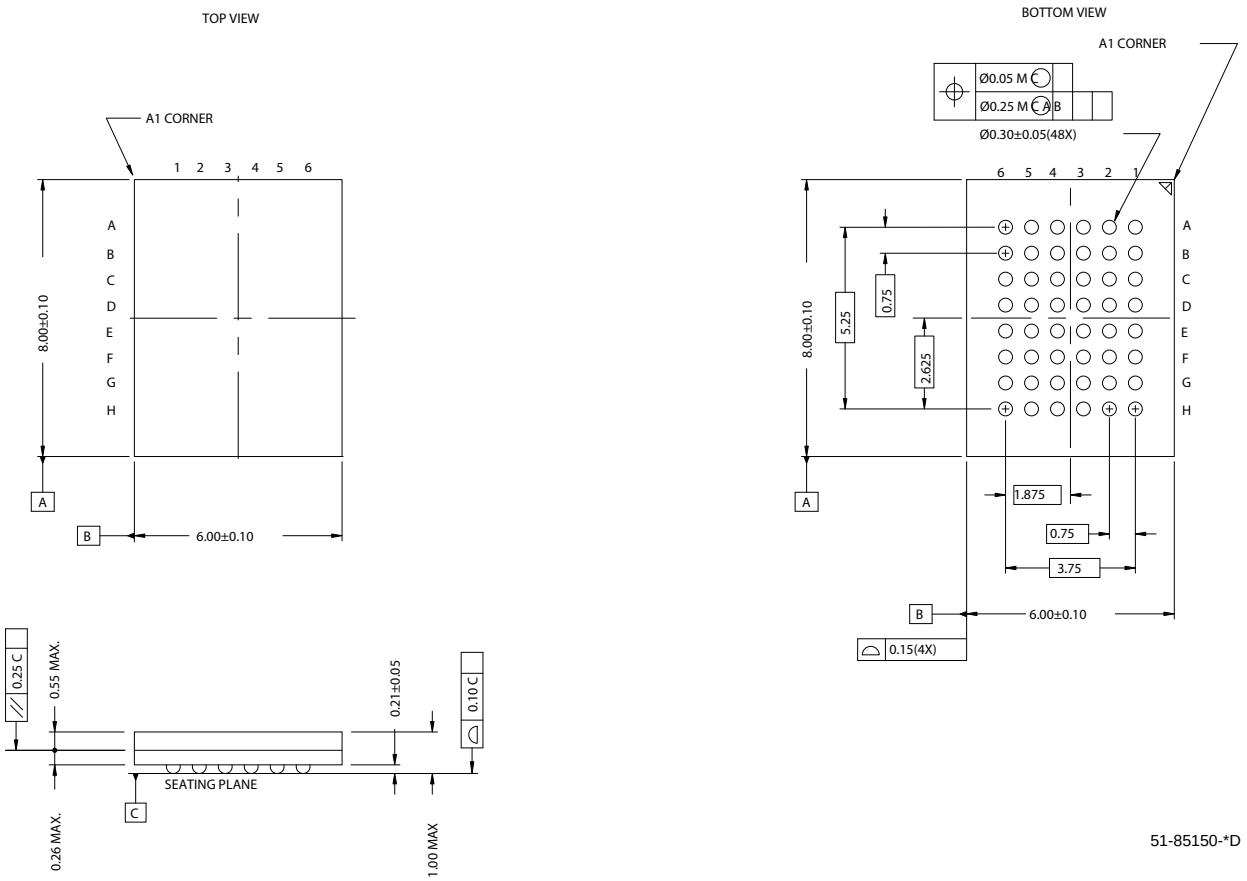
## Ordering Information

Contact your local Cypress sales representative for availability of these parts

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 55 | CY62137CV30LL-55BVI | 51-85150 | 48-ball FBGA (6 x 8 x 1 mm) | Industrial |
| | CY62137CV30LL-55BVXI | | 48-ball FBGA (6 x 8 x 1 mm), Pb-free | |
| | CY62137CV33LL-55BVI | | 48-ball FBGA (6 x 8 x 1 mm) | |
| 70 | CY62137CV30LL-70BAI | 51-85096 | 48-ball FBGA (7 x 7 x 1.2 mm) | Industrial |
| | CY62137CV30LL-70BVI | 51-85150 | 48-ball FBGA (6 x 8 x 1 mm) | |
| | CY62137CVSL-70BAI | 51-85096 | 48-ball FBGA (7 x 7 x 1.2 mm) | |
| | CY62137CVSL-70BAXI | | 48-ball FBGA (7 x 7 x 1.2 mm), Pb-free | |
| | CY62137CV30LL-70BAE | 51-85096 | 48-ball FBGA (7 x 7 x 1.2 mm) | Automotive |
| | CY62137CV30LL-70BVE | 51-85150 | 48-ball FBGA (6 x 8 x 1 mm) | |
| | CY62137CV30LL-70BVXE | | 48-ball FBGA (6 x 8 x 1 mm), Pb-free | |

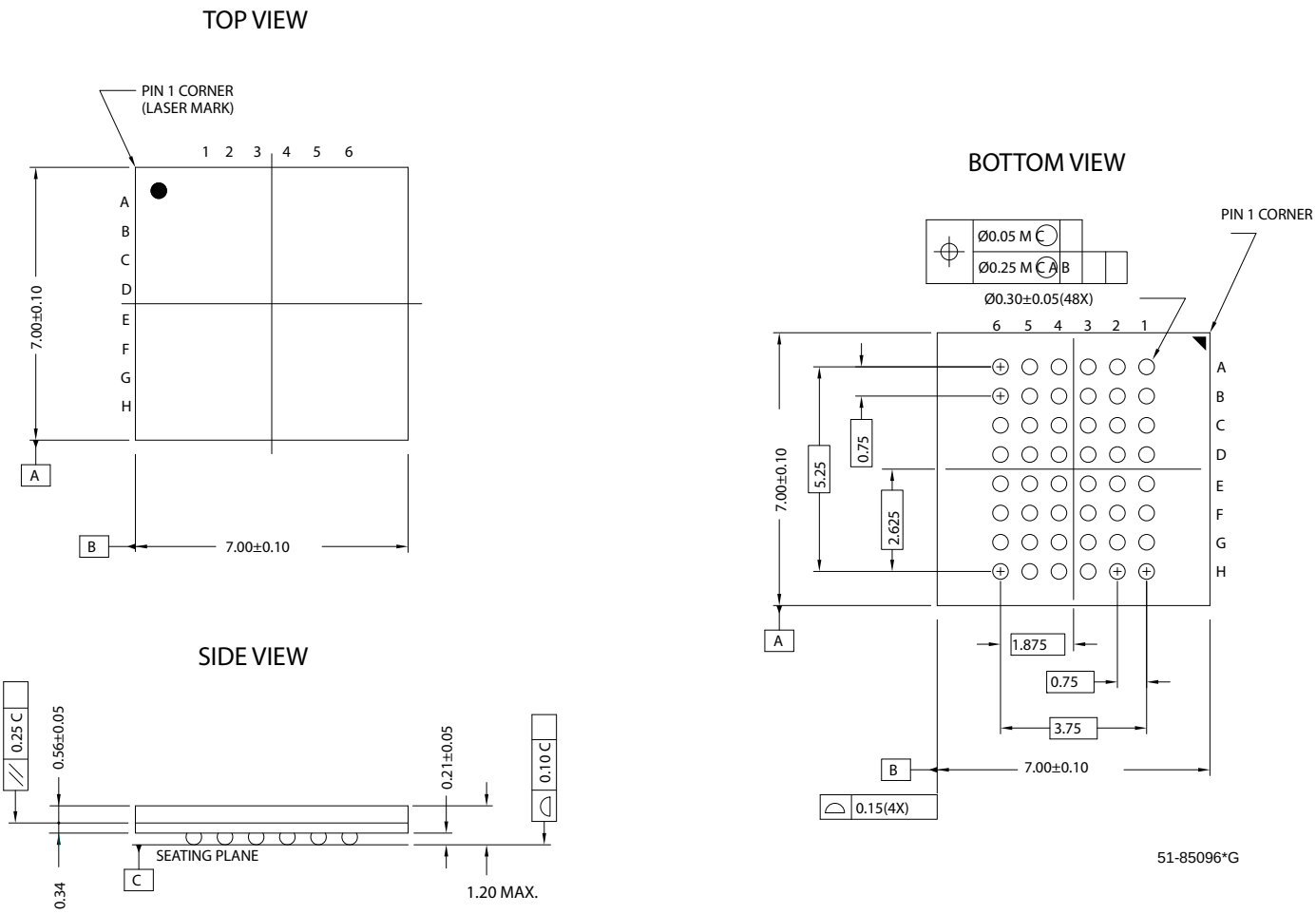
## Package Diagrams

**Figure 10. 48-Ball FBGA (6 x 8 x 1 mm)**



## Package Diagrams (continued)

**Figure 11. 48-Ball FBGA (7 x 7 x 1.2 mm)**



## Document History Page

| Document Title: CY62137CV30/33 MoBL® and CY62137CV MoBL 2-Mbit (128K x 16) Static RAM<br>Document Number: 38-05201 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 112393 | 02/19/02 | GAV | New Data Sheet (advance information) |
| *A | 114015 | 04/25/02 | JUI | Added BV package diagram<br>Changed from Advance Information to Preliminary |
| *B | 117064 | 07/12/02 | MGN | Changed from Preliminary to Final |
| *C | 118122 | 09/10/02 | MGN | Added new part number: CY62137CV with wider voltage (2.7V – 3.6V)<br>Added new SL power bin for new part number<br>For $T_{AA}$ = 55 ns, improved $t_{PWE}$ min from 45 ns to 40 ns<br>For $T_{AA}$ = 70 ns, improved $t_{PWE}$ min from 50 ns to 45 ns<br>For $T_{AA}$ = 70 ns, improved $t_{LZWE}$ min from 5 ns to 10 ns |
| *D | 118761 | 09/23/02 | MGN | Improved Typ $I_{CC}$ spec to 7 mA (for 55 ns) and 5.5 mA (for 70 ns)<br>Improved Max $I_{CC}$ spec to 15 mA (for 55 ns) and 12 mA (for 70 ns)<br>For $T_{AA}$ = 55 ns, improved $t_{LZWE}$ min from 5 ns to 10 ns<br>Changed upper spec for Supply Voltage to Ground Potential to $V_{CC(Max)}$ + 0.5V<br>Changed upper spec. for DC Voltage Applied to Outputs in High-Z State and DC Input Voltage to $V_{CC}$ + 0.3V |
| *E | 343877 | See ECN | PCI | Added Automotive Information in Operating Range, DC, and Ordering Information Table |
| *F | 419237 | See ECN | ZSD | Changed the address of Cypress Semiconductor Corporation on Page 1 from “3901 North First Street” to “198 Champion Court”<br>Updated the ordering information table and replaced the Package name column with Package diagram |
| *G | 486789 | See ECN | VKN | Removed part number CY62137CV25 from the product offering<br>Updated the ordering information table |
| *H | 1665045 | See ECN | VKN/SFV | Changed $V_{CC}$ range for CY7C62137CV from 2.7–3.6V to 2.9–3.6V |