# CY62128B
## MoBL®
# 1-Mbit (128K x 8) Static RAM

## Features

- **Temperature Ranges**
  - **Commercial: 0°C to 70°C**
  - **Industrial: –40°C to 85°C**
  - **Automotive: –40°C to 125°C**
- **4.5V–5.5V operation**
- **CMOS for optimum speed/power**
- **Low active power (70 ns, LL version, Commercial, Industrial)**
  - **82.5 mW (max.) (15 mA)**
- **Low standby power (70 ns, LL version, Commercial, Industrial)**
  - **110 μW (max.) (15 μA)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$, $CE_2$, and $\overline{OE}$ options**

## Functional Description[1]

The CY62128B is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}_1$), an active HIGH Chip Enable ($CE_2$), an active LOW Output Enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

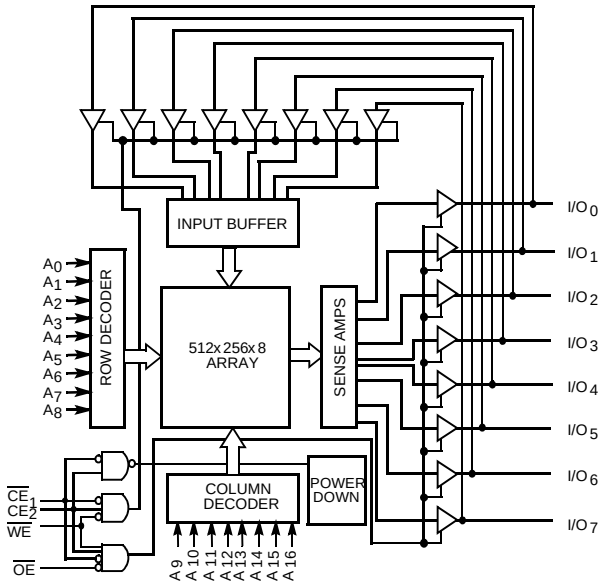
Writing to the device is accomplished by taking Chip Enable One ($\overline{CE}_1$) and Write Enable ($\overline{WE}$) inputs LOW and Chip Enable Two ($CE_2$) input HIGH. Data on the eight I/O pins ($I/O_0$ through $I/O_7$) is then written into the location specified on the address pins ($A_0$ through $A_{16}$).

Reading from the device is accomplished by taking Chip Enable One ($\overline{CE}_1$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) and Chip Enable Two ($CE_2$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ($I/O_0$ through $I/O_7$) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or $CE_2$ LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, $CE_2$ HIGH, and $\overline{WE}$ LOW).

The CY62128B is available in a standard 450-mil-wide SOIC, 32-pin TSOP type I and STSOP packages.

## Logic Block Diagram

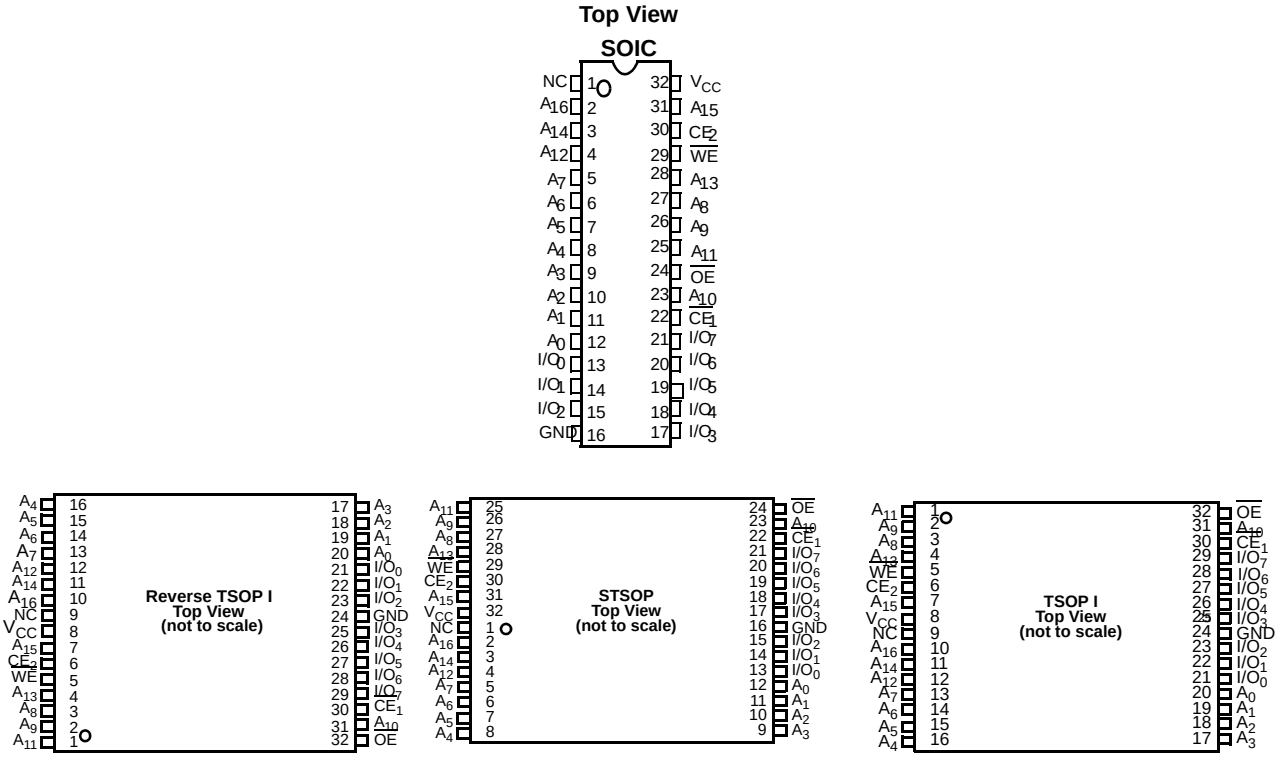



**Note:**
1. For best-practice recommendations, please refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com.

## Product Portfolio

| Product | | $V_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Operating, $I_{CC}$ (mA) | | Standby, $I_{SB2}$ (µA) | |
| | | Min. | Typ.[2] | Max. | | Typ.[2] | Max. | Typ.[2] | Max. |
| CY62128BLL | Industrial | 4.5 | 5.0 | 5.5 | 55 | 7.5 | 20 | 2.5 | 15 |
| | Industrial | | | | 70 | 6 | 15 | 2.5 | 15 |
| | Automotive | | | | 70 | 6 | 25 | 2.5 | 25 |

## Pin Configurations




## Pin Definitions

| | |
|---|---|
| Input | **$A_0$-$A_{16}$**. Address Inputs |
| Input/Output | **$I/O_0$-$I/O_7$**. Data lines. Used as input or output lines depending on operation |
| Input/Control | **$\overline{WE}$**. Write Enable, Active LOW. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted. |
| Input/Control | **$\overline{CE_1}$**. Chip Enable 1, Active LOW. |
| Input/Control | **$CE_2$**. Chip Enable 2, Active HIGH. |
| Input/Control | **$\overline{OE}$**. Output Enable, Active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins |
| Ground | **GND**. Ground for the device |
| Power Supply | **$V_{CC}$**. Power supply for the device |

**Note:**
2. Typical values are included for reference only and are not tested or guaranteed. Typical values are an average of the distribution across normal production variations as measured at $V_{CC}$ = 5.0V, $T_A$ = 25°C, and $t_{AA}$ = 70 ns.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on $V_{CC}$ to Relative GND[3] .... –0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State[3].....–0.5V to $V_{CC}$ + 0.5V

DC Input Voltage[3].....–0.5V to $V_{CC}$ + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage.....> 2001V (per MIL-STD-883, Method 3015)

Latch-up Current.....> 200 mA

## Operating Range

| Range | Ambient Temperature ($T_A$)[4] | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 5V ± 10% |
| Industrial | –40°C to +85°C | 5V ± 10% |
| Automotive | –40°C to +125°C | 5V ± 10% |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | CY62128B-55 Min. | CY62128B-55 Typ.[2] | CY62128B-55 Max. | CY62128B-70 Min. | CY62128B-70 Typ.[2] | CY62128B-70 Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = –1.0 mA | | 2.4 | | | 2.4 | | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 2.1 mA | | | | 0.4 | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2.2 | | $V_{CC}$ + 0.3 | 2.2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage[3] | | | –0.3 | | 0.8 | –0.3 | | 0.8 | V |
| $I_{IX}$ | Input Load Current | GND ≤ $V_I$ ≤ $V_{CC}$ | | –1 | | +1 | –1 | | +1 | µA |
| | | | Automotive | | | | –10 | | +10 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$, Output Disabled | | –1 | | +1 | –1 | | +1 | µA |
| | | | Automotive | | | | –10 | | +10 | µA |
| $I_{OS}$ | Output Short Circuit Current[5] | $V_{CC}$ = Max., $V_{OUT}$ = GND | | | | –300 | | | –300 | mA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = $1/t_{RC}$ | Industrial, Commercial | | 7.5 | 20 | | 6 | 15 | mA |
| | | | Automotive | | | | | 6 | 25 | mA |
| $I_{SB1}$ | Automatic CE Power-down Current —TTL Inputs | Max. $V_{CC}$, $\overline{CE_1}$ ≥ $V_{IH}$ or $CE_2$ ≤ $V_{IL}$, $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = $f_{MAX}$ | Industrial Commercial | | 0.1 | 2 | | 0.1 | 1 | mA |
| | | | Automotive | | | | | 0.1 | 2 | mA |
| $I_{SB2}$ | Automatic CE Power-down Current —CMOS Inputs | Max. $V_{CC}$, $\overline{CE_1}$ ≥ $V_{CC}$ – 0.3V, or $CE_2$ ≤ 0.3V, $V_{IN}$ ≥ $V_{CC}$ – 0.3V, or $V_{IN}$ ≤ 0.3V, f = 0 | Industrial Commercial | | 2.5 | 15 | | 2.5 | 15 | µA |
| | | | Automotive | | | | | 2.5 | 25 | µA |

**Notes:**

3. $V_{IL}$ (min.) = –2.0V for pulse durations of less than 20 ns.
4. $T_A$ is the "Instant On" case temperature.
5. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

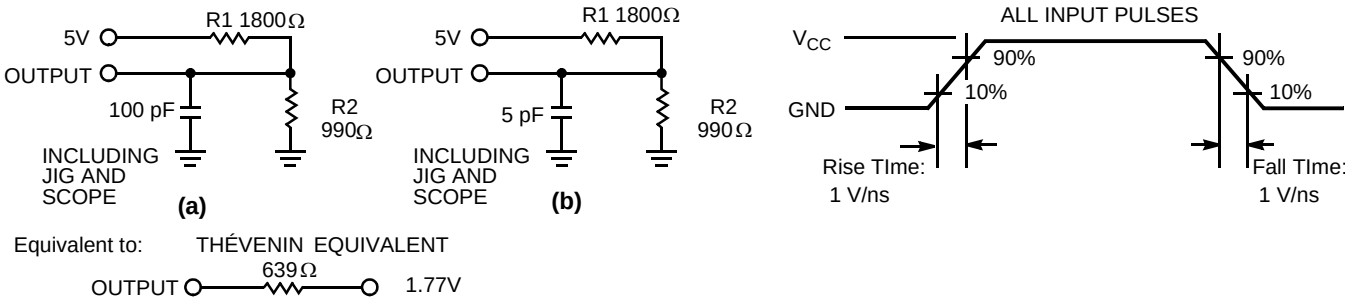
## Thermal Resistance[6]

| Parameter | Description | Test Conditions | 32 SOIC | 32 TSOP | 32 STSOP | 32 RTSOP | Unit |
|---|---|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51. | 66.17 | 97.44 | 105.14 | 97.44 | °C/W |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case) | | 30.87 | 26.05 | 14.09 | 26.05 | °C/W |

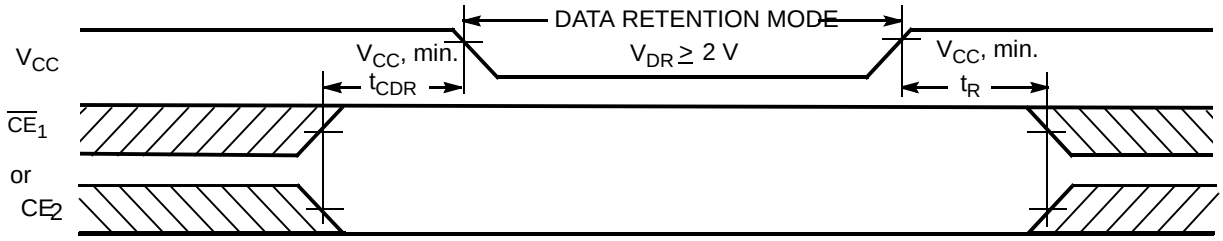
## Capacitance[6]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 5.0V | 9 | pF |
| $C_{OUT}$ | Output Capacitance | | 9 | pF |

## AC Test Loads and Waveforms




## Data Retention Waveform




## Data Retention Characteristics (Over the Operating Range for "LL" version only)

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | | 2.0 | | | V |
| $I_{CCDR}$ | Data Retention Current | $V_{CC} = V_{DR} = 2.0V$, $\overline{CE_1} \geq V_{CC} - 0.3V$, or $CE_2 \leq 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or, $V_{IN} \leq 0.3V$ | | 1.5 | 15 | µA |
| $t_{CDR}$ | Chip Deselect to Data Retention Time | | 0 | | | ns |
| $t_R$ | Operation Recovery Time | | 70 | | | ns |

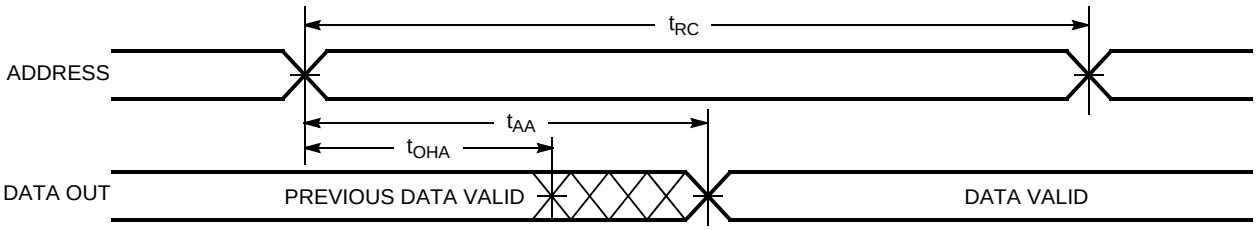
**Note:**
6. Tested initially and after any design or process changes that may affect these parameters.

## Switching Characteristics[7] Over the Operating Range

| Parameter | Description | 62128B-55 | | 62128B-70 | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| **READ CYCLE** | | | | | | |
| $t_{RC}$ | Read Cycle Time | 55 | | 70 | | ns |
| $t_{AA}$ | Address to Data Valid | | 55 | | 70 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 5 | | 5 | | ns |
| $t_{ACE}$ | $\overline{CE}_1$ LOW to Data Valid, $CE_2$ HIGH to Data Valid | | 55 | | 70 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 20 | | 35 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z | 0 | | 0 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z[7, 9] | | 20 | | 25 | ns |
| $t_{LZCE}$ | $\overline{CE}_1$ LOW to Low Z, $CE_2$ HIGH to Low Z[9] | 5 | | 5 | | ns |
| $t_{HZCE}$ | $\overline{CE}_1$ HIGH to High Z, $CE_2$ LOW to High Z[8, 9] | | 20 | | 25 | ns |
| $t_{PU}$ | $\overline{CE}_1$ LOW to Power-up, $CE_2$ HIGH to Power-up | 0 | | 0 | | ns |
| $t_{PD}$ | $\overline{CE}_1$ HIGH to Power-down, $CE_2$ LOW to Power-down | | 55 | | 70 | ns |
| **WRITE CYCLE**[10] | | | | | | |
| $t_{WC}$ | Write Cycle Time | 55 | | 70 | | ns |
| $t_{SCE}$ | $\overline{CE}_1$ LOW to Write End, $CE_2$ HIGH to Write End | 45 | | 60 | | ns |
| $t_{AW}$ | Address Set-up to Write End | 45 | | 60 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | 0 | | ns |
| $t_{SA}$ | Address Set-up to Write Start | 0 | | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 45 | | 50 | | ns |
| $t_{SD}$ | Data Set-up to Write End | 25 | | 30 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | 0 | | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z[9] | 5 | | 5 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z[8, 9] | | 20 | | 25 | ns |

## Switching Waveforms

### Read Cycle No.1[12, 13]

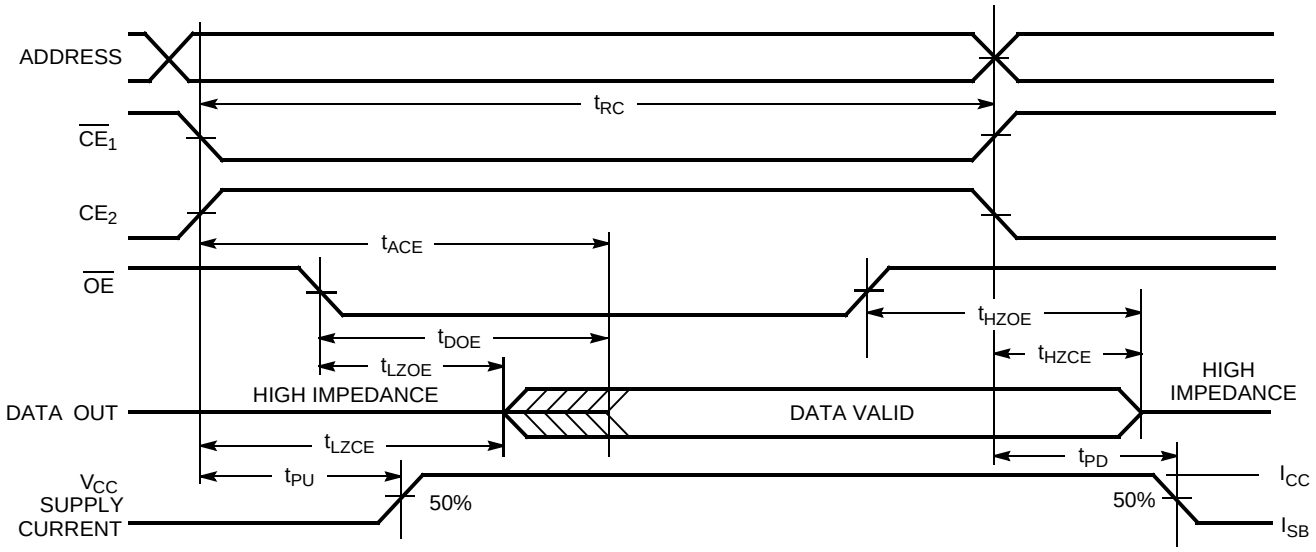



**Notes:**

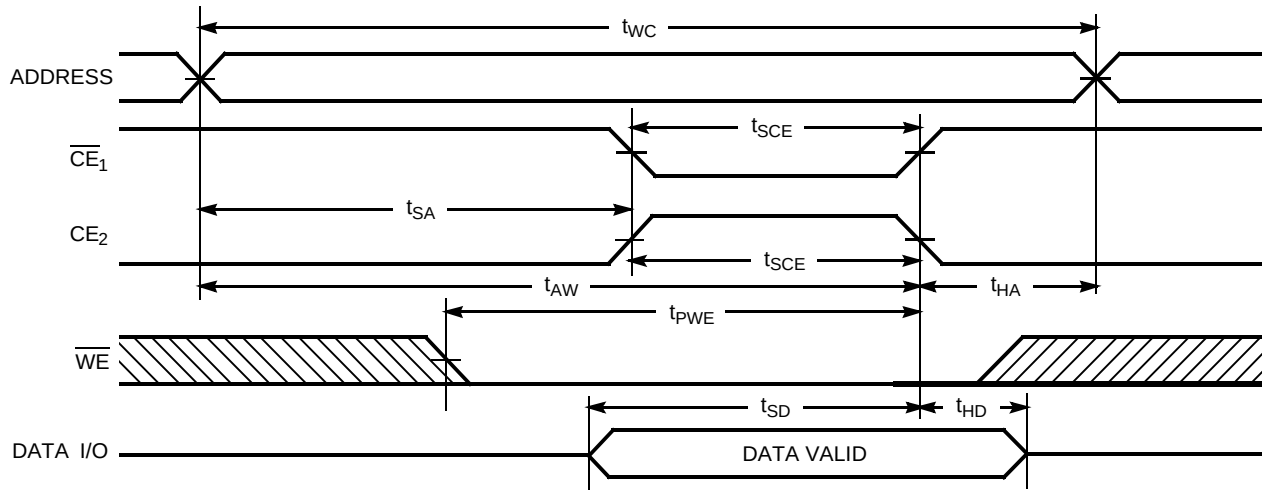
7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified $I_{OL}/I_{OH}$ and 100-pF load capacitance.
8. $t_{HZOE}$, $t_{HZCE}$, and $t_{HZWE}$ are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any given device.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $CE_2$ HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ must be LOW and $CE_2$ HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
11. No input may exceed $V_{CC}$ + 0.5V.
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
13. $\overline{WE}$ is HIGH for read cycle.

## Switching Waveforms (continued)

### Read Cycle No. 2 ($\overline{OE}$ Controlled)[13, 14]



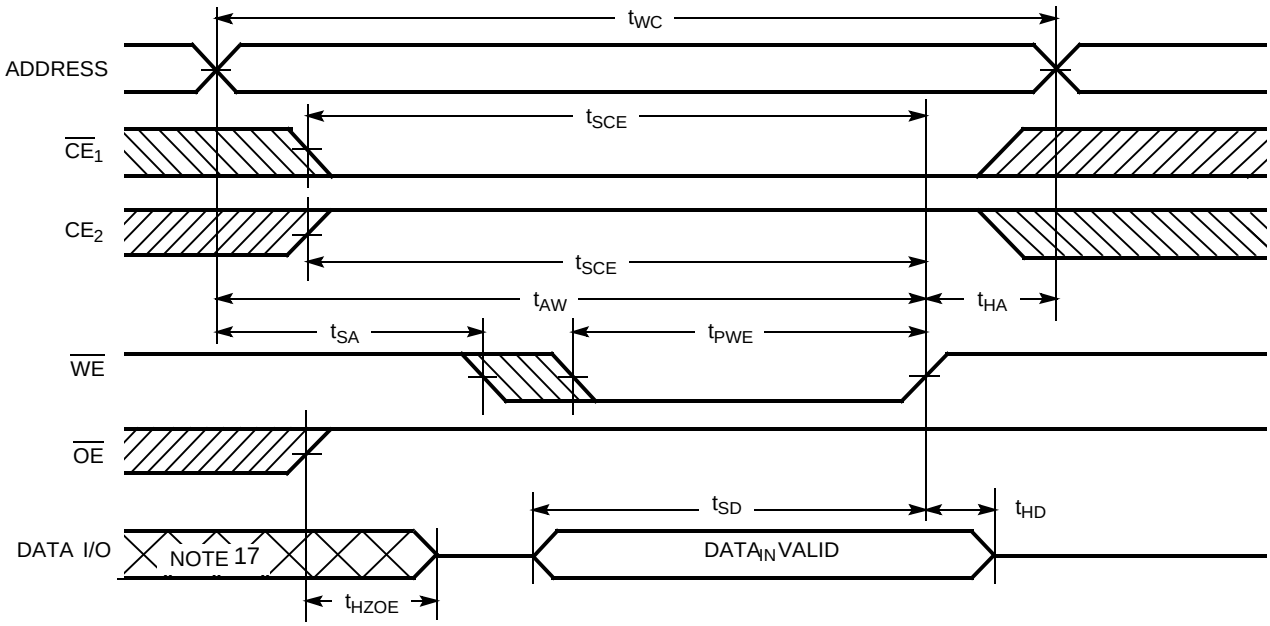

### Write Cycle No. 1 ($\overline{CE_1}$ or $CE_2$ Controlled)[15, 16]



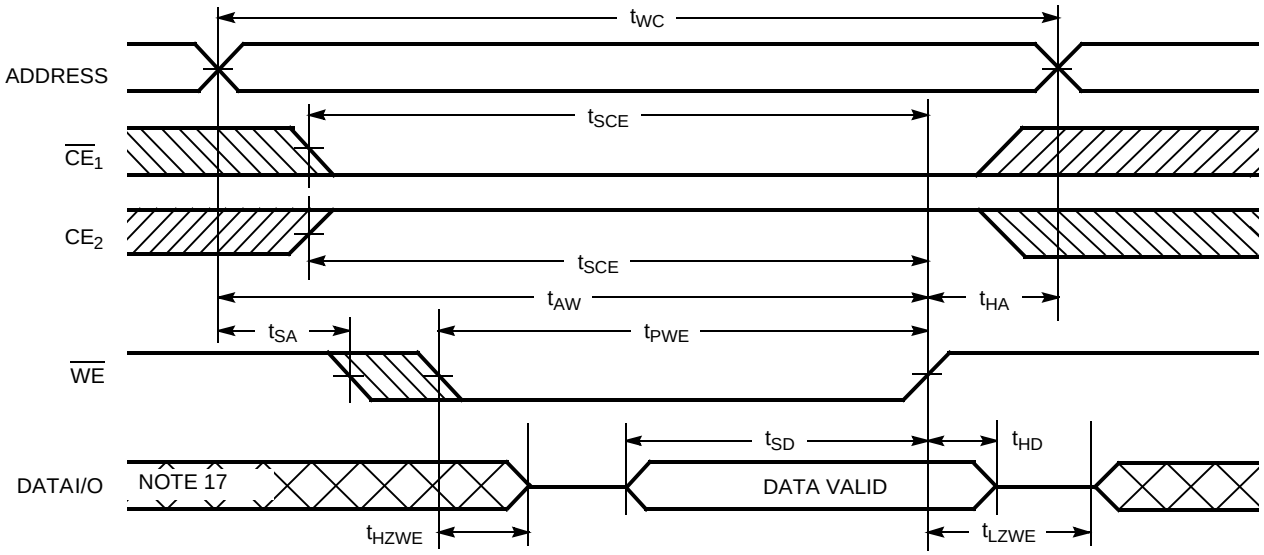

**Notes:**
14. Address valid prior to or coincident with $\overline{CE_1}$ transition LOW and $CE_2$ transition HIGH.
15. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
16. If $\overline{CE_1}$ goes HIGH or $CE_2$ goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

## Switching Waveforms (continued)

### Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[15, 16]




### Write Cycle No.3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[15, 16]




**Note:**
17. During this period the I/Os are in the output state and input signals should not be applied.

## Truth Table

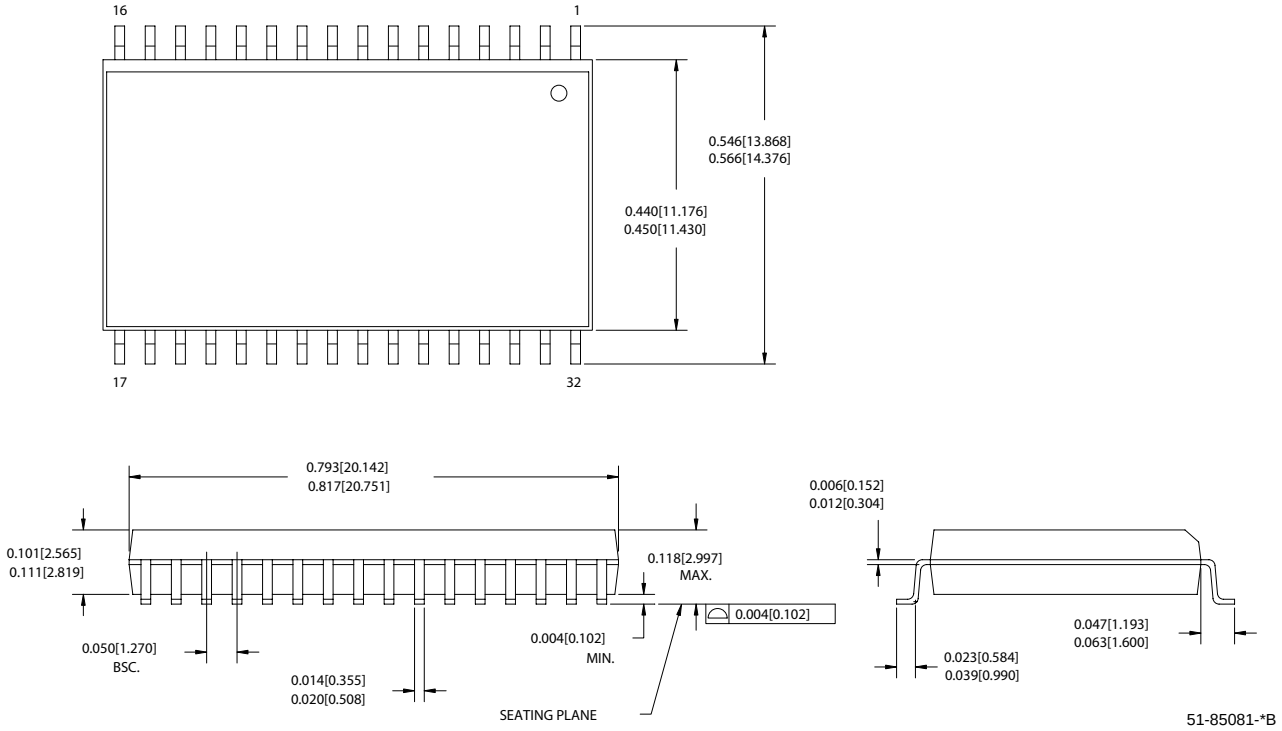
| $\overline{CE_1}$ | $CE_2$ | $\overline{OE}$ | $\overline{WE}$ | $I/O_0$–$I/O_7$ | Mode | Power |
|---|---|---|---|---|---|---|
| H | X | X | X | High Z | Power-down | Standby ($I_{SB}$) |
| X | L | X | X | High Z | Power-down | Standby ($I_{SB}$) |
| L | H | L | H | Data Out | Read | Active ($I_{CC}$) |
| L | H | X | L | Data In | Write | Active ($I_{CC}$) |
| L | H | H | H | High Z | Selected, Outputs Disabled | Active ($I_{CC}$) |

## Ordering Information

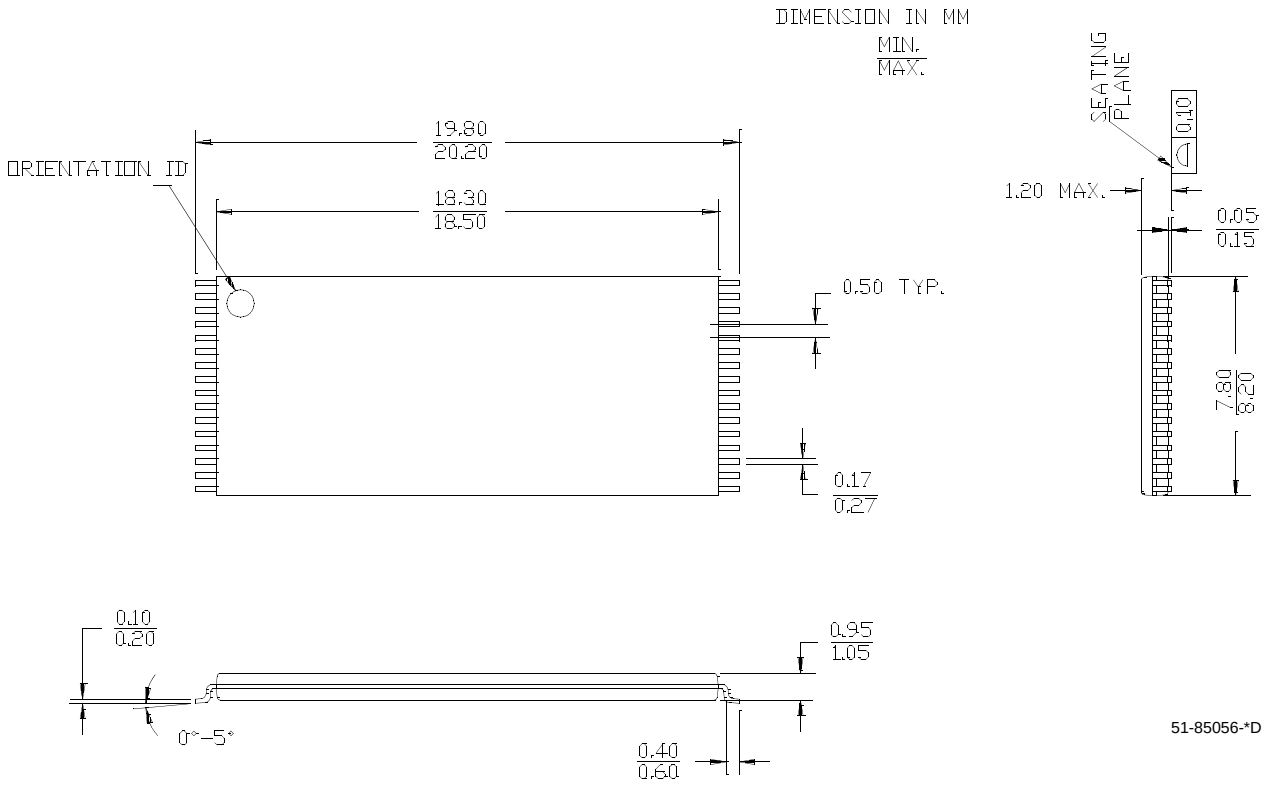
| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 55 | CY62128BLL-55SI | S34 | 32-Lead 450-Mil SOIC | Industrial |
| | CY62128BLL-55SXI | S34 | 32-Lead 450-Mil SOIC (Pb-Free) | Industrial |
| | CY62128BLL-55SC | S34 | 32-Lead 450-Mil SOIC | Commercial |
| | CY62128BLL-55SXC | S34 | 32-Lead 450-Mil SOIC (Pb-Free) | Commercial |
| | CY62128BLL-55ZI | Z32 | 32-Lead TSOP Type I | Industrial |
| | CY62128BLL-55ZXI | Z32 | 32-Lead TSOP Type I (Pb-Free) | Industrial |
| | CY62128BLL-55ZAI | ZA32 | 32-Lead STSOP Type I | Industrial |
| | CY62128BLL-55ZAXI | ZA32 | 32-Lead STSOP Type I (Pb-Free) | Industrial |
| | CY62128BLL-55ZRI | ZR32 | 32-Lead Reverse TSOP Type I | Industrial |
| 70 | CY62128BLL-70SI | S34 | 32-Lead 450-Mil SOIC I | Industrial |
| | CY62128BLL-70SXI | S34 | 32-Lead 450-Mil SOIC I (Pb-Free) | Industrial |
| | CY62128BLL-70SC | S34 | 32-Lead 450-Mil SOIC I | Commercial |
| | CY62128BLL-70SXC | S34 | 32-Lead 450-Mil SOIC I (Pb-Free) | Commercial |
| | CY62128BLL-70SE | S34 | 32-Lead 450-Mil SOIC I | Automotive |
| | CY62128BLL-70SXE | S34 | 32-Lead 450-Mil SOIC I (Pb-Free) | Automotive |
| | CY62128BLL-70ZI | Z32 | 32-Lead TSOP Type I | Industrial |
| | CY62128BLL-70ZC | Z32 | 32-Lead TSOP Type I | Commercial |
| | CY62128BLL-70ZE | Z32 | 32-Lead TSOP Type I | Automotive |
| | CY62128BLL-70ZXE | Z32 | 32-Lead TSOP Type I (Pb-Free) | Automotive |
| | CY62128BLL-70ZAI | ZA32 | 32-Lead STSOP Type I | Industrial |
| | CY62128BLL-70ZAXI | ZA32 | 32-Lead STSOP Type I (Pb-Free) | Industrial |
| | CY62128BLL-70ZAE | ZA32 | 32-Lead STSOP Type I | Automotive |
| | CY62128BLL-70ZAXE | ZA32 | 32-Lead STSOP Type I (Pb-Free) | Automotive |
| | CY62128BLL-70ZRXE | ZR32 | 32-Lead Reverse TSOP Type I (Pb-Free) | Automotive |

## Package Diagrams

### 32-Lead (450 MIL) Molded SOIC S34

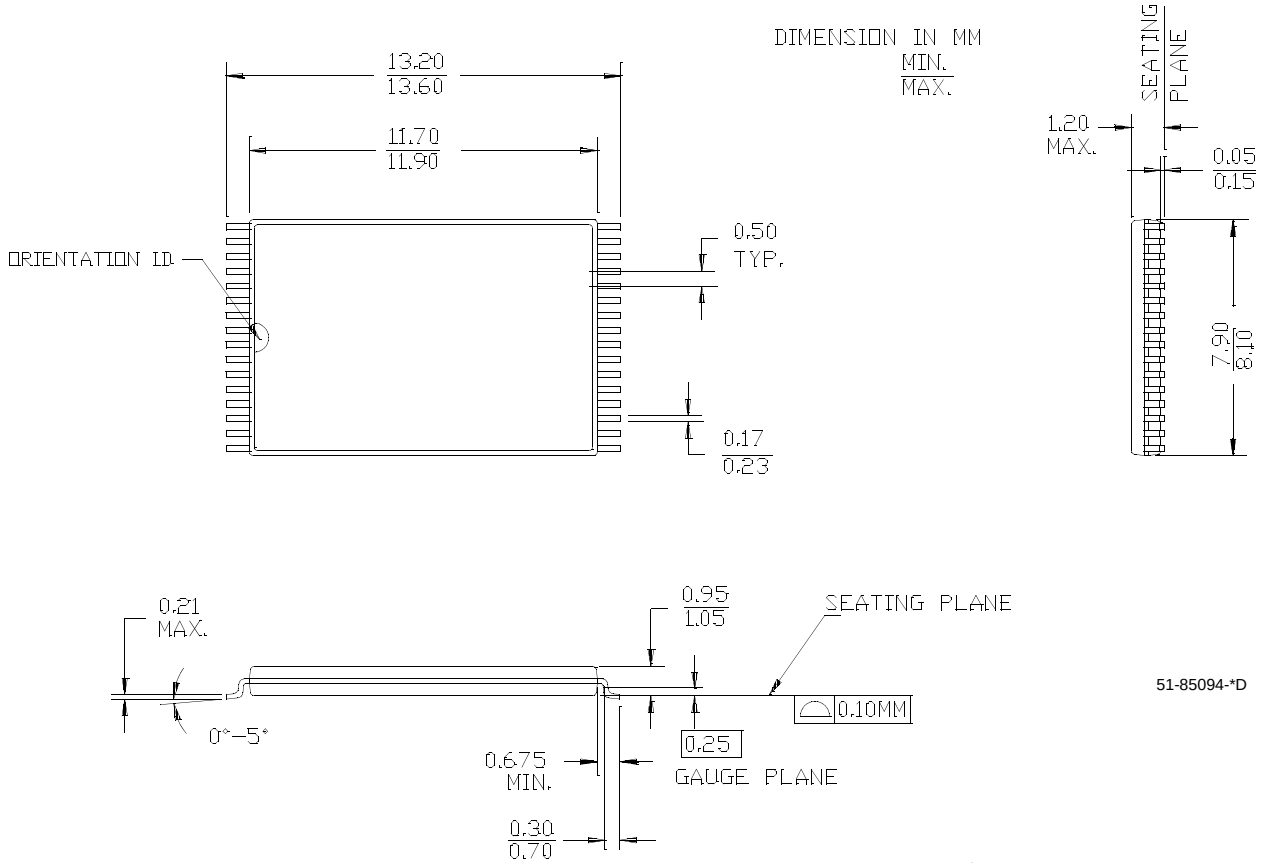



### 32-Lead Thin Small Outline Package Type I (8x20 mm) Z32

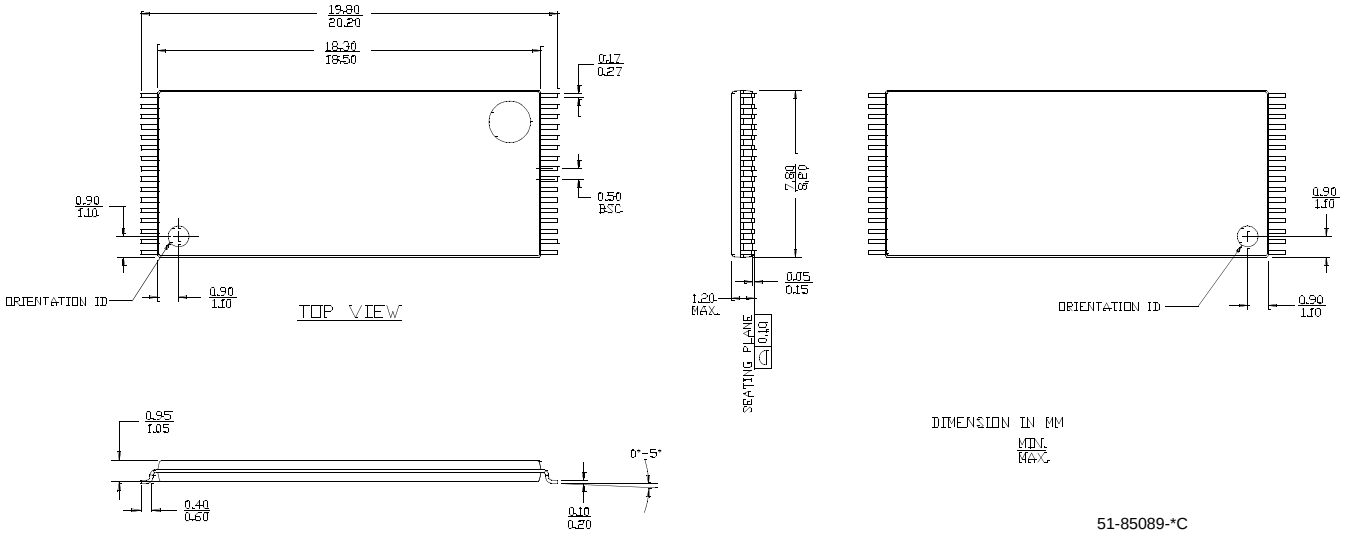


## Package Diagrams (continued)

**32-Lead Shrunk Thin Small Outline Package (8x13.4 mm) ZA32**




**32-Lead Reverse Thin Small Outline Package ZR32**

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## Document History Page

| Document Title: CY62128B MoBL® 1-Mbit (128K x 8) Static RAM<br>Document Number: 38-05300 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 116566 | 06/20/02 | DSG | Changed from Spec number: 38-00524 to 38-05300 |
| *A | 126601 | 06/09/03 | JUI | Changed CE to $\overline{CE}_1$ and added $CE_2 \leq 0.3V$ in Data Retention Characteristics table<br>Removed these part numbers from Ordering Information table:<br>CY62128BLL-55ZC, CY62128BLL-55ZAC, CY62128BLL-55ZRC,<br>CY62128BLL-70ZAC, CY62128BLL-70ZRI, CY62128BLL-70ZRC |
| *B | 239134 | See ECN | AJU | Added Thermal Resistance table<br>Added Automotive product information |
| *C | 334398 | See ECN | SYT | Added Pb-Free part numbers to the Ordering info on Page #8 |