



CYPRESS

**PRELIMINARY**

**CY24119**

**MediaClock™ 27-MHz VCXO Clock Generator**

**Features**

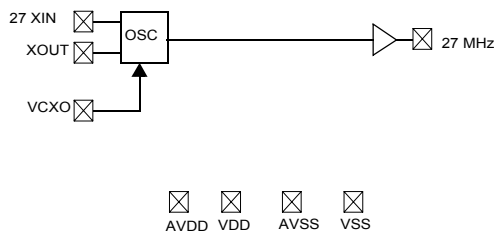
- Low-jitter, high-accuracy output
- VCXO with analog adjust
- 3.3V operation

**Benefits**

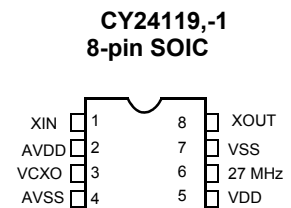
- Meets critical timing requirements in complex system designs
- Large  $\pm 150$  ppm range, better linearity

Part Number	Outputs	Input Frequency Range	Output Frequencies
CY24119	1	27-MHz pullable crystal per Cypress specification	One copy of 27-MHz (3.3V) positive slope VCXO curve
CY24119-1	1	27-MHz pullable crystal per Cypress specification	One copy of 27-MHz (3.3V) negative slope VCXO curve

**Logic Block Diagram**



**Pin Configuration**



**Pin Summary**

Name	Pin Number	Description
$A_{VDD}$	2	Analog Voltage Supply
$V_{DD}$	5	Output Voltage Supply
$A_{VSS}$	4	Analog Ground
$V_{SS}$	7	Output Ground
$X_{IN}$	1	Reference Crystal Input
$V_{CXO}$	3	Analog Control for $V_{CXO}$
$X_{OUT}$	8	Reference Crystal Output
27 MHz	6	27-MHz Clock Output

**Absolute Maximum Conditions**

Parameter	Description	Min.	Max.	Unit
$V_{DD}$	Supply Voltage	-0.5	7.0	V
$T_S$	Storage Temperature <sup>[1]</sup>	-65	125	°C
$T_J$	Junction Temperature		125	°C
	Electrostatic Discharge	2		kV

**Recommended Operating Conditions**

Parameter	Description	Min.	Typ.	Max.	Unit
$V_{DD}, A_{VDD}$	Operating Voltage	3.14	3.3	3.47	V
$T_A$	Ambient Temperature	0		70	°C
$C_{LOAD}$	Max Load Capacitance			15	pF
$f_{REF}$	Reference Frequency	10	27	30	MHz
$t_{PU}$	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05		500	ms

**DC Electrical Characteristics**

Parameter	Name	Description	Min.	Typ.	Max.	Unit
$I_{OH}$	Output HIGH Current	$V_{OH} = V_{DD} - 0.5, V_{DD} = 3.3V$ (source)	12	24		mA
$I_{OL}$	Output LOW Current	$V_{OL} = 0.5, V_{DD} = 3.3V$ (sink)	12	24		mA
$C_{IN}$	Input Capacitance				7	pF
$I_{IZ}$	Input Leakage Current			5		μA
$f_{\Delta XO}$	$V_{CXO}$ Pullability Range		-150		+150	ppm
$V_{VCXO}$	$V_{CXO}$ Input Range		0		$A_{VDD}$	V
$f_{VBW}$	$V_{CXO}$ Input Bandwidth			DC to 200		kHz
$I_{DD}$	Supply Current	Sum of Core and Output Current			13	mA

**Pullable Crystal Specifications**

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
$F_{NOM}$	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut		27		MHz
$C_{LNOM}$	Nominal load capacitance			14		pF
$R_1$	Equivalent series resistance (ESR)	Fundamental mode			25	Ω

**Note:**

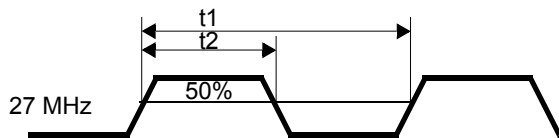
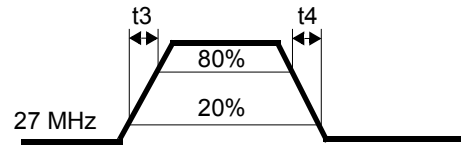
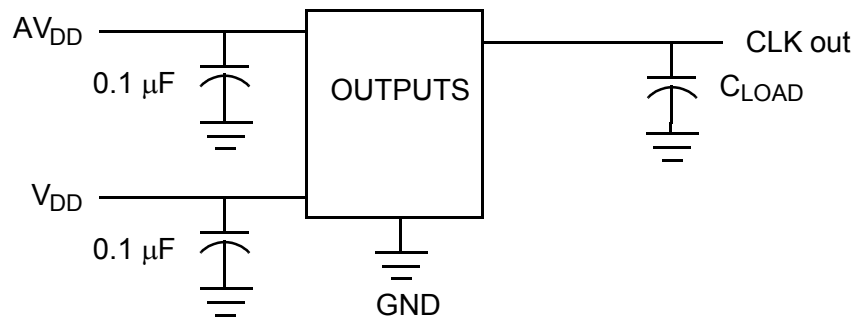
1. Not 100% tested.

**Pullable Crystal Specifications** (continued)

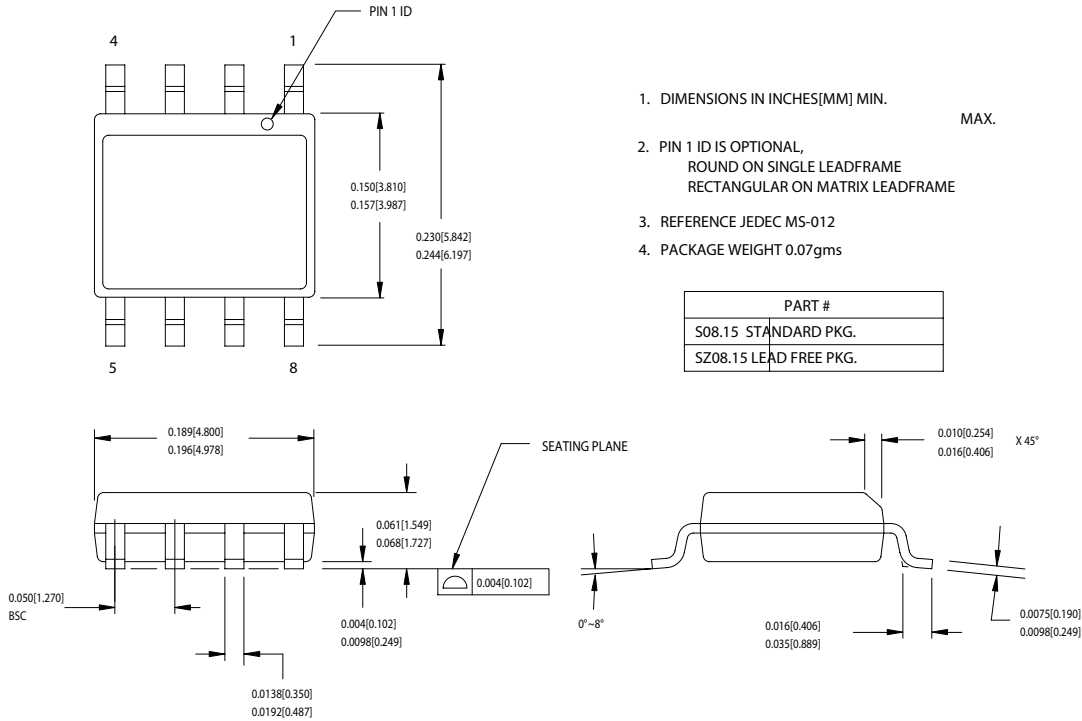
Parameter	Description	Condition	Min.	Typ.	Max.	Unit
$R_3/R_1$	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical $R_1$ values are much less than the maximum spec.	3			
DL	Crystal drive level	No external series resistor assumed		0.5	2.0	mW
$F_{3SEPHI}$	Third overtone separation from $3.F_{NOM}$	High side	300			ppm
$F_{3SEPLO}$	Third overtone separation from $3.F_{NOM}$	Low side			-150	ppm
$C_0$	Crystal shunt capacitance				7	pF
$C_0/C_1$	Ratio of shunt to motional capacitance		180		250	
$C_1$	Crystal motional capacitance		14.4	18	21.6	pF

**AC Electrical Characteristics** ( $V_{DD} = 3.3V$ )

Parameter <sup>[1]</sup>	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in <i>Figure 1</i> , 50% of $V_{DD}$	45	50	55	%
$t_3$	Rising Edge Slew Rate	Output Clock Rise Time, 20% – 80% of $V_{DD}$	0.8	1.4		V/ns
$t_4$	Falling Edge Slew Rate	Output Clock Fall Time, 80% – 20% of $V_{DD}$	0.8	1.4		V/ns
$t_9$	Clock Jitter	Peak-to-Peak Period Jitter			100	ps


**Figure 1. Duty Cycle Definition; DC =  $t_2/t_1$** 

**Figure 2. Rise and Fall Time Definitions**

**Test Circuit**
**Ordering Information**

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY24119SC	S8	8-pin SOIC	Commercial	3.3V
CY24119SCT	S8	8-pin SOIC – Tape and Reel	Commercial	3.3V
CY24119SC-1	S8	8-pin SOIC	Commercial	3.3V
CY24119SC-1T	S8	8-pin SOIC – Tape and Reel	Commercial	3.3V

**Package Diagram**
**8-lead (150-Mil) SOIC S8**


51-85066-°C

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**Document History Page**

<b>Document Title: CY24119 MediaClock™ 27-MHz VCXO Clock Generator</b>				
<b>Document Number: 38-07200</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	111551	03/22/02	CKN	New Data Sheet
*A	121877	12/14/02	RBI	Power-up requirements added to Operating Conditions Information
*B	129724	10/09/03	IJA	Added -1 part, updated Crystal Spec Table