

3.3V SDRAM Buffer for Mobile PCs with Four SO-DIMMs

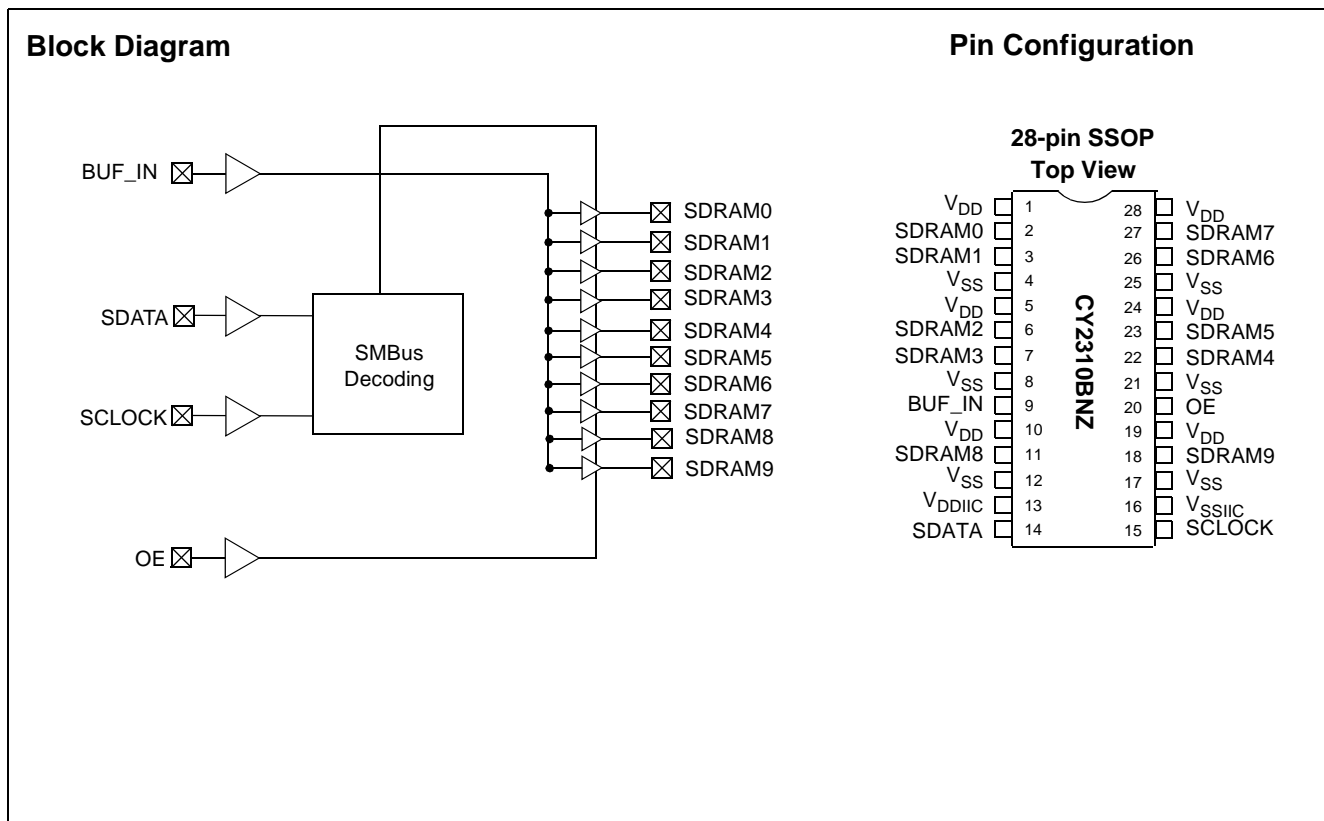
Features

- One input to 10 output buffer/driver
- Supports up to four SDRAM SO-DIMMs
- Two additional outputs for feedback
- SMBus interface for output control
- Low skew outputs
- Up to 100 MHz operation
- Multiple V_{DD} and V_{SS} pins for noise reduction
- Dedicated OE pin for testing
- Space-saving 28-pin SSOP package
- 3.3V operation

Description

The CY2310BNZ is a 3.3V buffer designed to distribute high-speed clocks in mobile PC applications. The part has ten outputs, eight of which can be used to drive up to four SDRAM SO-DIMMs, and the remaining can be used for external feedback to a PLL. The device operates at 3.3V and outputs can run up to 100 MHz, thus making it compatible with Pentium II[®] processors. The CY2310BNZ can be used in conjunction with the CY2281 or similar clock synthesizer for a full Pentium II motherboard solution.

The CY2310BNZ also includes an SMBus interface that can enable or disable each output clock. On power-up, all output clocks are enabled. A separate Output Enable pin facilitates testing on ATE.



Pin Description

Pins	Name	Description
1, 5, 10, 19, 24, 28	V _{DD}	3.3V Digital voltage supply
4, 8, 12, 17, 21, 25	V _{SS}	Ground
13	V _{DDIIC}	SMBus Voltage supply
16	V _{SSIIC}	Ground for SMBus
9	BUF_IN	Input clock
20	OE	Output Enable, three-states outputs when LOW. Internal pull-up to V _{DD}
14	SDATA	SMBus data input, internal pull-up to V _{DD}
15	SCLK	SMBus clock input, internal pull-up to V _{DD}
2, 3, 6, 7	SDRAM [0–3]	SDRAM byte 0 clock outputs
22, 23, 26, 27	SDRAM [4–7]	SDRAM byte 1 clock outputs
11, 18	SDRAM [8–9]	SDRAM byte 2 clock outputs

Device Functionality

OE	SDRAM [0–17]
0	High-Z
1	1 x BUF_IN

Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:
 - Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0
 - Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0
 - ...
 - Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0
- Reserved and unused bits should be programmed to "0."
- SMBus Address for the CY2310BNZ is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	----

**Byte 0:SDRAM Active/Inactive Register
(1 = Enable, 0 = Disable), Default = Enabled**

Bit	Pin #	Description
Bit 7	–	Initialize to 0
Bit 6	–	Initialize to 0
Bit 5	–	Initialize to 0
Bit 4	–	Initialize to 0
Bit 3	7	SDRAM3 (Active/Inactive)
Bit 2	6	SDRAM2 (Active/Inactive)
Bit 1	3	SDRAM1 (Active/Inactive)
Bit 0	2	SDRAM0 (Active/Inactive)

**Byte 1: SDRAM Active/Inactive Register
(1 = Active, 0 = Inactive), Default = Active**

Bit	Pin #	Description
Bit 7	27	SDRAM7 (Active/Inactive)
Bit 6	26	SDRAM6 (Active/Inactive)
Bit 5	23	SDRAM5 (Active/Inactive)
Bit 4	22	SDRAM4 (Active/Inactive)
Bit 3	–	Initialize to 0
Bit 2	–	Initialize to 0
Bit 1	–	Initialize to 0
Bit 0	–	Initialize to 0

**Byte 2: SDRAM Active/Inactive Register
(1 = Active, 0 = Inactive), Default = Active**

Bit	Pin #	Description
Bit 7	18	SDRAM9 (Active/Inactive)
Bit 6	11	SDRAM8 (Active/Inactive)
Bit 5	–	Reserved, drive to 0
Bit 4	–	Reserved, drive to 0
Bit 3	–	Reserved, drive to 0
Bit 2	–	Reserved, drive to 0
Bit 1	–	Reserved, drive to 0
Bit 0	–	Reserved, drive to 0

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V _{DD}	Core Supply Voltage		-0.5	7.0	V
V _{IN}	Input Voltage	Relative to V _{SS}	-0.5	V _{DD} +0.5	VDC
T _S	Temperature, Storage	Non Functional	-65	+150	°C
T _A	Temperature, Operating Ambient	Functional	-40	85	°C
T _J	Temperature, Junction	Functional		150	°C
∅ _{JC}	Dissipation, Junction to Case	Mil-Spec 883E Method 1012.1	32.24		°C/W
∅ _{JA}	Dissipation, Junction to Ambient	JEDEC (JESD 51)	98.31		°C/W
ESD _{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000		Volts
UL-94	Flammability Rating	@1/8 in.	V-0		
MSL	Moisture Sensitivity Level		1		ppm

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
V _{DD}	Supply Voltage	@3.3V±5%	3.135	3.465	V
I _{DD1}	3.3V Supply Current	at 64MHz	100	180	mA
I _{DD2}	3.3V Supply Current	at 100 MHz	150	220	mA
I _{DD Tristate}	3.3V Supply Current in Three-State		-	10	mA
Logic Inputs					
V _{IL}	Input Low Voltage		V _{SS} -0.3	0.8	V
V _{IH}	Input High Voltage		2.0	V _{DD} +0.5	V
I _{IL1}	Input Leakage Current, BUF_IN		-5	+5	µA
I _{IL2}	Input Leakage Current ^[1]		-20	+5	µA
Logic Outputs (SDRAM0:9)^[2]					
V _{OL}	Output Low Voltage	I _{OL} = 1 mA	-	50	mV
V _{OH}	Output High Voltage	I _{OH} = -1 mA	3.1	-	V
I _{OL}	Output Low Current	V _{OL} = 1.5V	70	185	mA
I _{OH}	Output High Current	V _{OH} = 1.5V	65	160	mA
Pin Capacitance/Inductance					
C _{IN}	Input Pin Capacitance		-	5	pF
C _{OUT}	Output Pin Capacitance		-	6	pF
L _{IN}	Input Pin Inductance		-	7	nH
C _{LOAD}	Input Load Capacitance		20	30	pF

AC Electrical Specifications

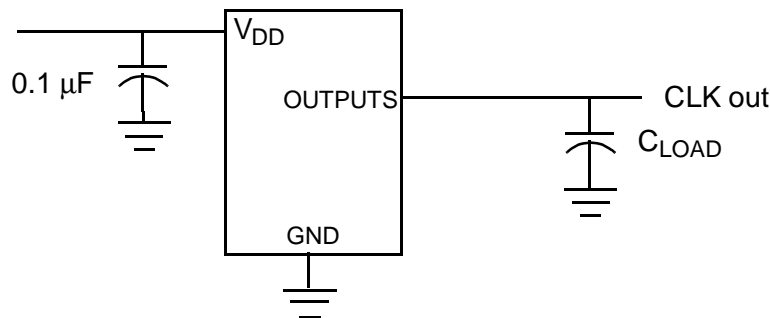
Parameter	Description	Test Condition	Min.	Max.	Unit
F _{IN}	Input Frequency	at 64 MHz	0	133	MHz
T _R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1.5	4.0	V/ns
T _F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1.5	4.0	V/ns
T _{SR}	Output Skew, Rising Edges			200	ps
T _{SF}	Output Skew, Falling Edges			200	ps
T _{EN}	Output Enable Time		1.0	8.0	ns
T _{DIS}	Output Disable Time		1.0	8.0	ns

Notes:

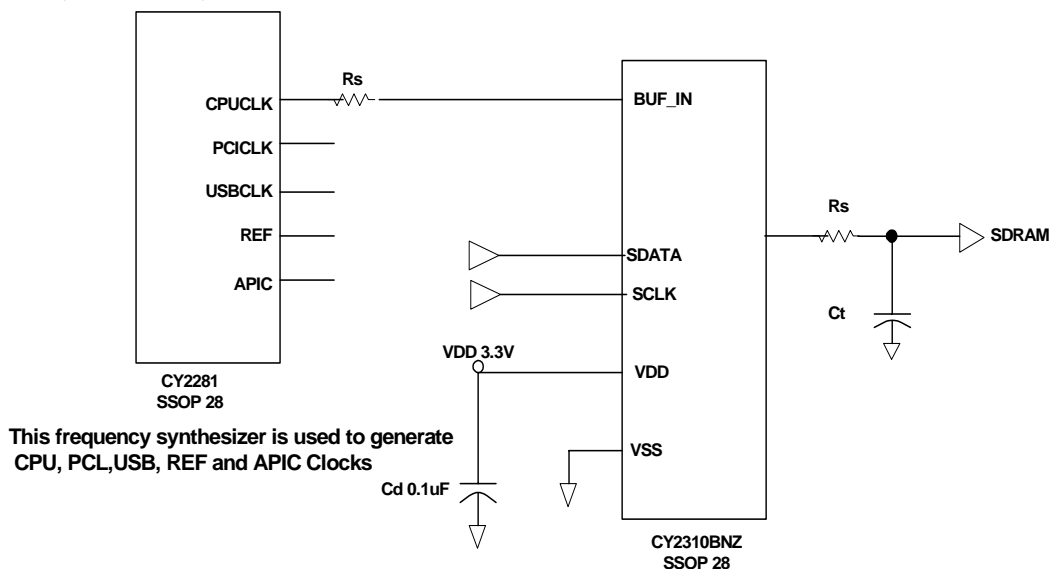
1. OE, SDATA, and SCLOCK logic pins have a 250-kΩ internal pull-up resistor (V_{DD} - 0.8V).
2. All SDRAM outputs loaded by 6" transmission lines with 22-pF capacitors on ends.

AC Electrical Specifications (continued)

Parameter	Description	Test Condition	Min.	Max.	Unit
t_{PR}	Rising Edge Propagation Delay		3.0	5.0	ns
T_{PF}	Falling Edge Propagation Delay		3.0	5.0	ns
T_{DC}	Duty Cycle	Measured at 1.5V	50	60	%
Z_o	AC Output Impedance				Ω

Test Circuit

Figure 1. Test Circuit
Application Information

Clock traces must be terminated with either series or parallel termination, as they are normally done.



This frequency synthesizer is used to generate CPU, PCL, USB, REF and APIC Clocks

C_d = Decoupling Capacitor
 C_t = Optional EMI-Reducing Capacitor
 R_s = Series Terminating Resistors

Summary

- Surface mount, low-ESR ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 μ F. In some cases, smaller value capacitors may be required.
- The value of the series-terminating resistor satisfies the following equation where R_{trace} is the loaded characteristic impedance of the trace, R_{out} is the output impedance of the

buffer (typically 25W), and R_{series} is the series terminating resistor.

$$R_{series} > R_{trace} - R_{out}$$

- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board V_{DD} from the clock generator V_{DD} island. Ensure that the Ferrite Bead

offers greater than 50W impedance at the clock frequency, under loaded DC conditions. Please refer to the application note "Layout and Termination Techniques for Cypress Clock Generators" for more details.

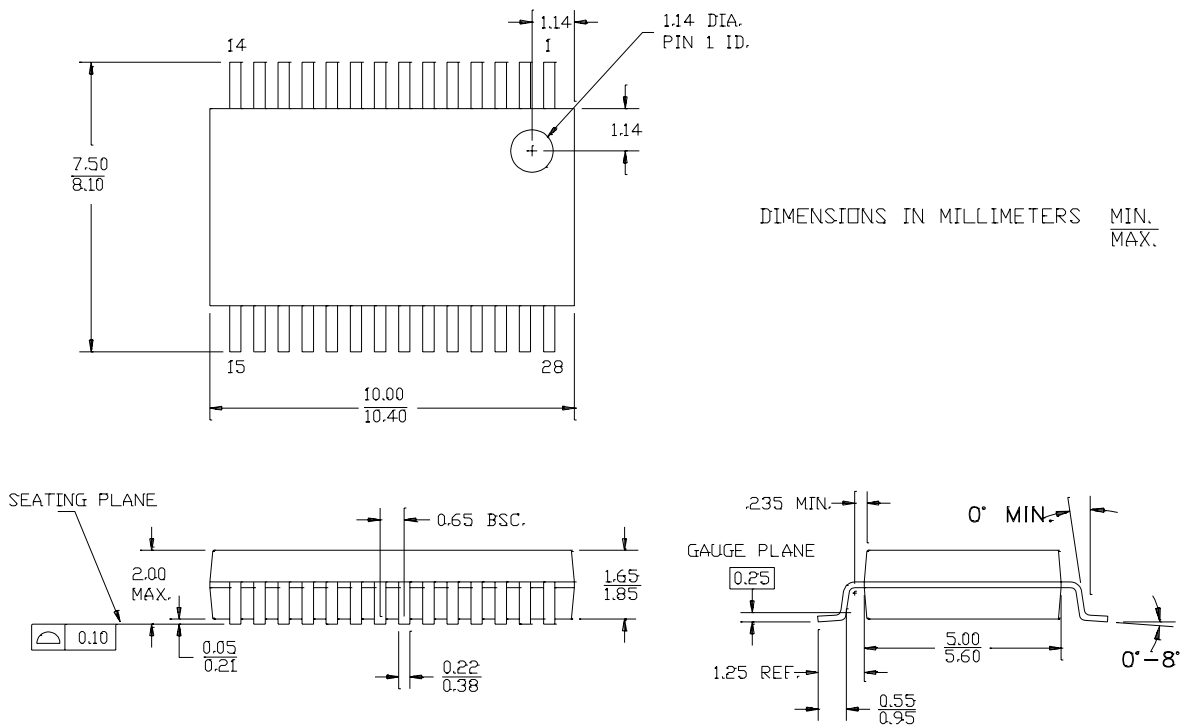
- If a Ferrite Bead is used, a 10 μF –22 μF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

Ordering Information

Ordering Code	Package Type	Operating Range
CY2310BNZPVC-1	28-pin SSOP	Commercial, 0 °C to 70°C
CY2310BNZPVC-1T	28-pin SSOP – Tape and Reel	Commercial, 0 °C to 70°C
CY2310BNZPVI-1	28-pin SSOP	Industrial, -40 °C to 85°C
CY2310BNZPVI-1T	28-pin SSOP – Tape and Reel	Industrial, -40 °C to 85°C

Package Drawing and Dimension

28-lead (5.3 mm) Shrunken Small Outline Package O28



51-85079-°C

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Document History Page

Document Title: CY2310BNZ 3.3V 3.3V SDRAM Buffer for Mobile PCs with Four SO-DIMMs				
Document Number: 38-07260				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	110525	02/07/02	SZV	Change from Spec number: 38-01089 to 38-07260
*A	121577	01/29/03	RGL	Corrected the ordering information to match the devmaster. Changed the max value of the VDD Core Supply in the Absolute Maximum Conditions table from 4.6V to 7.0V