REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R075-95. – LTG	95-03-30	Monica L. Poelking
B	Change AC limits in table I. Correct pin names in figure 2, figure 3, figure 4, and table III. Update boilerplate. Editorial changes throughout. – TVN	01-02-23	Thomas M. Hess

REV	B	B																		
SHEET	55	56																		
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS																	
	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

PREPARED BY
Thomas M. Hess

CHECKED BY
Thomas M. Hess

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
93-01-22

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, CMOS, VMEBUS INTERFACE CONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-92010**

SHEET 1 OF 56

DSCC FORM 2233
APR 97

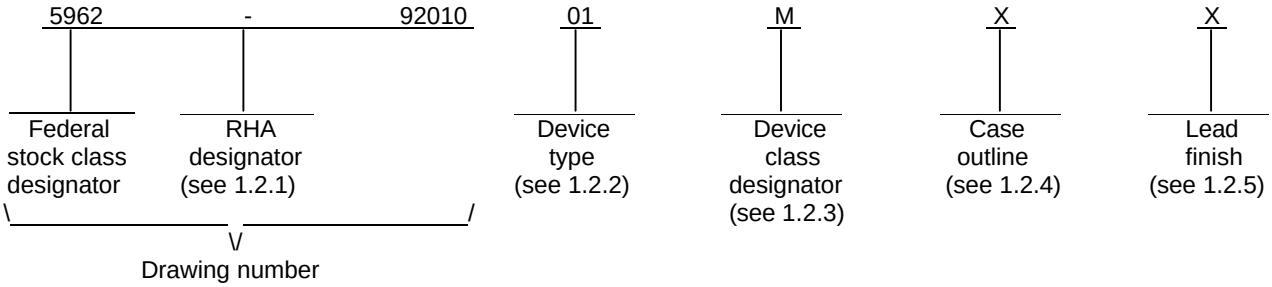
5962-E259-01

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	VIC068A	VMEbus interface controller

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA7-P145	145	Pin grid array
Y	See figure 1	160	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Voltage on any pin with respect to ground ..... -0.5 V dc to +7.0 V dc
Power dissipation (P_D)..... 1.5 W
Storage temperature range (T_{STG})..... -65°C to +150°C
Lead temperature (soldering, 10 seconds)..... +260°C
Thermal resistance, junction-to-case (Θ_{JC}):
Case outline X..... See MIL-STD-1835
Case outline Y..... 10°C/W
Junction temperature (T_J)..... 175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})..... 5.0 V dc ±10%
Case operating temperature range (T_C) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Timing waveforms. The timimg waveforms shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Input low voltage	V_{IL}		1, 2, 3	All		0.8	V
Input high voltage	V_{IH}		1, 2, 3	All	2.0		
Output low voltage	V_{OL}	V_{CC} = MIN, I_{OL} = 8 mA 2/	1, 2, 3	All		0.6	V
		V_{CC} = MIN, I_{OL} = 48 mA 3/				0.6	
Output high voltage	V_{OH}	V_{CC} = MIN, I_{OH} = -3 mA 3/	1, 2, 3	All	2.4		V
		V_{CC} = MIN, I_{OH} = -8 mA 2/			2.4		
Input leakage current	I_{IL}	V_{CC} = MAX $0.0\ V \le V_{IN} \le V_{CC}$	1, 2, 3	All	-10	+10	µA
Output leakage current (All output pins disabled)	I_{LO}	V_{CC} = MAX, VMEbus pins $0.6\ V \le V_{OUT} \le 2.4\ V$	1, 2, 3	All	-10	+10	µA
		V_{CC} = MAX, other pins $0.0\ V \le V_{OUT} \le V_{CC}$			-10	+10	
Input clamp voltage	V_{IK}	V_{CC} = MIN, I_{IN} = -18 mA	1, 2, 3	All		-1.2	V
		I_{IN} = 18 mA			V_{CC} +1.2		
Power supply current	I_{CC}	V_{CC} = 5.5 V V_{IN} = 0.0 V, 5.5 V	1, 2, 3	All		150	mA
Input capacitance 4/	C_{IN}	V_{CC} = 5.0 V T_C = 25°C, f = 1 MHz See 4.4.1c	4	All		10	pF
Output capacitance 4/	C_{OUT}					15	
Functional testing		See 4.4.1b	7, 8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
BRi[0] to BBSY[H] 5/	t_{A1}	Arbitration signals	9, 10, 11	All	2.5T+4	3T+31.5	ns
BRi[0] to BBSY[L] 6/	t_{A2}		9, 10, 11	All	3T+7	3.5T+35	ns
BRi[0] to BGiOUT[L] 6/	t_{A3}		9, 10, 11	All	3T+3	4T+28	ns
BRi[0] to BCLR[L]	t_{A4}		9, 10, 11	All	2	19	ns
BGiIN[0] TO BGiOUT[L]	t_{A5}		9, 10, 11	All	2	20	ns
BGiIN[0] to BBSY[L] 7/	t_{A6}		9, 10, 11	All	3	25	ns
BGiIN[0] to BRi[H] 7/	t_{A7}		9, 10, 11	All	4	3T+31	ns
BGiIN[1] to BGiOUT[H]	t_{A8}		9, 10, 11	All	2	23	ns
BBSY[0] to BGiOUT[H] 6/	t_{A9}		9, 10, 11	All	3	24	ns
BBSY[1] to BGiOUT[L]	t_{A10}		9, 10, 11	All	3T+3	4T+29	ns
BBSY[1] to BCLR[H]	t_{A11}		9, 10, 11	All	1T+3	2T+27	ns
BGiIN[0] to DENO[L] 7/ 8/	t_{B1}	Master access signals	9, 10, 11	All	6	3T+42	ns
BGiIN[0] to LADO[H] 7/	t_{B2}		9, 10, 11	All	12	3T+67	ns
BGiIN[0] to AS[L] 7/	t_{B3}		9, 10, 11	All	3T+4	6T+31	ns
BGiIN[0] to A[7:1] valid 7/	t_{B4}		9, 10, 11	All	5	3T+37	ns
BGiIN[0] to LWORD[H/L] 7/	t_{B5}		9, 10, 11	All	5	3T+37	ns
BGiIN[0] to WRITE[H/L] 7/	t_{B6}		9, 10, 11	All	5	3T+37	ns
BGiIN[0] to ABEN[L] 7/	t_{B7}		9, 10, 11	All	6	3T+38	ns
PAS[0] & MWB[0] to BRi[L]	t_{B8}		9, 10, 11	All	3	24	ns
PAS[0] & MWB[0] to ISOBE[L]	t_{B9}		9, 10, 11	All	3	25	ns
PAS[0] & MWB[0] to LADO[H]	t_{B10}		9, 10, 11	All	12	68	ns
PAS[0] & MWB[0] to BBSY[L] 9/	t_{B11}		9, 10, 11	All	5	36	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
PAS[0] & MWB[0] to ABEN[L] 9/	t_{B12}	Master access signals	9, 10, 11	All	1.5T+6	2.5T+41	ns
PAS[0] & MWB[0] to A(7:1) 9/	t_{B13}		9, 10, 11	All	1.5T+5	2.5T+41	ns
PAS[0] & MWB[0] to LWORD[H/L] 9/	t_{B14}		9, 10, 11	All	1.5T+5	2.5T+41	ns
PAS[0] & MWB[0] to WRITE[H/L] 9/	t_{B15}		9, 10, 11	All	1.5T+5	2.5T+41	ns
PAS[0] & MWB[0] & DS[0] to DS1/0[L] 9/	t_{B16}		9, 10, 11	All	4.5T+9	5.5T+57	ns
PAS[0] & MWB[0] to SWDEN[L]	t_{B17}		9, 10, 11	All	3	14	ns
PAS[0] & MWB[0] to LWDENIN[L] 10/	t_{B18}		9, 10, 11	All	2	22	ns
PAS[0] & MWB[0] to UWDENIN[L] 10/	t_{B19}		9, 10, 11	All	3	23	ns
PAS[0] & MWB[0] & DS[0] to AS[L] 9/	t_{B20}		9, 10, 11	All	4.5T+5	5.5T+32	ns
R/W[0]to DDIR[H] 8/	t_{B21}		9, 10, 11	All	2	25	ns
R/W[1] to DDIR[L] 8/	t_{B22}		9, 10, 11	All	1	15	ns
D(7:0) to LD(7:0) valid 10/	t_{B23}		9, 10, 11	All	2	22	ns
DTACK[0] to LEDI[H] 10/	t_{B24}		9, 10, 11	All	3T+4	4T+32	ns
DTACK[0] to DSACKi[L]	t_{B25}		9, 10, 11	All	3	36	ns
PAS[1] & DS[1] to DSACKi[H]	t_{B26}		9, 10, 11	All	2	27	ns
PAS[1] to AS[H]	t_{B27}		9, 10, 11	All	5	41	ns
DS[1] to ISOBE[H]	t_{B28}		9, 10, 11	All	3	26	ns
DS[1] to SWDEN[H]	t_{B29}		9, 10, 11	All	2	13	ns
DS[1] to UWDENIN[H] 10/	t_{B30}		9, 10, 11	All	2	22	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
DS[1] to LWDENIN[H] 10/	t_{B31}	Master access signals	9, 10, 11	All	2	22	ns
DS[1] to LD(7:0) invalid 10/	t_{B32}		9, 10, 11	All	2	28	ns
DS[1] to LD(7:0) Hi-Z 10/	t_{B33}		9, 10, 11	All	2	28	ns
DS[0] to DSACKi[L] 11/	t_{B34}		9, 10, 11	All	5	T+35	ns
DS[0] to LADO[H] 11/	t_{B35}		9, 10, 11	All	7	43	ns
DS[0] to LEDO[H] 11/	t_{B36}		9, 10, 11	All	3	T+20	ns
LBG[0] to PAS[L]	t_{C1}	Local bus timing signals	9, 10, 11	All	5T+5	6T+44	ns
LBG[0] to LA(7:0) valid	t_{C2}		9, 10, 11	All	3T+6	4T+46	ns
LBG[0] to SIZ(1:0) valid	t_{C3}		9, 10, 11	All	1T+2	2T+28	ns
LBG[0] to FC(2:1) valid	t_{C4}		9, 10, 11	All	1T+2	2T+27	ns
LBG[0] to LD(7:0) driven 8/	t_{C5}		9, 10, 11	All	3T+7	4T+48	ns
LBG[0] to LAEN[H]	t_{C6}		9, 10, 11	All	3T+8	4T+48	ns
LBG[0] to ISOBE[L]	t_{C7}		9, 10, 11	All	3T+7	4T+42	ns
LBG[0] to SWDEN[L]	t_{C8}		9, 10, 11	All	3T+7	4T+45	ns
LBG[0] to DDIR[H] 8/	t_{C9}		9, 10, 11	All	3T+7	4T+42	ns
LBG[0] to UWDENIN[L] 8/	t_{C10}		9, 10, 11	All	3T+6	4T+42	ns
LBG[0] to LWDENIN[L] 8/	t_{C11}		9, 10, 11	All	3T+5	4T+38	ns
LBG[0] & DS1/0[0] & WRITE[0] to R/W[L] 8/	t_{C12}		9, 10, 11	All	3T+7	4T+47	ns
LBG[0] & DS1/0[0] to DS[L]	t_{C13}		9, 10, 11	All	5T+7	6T+56	ns
PAS[0] to DS[L] 12/	t_{C14}		9, 10, 11	All	0	15	ns
LBR[H] to LBG[1] 4/	t_{C15}		9, 10, 11	All		T	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
SLSELi[0] & AS[0] to LBR[L]	t_{D1}	Slave access signals	9, 10, 11	All	6	40	ns
SLSELi[0] & AS[0] & DS1/0 to LADI[H]	t_{D2}		9, 10, 11	All	4	29	ns
LD(7:0) to D(7:0) 10/	t_{D3}		9, 10, 11	All	2	18	ns
DSACKI[0] to LEDO[H] 10/	t_{D4}		9, 10, 11	All	SAT+6	SAT+39 + 0.5T	ns
DSACKI[0] to DTACK[L]	t_{D5}		9, 10, 11	All	SAT+9	SAT+53 + 0.5T	ns
DS1/0[0] to DTACK[L]	t_{D6}	Slave access signals Slave write post only	9,10,11	All	2T+4	3.5T+33	ns
DS1/0[0] to LEDI[H]	t_{D7}		9, 10, 11	All	8	47	ns
AS[1] to LA(7:0), R/W invalid	t_{D8}	Slave access signals	9, 10, 11	All	4	55	ns
AS[1] to LA(7:0), R/W Hi-Z	t_{D9}		9, 10, 11	All	4	55	ns
AS[1] to FC2/1 invalid	t_{D10}		9, 10, 11	All	8	56	ns
AS[1] & DSACKi[1] to FC2/1 Hi-Z	t_{D11}		9, 10, 11	All	8	56	ns
AS[1] to SIZ1/0 invalid	t_{D12}		9, 10, 11	All	6	37	ns
As[1] & DSACKi[1] to SIZ1/0, Hi-Z	t_{D13}		9, 10, 11	All	2	1T+24	ns
AS[1] to ISOBE[H]	t_{D14}		9, 10, 11	All	5	34	ns
AS[1] to SWDEN[H]	t_{D15}		9, 10, 11	All	3	27	ns
AS[1] to UWDENIN[H] 8/	t_{D16}		9, 10, 11	All	4	30	ns
AS[1] to LWDENIN[H] 8/	t_{D17}		9, 10, 11	All	4	30	ns
AS[1] & DSACKi[1] to LBR[H]	t_{D18}		9, 10, 11	All	4	30	ns
AS[1] to LAEN[L]	t_{D19}		9, 10, 11	All	7	56	ns
DS1/0[1] to LD(7:0) invalid 8/	t_{D20}		9, 10, 11	All	2	39	ns
DS1/0[1] to LD(7:0) Hi-Z 8/	t_{D21}		9, 10, 11	All	2	39	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
DSACKi[0] to PAS[H]	t_{D22}	Slave access signals	9, 10, 11	All	SAT+8	SAT+56 + 0.5T	ns
DSACKi[0] to DS[H]	t_{D23}		9, 10, 11	All	SAT+7	SAT+48 + 0.5T	ns
DSACKi[1] to DTACK[H]	t_{D24}		9, 10, 11	All	3	35	ns
IACKIN[0] to IACKOUT[L]	t_{E1}	Interrupt signals	9, 10, 11	All	2	18	ns
IACKIN[1] to IACKOUT[H]	t_{E2}		9, 10, 11	All	2	20	ns
FCIACK[0] & PAS[0] to BRi[L]	t_{E3}		9, 10, 11	All	5T+7	6T+48	ns
FCIACK[0] & PAS[0] to IACK[L] 9/	t_{E4}		9, 10, 11	All	7.5T+6	8.5T+39	ns
FCIACK[0] & PAS[0] to LD(7:0) driven 13/	t_{E5}		9, 10, 11	All	5T+10	6T+57	ns
FCIACK[0] & PAS[0] to LD(7:0) valid 14/	t_{E6}		9, 10, 11	All	9T+4	10T+37	ns
FCIACK[0] & PAS[0] to LIACKO[L] 15/	t_{E7}		9, 10, 11	All	5T+5	6T+36	ns
IRQi[0] to IPL	t_{E8}		9, 10, 11	All	4	37	ns
BGiIN[0] to BBSY[L]	t_{E9}		9, 10, 11	All	5	36	ns
BGiiN[0] to AS[L]	t_{E10}		9, 10, 11	All	3T+4	4T+31	ns
BGiIN[0] to DS1/0[L]	t_{E11}		9, 10, 11	All	3T+8	4T+55	ns
BGiIN[0] to IACK[L] 14/	t_{E12}		9, 10, 11	All	44		ns
PAS[0] to ISOBE[L]	t_{E13}		9, 10, 11	All	5T+7	6T+44	ns
PAS[0] to SWDEN[L]	t_{E14}		9, 10, 11	All	5T+6	6T+42	ns
IPLi to IPLi 4/ 12/	t_{E15}		9, 10, 11	All		12	ns
MWB[0] & PAS[0] & DS[0] to BRi[L]	t_{F1}	Master block transfer with local DMA signals (initiation cycle)	9, 10, 11	All	T+5	2T+38	ns
BGiIN[0] to LBR[L]	t_{F2}		9, 10, 11	All	4T+8	5T+50	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
MWB[0] & PAS[0] & DS[0] to LBR[L] 9/	t_{F3}	Master block transfer with local DMA signals (initiation cycle)	9, 10, 11	All	5T+8	6T+50	ns
MWB[0] & PAS[0] & DS[0] to LADO[H]	t_{F4}		9, 10, 11	All	T+6	2T+39	ns
MWB[0] & PAS[0] & DS[0] to BLT[L]	t_{F5}		9, 10, 11	All	T+4	2T+37	ns
DSACKi[0] & DS[0] to DS[H]	t_{G1}	Master block transfer with local DMA signals (write cycle)	9, 10, 11	All	MBAT0+7	MBAT0+ 0.5T+52	ns
DSACKi[0] & DS[L] to LEDO[H]	t_{G2}		9, 10, 11	All	MBAT0+6	MBAT0+ 0.5T+40	ns
DSACKi[0] & DS[L] to LA(7:0) valid	t_{G3}		9, 10, 11	All	MBAT0+T+ 9	MBAT0+ 1.5T+40	ns
DSACKi[0] & DS[L] to DSi[L]	t_{G4}		9, 10, 11	All	MBAT0+3T +5	MBAT0+ 3.5T+42	ns
DTACK[0] to LEDO[L]	t_{G5}		9, 10, 11	All	6	38	ns
DTACK[0] to DSi[H]	t_{G6}		9, 10, 11	All	9	56	ns
DTACK[0] to A(7:0) valid	t_{G7}		9, 10, 11	All	9	64	ns
DS[H] to DS[L] 4/	t_{G8}		9, 10, 11	All	DST+ 1.5T-15	DST+ 1.5T-4	ns
DSACKi[0] & DS[L] to DS[H]	t_{G9}		9, 10, 11	All	MBAT1+7	MBAT1+ 0.5T+52	ns
DSACKi[0] & DS[L] to LEDO[H]	t_{G10}		9, 10, 11	All	MBAT1+6	MBAT1+ 0.5T+40	ns
DSACKi[0] & DS[L] to LA(7:0) valid	t_{G11}		9, 10, 11	All	MBAT1+T+ 9	MBAT1+ 1.5T+40	ns
DSACKi[0] & DS[L] to DSi[L]	t_{G12}		9, 10, 11	All	MBAT1+3T +5	MBAT1+ 3.5T+38	ns
DTACK[0] to LEDO[L]	t_{G13}		9, 10, 11	All	6	38	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
DTACK[0] to DSi[H]	t_{G14}	Master block transfer with local DMA signals (write cycle)	9, 10, 11	All	9	59	ns
DTACK[0] to A(7:0) valid	t_{G15}		9, 10, 11	All	9	64	ns
DTACK[0] to DS[H] (Slow Slave) 4/	t_{G16}		9, 10, 11	All	T+13	1.5T+47	ns
LEDO[L] to LEDO[H] (Slow Slave) 4/	t_{G17}		9, 10, 11	All	T+9	1.5T+27	ns
DTACK[0] to LEDi[H]	t_{H1}	Master block transfer with local DMA signals (read cycle)	9, 10, 11	All	2.0T+4	3T+27	ns
DTACK[0] to DSi[H]	t_{H2}		9, 10, 11	All	2.0T+7	3T+32	ns
DTACK[0] to A(7:0) valid	t_{H3}		9, 10, 11	All	1.5T+8	2.5T+53	ns
DTACK[0] to DS[L]	t_{H4}		9, 10, 11	All	1.5T+7	2.5T+47	ns
DSACKi[0] & DS[L] to DS[H]	t_{H5}		9, 10, 11	All	MBAT0+7	MBAT0+ 0.5T+45	ns
DSACKi[0] & DS[L] to LEDI[L]	t_{H6}		9, 10, 11	All	MBAT0+7	MBAT0+ 0.5T+55	ns
DSACKi[0] & DS[0] to LA(7:0) valid	t_{H7}		9, 10, 11	All	MBAT0+T+ 9	MBAT0+ 1.5T+35	ns
DSACKi[0] & DS[0] to DSi[L]	t_{H8}		9, 10, 11	All	MBAT0+ 10	MBAT0+ 0.5T+83	ns
DTACK[0] to LEDI[H]	t_{H9}		9, 10, 11	All	2T+4	3T+27	ns
DTACK[0] to DSi[H]	t_{H10}		9, 10, 11	All	2T+7	3T+32	ns
DTACK[0] to A(7:0) valid	t_{H11}		9, 10, 11	All	8	53	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
DTACK[0] to DS[L]	t_{H12}	Master block transfer with local DMA signals (read cycle)	9,10,11	All	7	47	ns
DSACKi[0] & DS[0] to DS[H]	t_{H13}		9, 10, 11	All	MBAT1+7	MBAT1+ 0.5T+45	ns
DSACKi[0] & DS[0] to LEDI[L]	t_{H14}		9, 10, 11	All	MBAT1+7	MBAT1+ 0.5T+55	ns
DSACKi[0] & DS[0] to LA(7:0) valid	t_{H15}		9, 10, 11	All	MBAT1+T+ 9	MBAT1+ 1.5T+35	ns
DSACKi[0] & DS[0] to DSi[L]	t_{H16}		9, 10, 11	All	MBAT1+ 10	MBAT1+ 0.5T+83	ns
DS[L] to BLT[H]	t_{J1}	Master block transfer with local DMA signals (boundary cycle)	9, 10, 11	All	2	35	ns
DS[L] to BLT[L]	t_{J2}		9, 10, 11	All	2	21	ns
DSi[L] to LEDO[H/L]	t_{J3}		9, 10, 11	All	2	25	ns
DSi[L] to LADO[L/H]	t_{J4}		9, 10, 11	All	2	20	ns
DSi[0] to LEDI[H]	t_{K1}	Slave block transfer signals (write cycle)	9, 10, 11	All	4	24	ns
DSi[0] to DS[L]	t_{K2}		9, 10, 11	All	5	39	ns
DSACKi[0] & DS[L] to DTACK[H]	t_{K3}		9, 10, 11	All	SBAT+7	SBAT+ 0.5T+52	ns
DSACKi[0] & DS[L] to DTACK[L]	t_{K4}		9, 10, 11	All	SBAT+10	SBAT+ 0.5T+67	ns
DSACKi[0] & DS[L] to ISOBE[H]	t_{K5}		9, 10, 11	All	SBAT+11	SBAT+ 0.5T+62	ns
DSACKi[0] & DS[L] to SWDEN[H]	t_{K6}		9, 10, 11	All	SBAT+10	SBAT+ 0.5T+61	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
DSACKi[0] & DS[L] to LA(7:0) valid	t_{K7}	Slave block transfer signals (write cycle)	9, 10, 11	All	SBAT+T+8	SBAT+ 1.5T+40	ns
DSACKi[0] & DS[L] to LEDI[L]	t_{K8}		9, 10, 11	All	SBAT+6	SBAT+ 0.5T+53	ns
DS1/0[1] to DTACK[H]	t_{K9}		9, 10, 11	All	4	35	ns
DS1/0[1] to LEDO[L] 4/	t_{L1}	Slave block transfer signals (read cycle)	9, 10, 11	All	3	30	ns
DS[H] to DS[L] 4/	t_{L2}		9, 10, 11	All	DST+ 1.5T-15	DST+ 1.5T-4	ns
DS1/0[0] to DENO[L]	t_{L3}		9, 10, 11	All	3	24	ns
DSACKi[0] & DS[0] to LEDO[H]	t_{L4}		9, 10, 11	All	SBAT+6	SBAT+ 0.5T+41	ns
DSACKi[0] & DS[0] to DS[H]	t_{L5}		9, 10, 11	All	SBAT+7	SBAT+ 0.5T+52	ns
DSACKi[0] & DS[0] to DTACK[L]	t_{L6}		9, 10, 11	All	SBAT+9	SBAT+ 0.5T+53	ns
DSACKi[0] & DS[0] to LA(7:0) valid	t_{L7}		9, 10, 11	All	SBAT+T+8	SBAT+ 0.5T+40	ns
DS1/0[1] to DENO[H]	t_{L8}		9, 10, 11	All	2	22	ns
DS1/0[1] to DTACK[H]	t_{L9}		9, 10, 11	All	3	24	ns
LEDO[L] to LEDO[H] (Slow Master) 4/	t_{L10}		9, 10, 11	All	1.5+9	1.5+27	ns
DTACK[0] to DS[H] (Slow Master) 4/	t_{L11}		9, 10, 11	All	1.5+13	1.5+47	ns
PAS[0] & DS[0] & CS[0] to DSACKi[L]	t_{M1}	Register access signals	9, 10, 11	All	4T+4	5T+38	ns
PAS[0] & DS[0] & CS[0] to LD(7:0) valid 10/	t_{M2}		9, 10, 11	All	3T+4	4T+37	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
AS[0] & ICFSEL[0] to DTACK[L]	t_{M3}	Register access signals	9, 10, 11	All	4T+5	4T+34	ns
LBG[0] to HALT[L], RESET[L]	t_{N1}	Reset signals	9, 10, 11	All	6	48	ns
IRESET[0] to LBR[L]	t_{N2}		9, 10, 11	All	5	33	ns
IRESET[0] to IPL0[Z]	t_{N3}		9, 10, 11	All	2	20	ns
LA, ASIZ(1:0) valid to PAS[0] 4/	t_{P1}	Setup times	9, 10, 11	All	-2T		ns
SIZ(1:0), WORD, FC(2:1) valid to PAS[0] 4/	t_{P2}		9, 10, 11	All	-2T		ns
LD(7:0) valid to DS[0] 4/	t_{P3}		9, 10, 11	All	0		ns
PAS[1] to LA, ASIZ(1:0) invalid 4/	t_{Q1}	Hold times	9, 10, 11	All	0		ns
PAS[1] to SIZ(1:0), WORD, FC(2:1) invalid 4/	t_{Q2}		9, 10, 11	All	0		ns
DS[1] to LD(7:0) invalid 4/	t_{Q3}		9, 10, 11	All	0		ns
DS1/0[1] to DTACK[H] 4/	t_{Q4}		9, 10, 11	All	0		ns
Frequency of operation		Clock inputs	9, 10, 11	All	1	64	MHz
Cycle time	1		9, 10, 11	All	15.6	1000	ns
Clock pulse width (measured from 1.5 V to 1.5 V)	2, 3		9, 10, 11	All	16/	16/	ns
Rise and fall time	4, 5		9, 10, 11	All		5	ns

See footnotes on next sheet.

TABLE I. Electrical performance characteristics - Continued.

1/ All testing to be performed using worst-case test conditions. The following pins are active low: CS, PAS, DSACK0, LBG, IPL1, IPL2, BLT, DSACK1, LBERR, W, RMC, IRESET, ABEN, LIACKO, DEDLK, RESET, HALT, LBR, SCON, LIRQ2, IPL0, LIRQ5, LIRQ1, UWDENIN, LIRQ4, LIRQ3, LWDENIN, SWDEN, LIRQ6, LIRQ7, DENO, ISOBE, SLSEL1, ICFSEL, WORD, MWB, SLSEL0, FCIACK, BG0OUT, BG1OUT, IRQ1, BG2IN, BG3OUT, IRQ2, IRQ5, SYSFAIL, IACKIN, BERR, BR2, BBSY, BG0IN, BG3IN, BG2OUT, IRQ3, IRQ6, SYSRESET, IACK, AS, DS, LWORD, WRITE, DS1, BR1, BR3, BG1IN, IRQ4, IRQ7, ACFAIL, IACKOUT, DTACK, DS0, BR0, BCLR.

2/ VMEbus signals (Low Drive, all VMEbus Daisy Chain Signals) and all non-VMEbus signals.

3/ VMEbus signals (AS, DS1, DS0, BCLR, SYSCLK) and VMEbus signals (Medium Drive, all non-High, non-Low Drive Signals).

4/ Tested initially and at process and design changes. Thereafter guaranteed, if not tested, to the limits specified in table I.

5/ ROR mode.

6/ While VMEbus system controller.

7/ Synchronous delay depends on speed in which BGiIN is returned. If BGiIN is returned in zero time after request, synchronous delay will be maximum.

8/ Write operation only.

9/ While VMEbus master.

10/ Read operation only.

11/ Master write post only.

12/ Skew.

13/ VMEbus interrupt only.

14/ Local interrupt (LICR[4] = 1) only.

15/ Local interrupt (LICR[4] = 0) only.

16/ A 60/40 to 40/60 duty cycle must be maintained.

Case Y

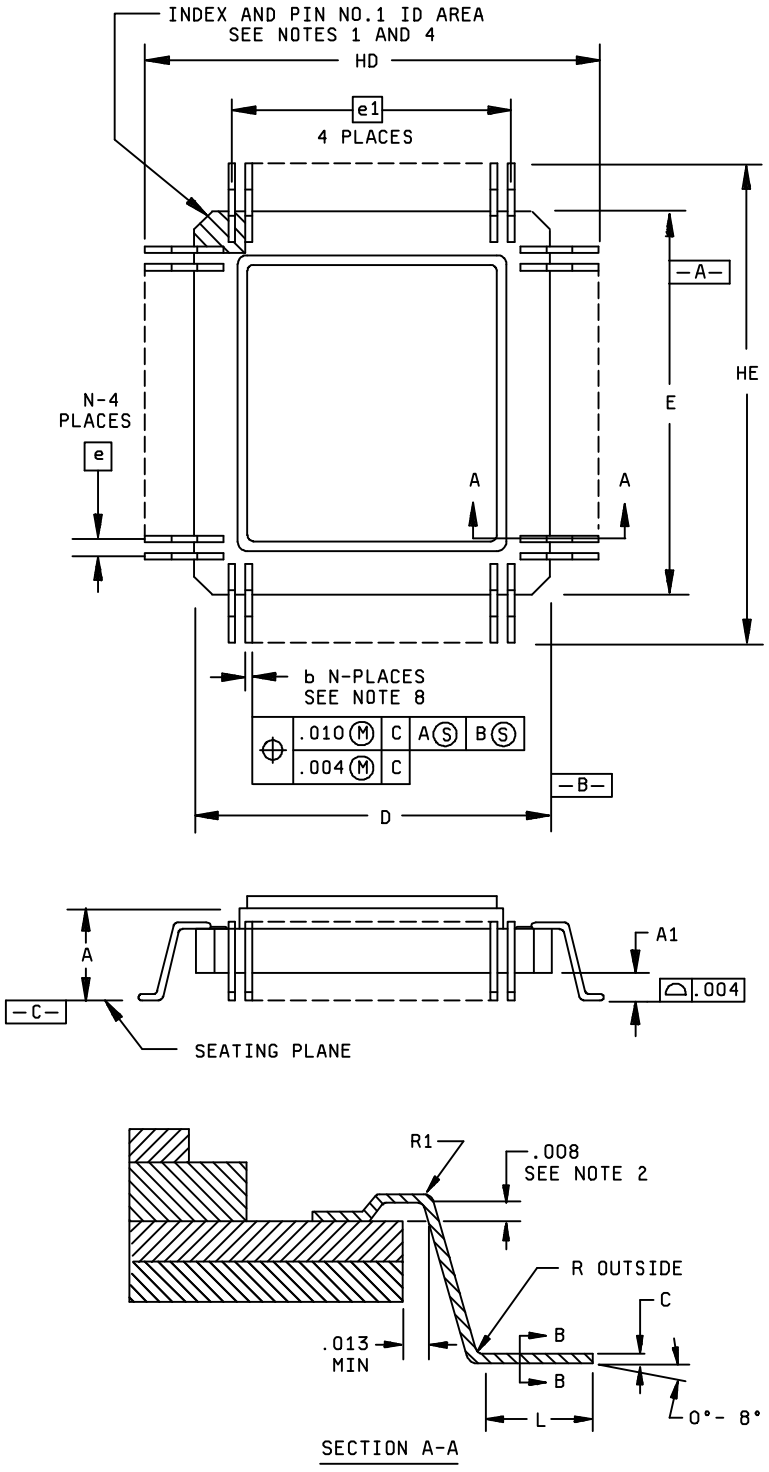
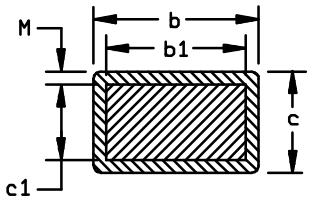


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE **A**		**5962-92010**
		REVISION LEVEL B	SHEET 18

DSCC FORM 2234
APR 97

Case Y – Continued



SECTION B-B

Symbol	Variations						Note
	Millimeters			Inches			
	Min	Nom	Max	Min	Nom	Max	
A	2.04		2.80	.080		.110	
A1	0.05	0.25	0.51	.002	.010	.020	
b	0.15		0.33	.006		.015	3
b1	0.15		0.38	.006		.013	3
c	0.11		0.26	.004		.010	3
c1	0.10		0.20	.004		.008	3
D/E	27.72	28.05	28.33	1.091	1.102	1.115	
e	0.65 BSC			.0256 BSC			
e1	25.35 BSC			.998 BSC			
HD/HE	31.00	31.26	31.51	1.218	1.228	1.238	
L	0.31	0.51	0.71	.012	.020	.028	
M			0.038			.0015	
N	160			160			4
ND/NE	40			40			5
R	0.28		0.64	.011		.025	
R1	2.55			.010			
Note	6						

NOTES:
1. A terminal 1 identification mark shall be located at the index corner in the shaded area shown. Terminal 1 is located immediately adjacent to and counterclockwise from the index corner. Terminal numbers increase in a counterclockwise direction when viewed as shown.
2. Generic lead attach dogleg depiction. May be flat configuration.
3. Dimensions b and c include lead finish; dimensions b1 and c1 apply to base metal only. Dimension M applies to plating thickness.
4. Dimension N: Number of terminals.
5. Dimensions ND/NE: Number of terminals per package edge.
6. The leads of this package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body “true positions” and lead “coplanarity” are always maintained until the next higher level package attachment process is complete. Package lead protection mechanisms (tie bars, carriers, etc.) are not shown on the drawing; however, when microcircuit devices contained in this package style are shipped for use in Government equipment, or shipped directly to the Government as spare parts or mechanical qualification samples, lead “true position” and “coplanarity” protection shall be in place.

FIGURE 1. Case outline – Continued.

Case X					
Terminal number	Symbol	Terminal number	Symbol	Terminal number	Symbol
A1	V_{SS}	B10	$\overline{\text{LBERR}}$	D4	LOCATOR PIN
A2	LD6	B11	R/$\overline{\text{W}}$	D13	CLK64M
A3	LD2	B12	$\overline{\text{RMC}}$	D14	LEDI
A4	LD1	B13	SIZ0	D15	LEDO
A5	LA7	B14	$\overline{\text{IRESET}}$	E1	$\overline{\text{LIRQ5}}$
A6	LA3	B15	$\overline{\text{ABEN}}$	E2	$\overline{\text{LIRQ1}}$
A7	LA2	C1	$\overline{\text{LIACKO}}$	E3	LAEN
A8	LA1	C2	$\overline{\text{IPL1}}$	E13	LADI
A9	$\overline{\text{CS}}$	C3	$\overline{\text{DEDLK}}$	E14	DDIR
A10	$\overline{\text{PAS}}$	C4	LD7	E15	$\overline{\text{UWDENIN}}$
A11	$\overline{\text{DSACK0}}$	C5	LD4	F1	ASIZ1
A12	$\overline{\text{HALT}}$	C6	LA6	F2	$\overline{\text{LIRQ4}}$
A13	FC2	C7	V_{SS}	F3	$\overline{\text{LIRQ3}}$
A14	SIZ1	C8	V_{DD}	F13	V_{SS}
A15	$\overline{\text{LBG}}$	C9	$\overline{\text{DS}}$	F14	$\overline{\text{LWDENIN}}$
B1	$\overline{\text{IPL2}}$	C10	$\overline{\text{RESET}}$	F15	$\overline{\text{SWDEN}}$
B2	$\overline{\text{BLT}}$	C11	FC1	G1	ASIZ0
B3	LD5	C12	$\overline{\text{LBR}}$	G2	$\overline{\text{LIRQ6}}$
B4	LD3	C13	$\overline{\text{SCON}}$	G3	$\overline{\text{LIRQ7}}$
B5	LD0	C14	LADO	G13	V_{DD}
B6	LA5	C15	V_{DD}	G14	$\overline{\text{DENO}}$
B7	LA4	D1	$\overline{\text{LIRQ2}}$	G15	$\overline{\text{ISOBE}}$
B8	LA0	D2	V_{DD}	H1	$\overline{\text{SLSEL1}}$
B9	$\overline{\text{DSACK1}}$	D3	$\overline{\text{IPL0}}$	H2	$\overline{\text{ICFSEL}}$

FIGURE 2. Terminal connections.

Case X					
Terminal number	Symbol	Terminal number	Symbol	Terminal number	Symbol
H3	V_{SS}	M13	$\overline{BGIN2}$	P8	AM2
H13	V_{SS}	M14	$\overline{BGOUT0}$	P9	$\overline{LWORD}$
H14	D6	M15	$\overline{BGOUT3}$	P10	$\overline{WRITE}$
H15	D7	N1	V_{DD}	P11	$\overline{DS1}$
J1	$\overline{WORD}$	N2	A7	P12	$\overline{BR1}$
J2	$\overline{MWB}$	N3	$\overline{IRQ2}$	P13	$\overline{BR3}$
J3	$\overline{SLSEL0}$	N4	$\overline{IRQ5}$	P14	$\overline{BGIN1}$
J13	V_{DD}	N5	$\overline{SYSFAIL}$	P15	SYSCLK
J14	D3	N6	$\overline{IACKIN}$	R1	$\overline{IRQ4}$
J15	D5	N7	V_{SS}	R2	$\overline{IRQ7}$
K1	$\overline{FCIACK}$	N8	V_{SS}	R3	$\overline{ACFAIL}$
K2	A1	N9	V_{DD}	R4	$\overline{IACKOUT}$
K3	V_{SS}	N10	$\overline{BERR}$	R5	$\overline{DTACK}$
K13	D0	N11	$\overline{BR2}$	R6	AM0
K14	D1	N12	$\overline{BBSY}$	R7	AM1
K15	D4	N13	$\overline{BGIN0}$	R8	AM3
L1	A2	N14	$\overline{BGIN3}$	R9	AM4
L2	A3	N15	$\overline{BGOUT2}$	R10	AM5
L3	A6	P1	V_{SS}	R11	$\overline{DS0}$
L13	$\overline{BGOUT1}$	P2	$\overline{IRQ3}$	R12	$\overline{BR0}$
L14	V_{SS7}	P3	$\overline{IRQ6}$	R13	V_{SS}
L15	D2	P4	V_{DD}	R14	$\overline{BCLR}$
M1	A4	P5	$\overline{SYSRESET}$	R15	V_{SS}
M2	A5	P6	$\overline{IACK}$		
M3	$\overline{IRQ1}$	P7	$\overline{AS}$		

FIGURE 2. Terminal connections – Continued.

Case Y					
Terminal number	Symbol	Terminal number	Symbol	Terminal number	Symbol
1	V_{SS}	28	A3	55	V_{SS}
2	V_{SS}	29	A4	56	AM0
3	$\overline{IPL0}$	30	V_{DD}	57	AM1
4	$\overline{IPL1}$	31	A5	58	AM2
5	$\overline{IPL2}$	32	A6	59	AM3
6	V_{DD}	33	A7	60	V_{SS}
7	LAEN	34	V_{SS}	61	V_{DD}
8	$\overline{LIACKO}$	35	$\overline{IRQ1}$	62	AM4
9	$\overline{LIRQ1}$	36	$\overline{IRQ2}$	63	AM5
10	$\overline{LIRQ2}$	37	$\overline{IRQ3}$	64	$\overline{LWORD}$
11	$\overline{LIRQ3}$	38	$\overline{IRQ4}$	65	$\overline{WRITE}$
12	$\overline{LIRQ4}$	39	V_{SS}	66	$\overline{BERR}$
13	$\overline{LIRQ5}$	40	V_{SS}	67	$\overline{DS0}$
14	$\overline{LIRQ6}$	41	V_{DD}	68	$\overline{DS1}$
15	$\overline{LIRQ7}$	42	V_{DD}	69	$\overline{BR0}$
16	ASIZ1	43	$\overline{IRQ5}$	70	V_{SS}
17	ASIZ0	44	$\overline{IRQ6}$	71	$\overline{BR1}$
18	$\overline{ICFSEL}$	45	$\overline{IRQ7}$	72	$\overline{BR2}$
19	$\overline{SLSEL1}$	46	V_{DD}	73	$\overline{BR3}$
20	V_{SS}	47	$\overline{SYSFAIL}$	74	$\overline{BCLR}$
21	$\overline{SLSEL0}$	48	$\overline{ACFAIL}$	75	$\overline{BBSY}$
22	$\overline{WORD}$	49	$\overline{SYSRESET}$	76	$\overline{BGIN0}$
23	$\overline{FCIACK}$	50	$\overline{IACKOUT}$	77	$\overline{BGIN1}$
24	$\overline{MWB}$	51	$\overline{IACKIN}$	78	V_{SS}
25	A1	52	$\overline{IACK}$	79	V_{DD}
26	V_{SS}	53	$\overline{DTACK}$	80	V_{DD}
27	A2	54	$\overline{AS}$	81	V_{SS}

FIGURE 2. Terminal connections - Continued.

Case Y					
Terminal number	Symbol	Terminal number	Symbol	Terminal number	Symbol
82	V_{SS}	109	LEDO	136	$\overline{PAS}$
83	$\overline{BGIN2}$	110	V_{DD}	137	$\overline{CS}$
84	$\overline{BGIN3}$	111	LEDI	138	LA0
85	SYSCLK	112	LADI	139	LA1
86	$\overline{BGOUT0}$	113	LADO	140	V_{DD}
87	$\overline{BGOUT1}$	114	$\overline{ABEN}$	141	V_{SS}
88	$\overline{BGOUT2}$	115	CLK64M	142	LA2
89	V_{SS}	116	$\overline{SCON}$	143	LA3
90	$\overline{BGOUT3}$	117	$\overline{IRESET}$	144	LA4
91	D0	118	$\overline{LBG}$	145	LA5
92	D1	119	V_{SS}	146	LA6
93	D2	120	V_{SS}	147	LA7
94	D3	121	V_{DD}	148	LD0
95	V_{DD}	122	V_{DD}	149	LD1
96	D4	123	$\overline{LBR}$	150	LD2
97	D5	124	SIZ0	151	LD3
98	D6	125	SIZ1	152	LD4
99	D7	126	$\overline{RMC}$	153	LD5
100	V_{SS}	127	FC1	154	LD6
101	V_{DD}	128	FC2	155	LD7
102	$\overline{ISOBE}$	129	R/$\overline{W}$	156	$\overline{DEDLK}$
103	$\overline{SWDEN}$	130	$\overline{HALT}$	157	$\overline{BLT}$
104	$\overline{DENO}$	131	$\overline{RESET}$	158	V_{SS}
105	$\overline{LWDENIN}$	132	$\overline{LBERR}$	159	V_{DD}
106	V_{SS}	133	$\overline{DSACK0}$	160	V_{DD}
107	$\overline{UWDENIN}$	134	$\overline{DSACK1}$		
108	DDIR	135	$\overline{DS}$		

FIGURE 2. Terminal connections – Continued.

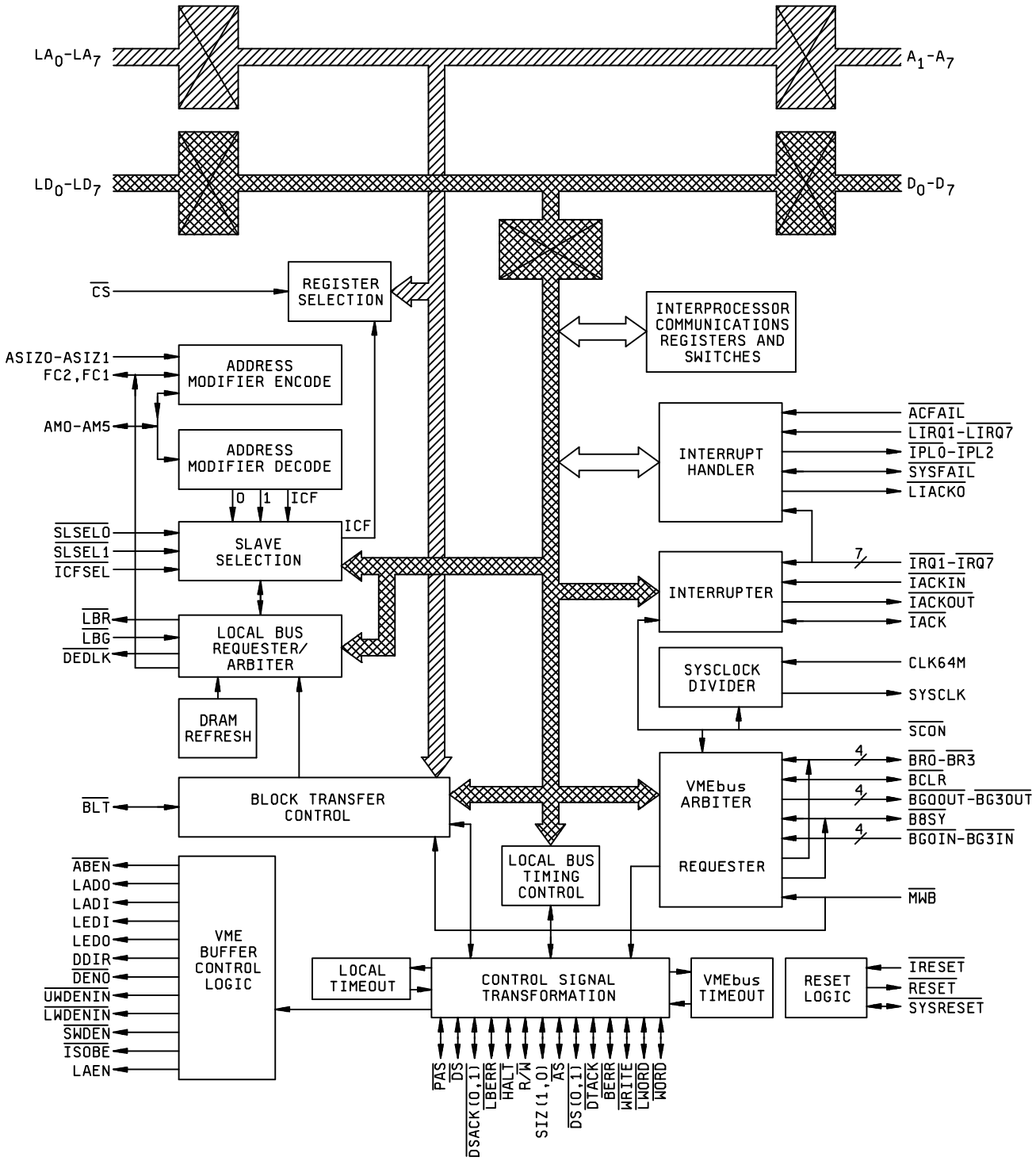


FIGURE 3. Block diagram.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-92010
		REVISION LEVEL B	SHEET 24

DSCC FORM 2234
APR 97

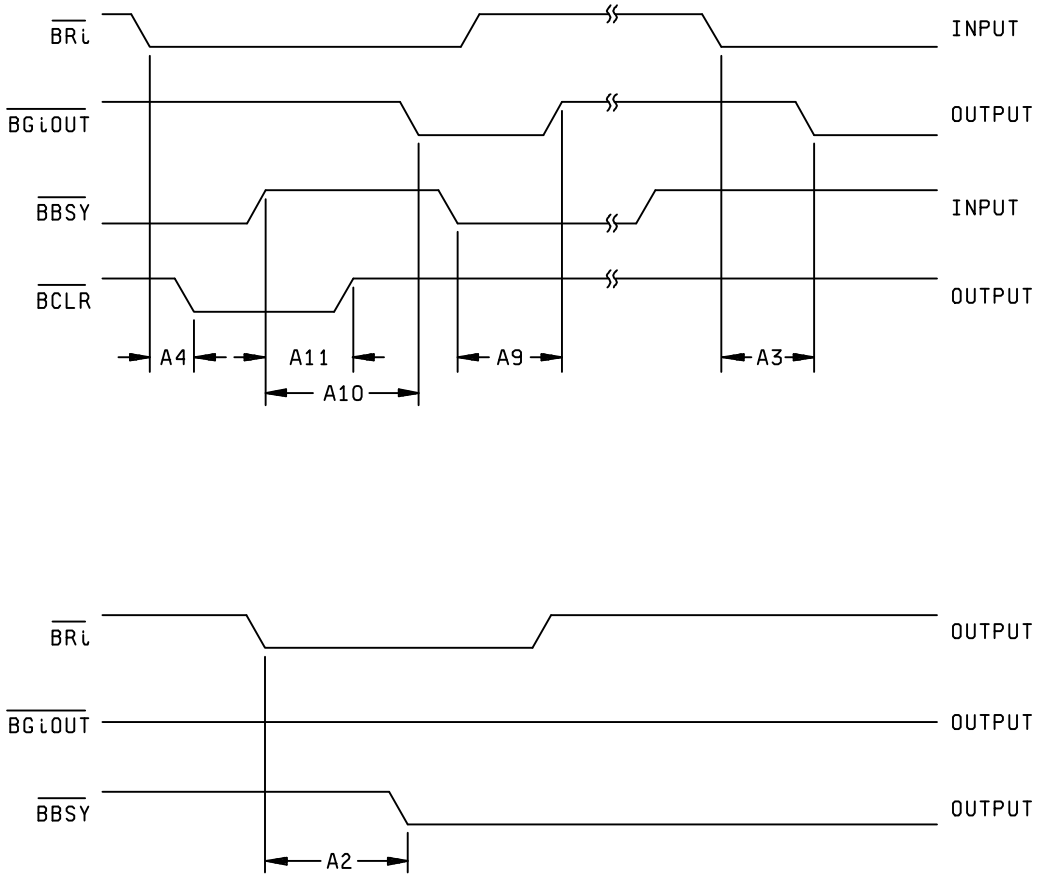


FIGURE 4. Timing waveforms.

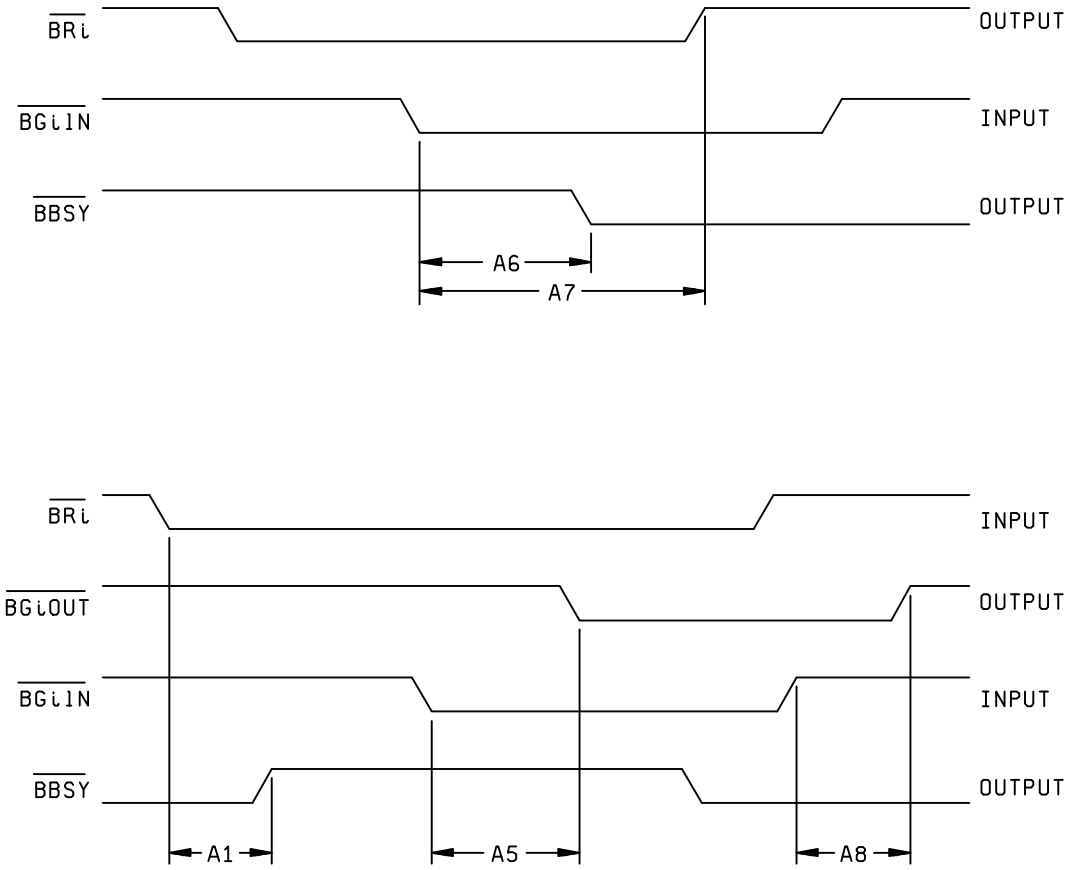


FIGURE 4. Timing waveforms - Continued.

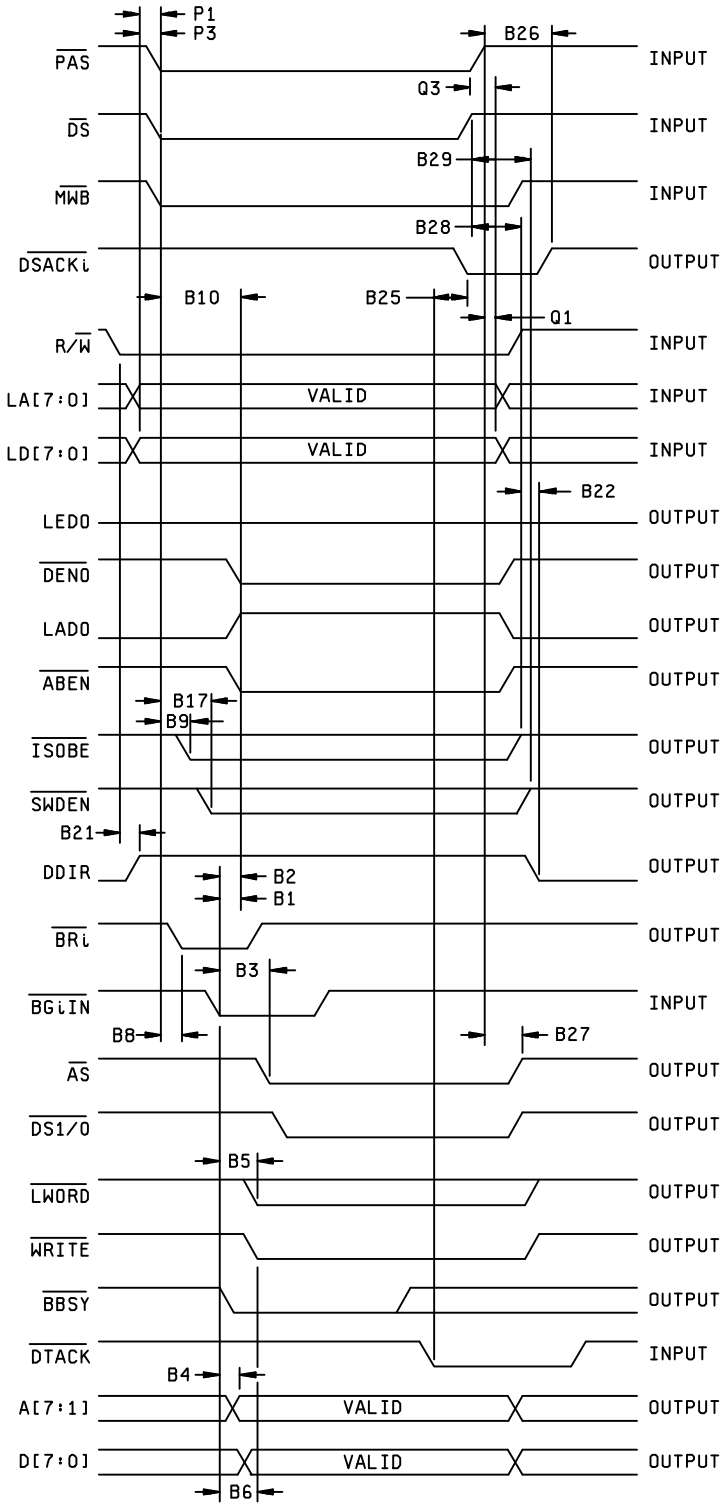


FIGURE 4. Timing waveforms - Continued.

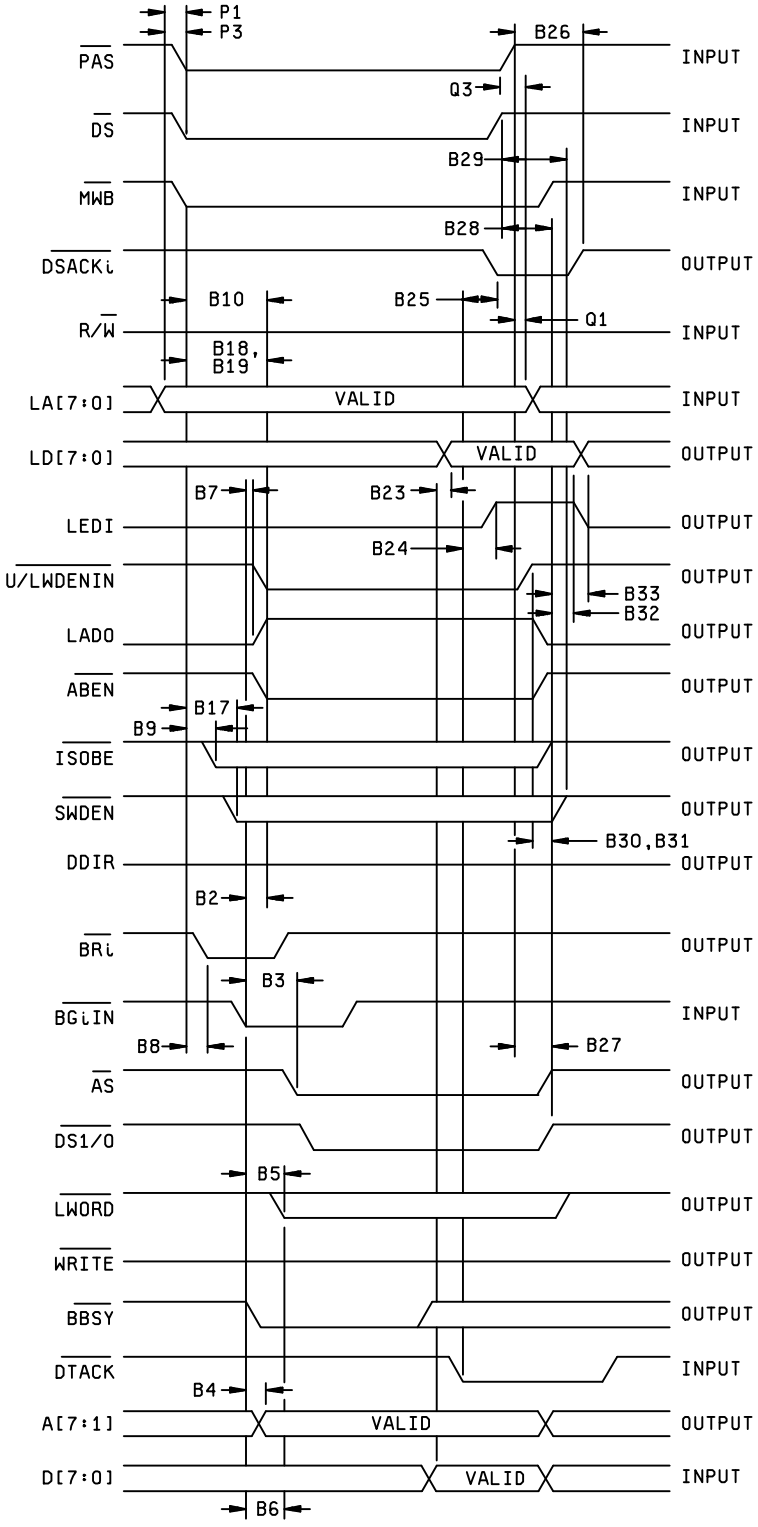


FIGURE 4. Timing waveforms - Continued.

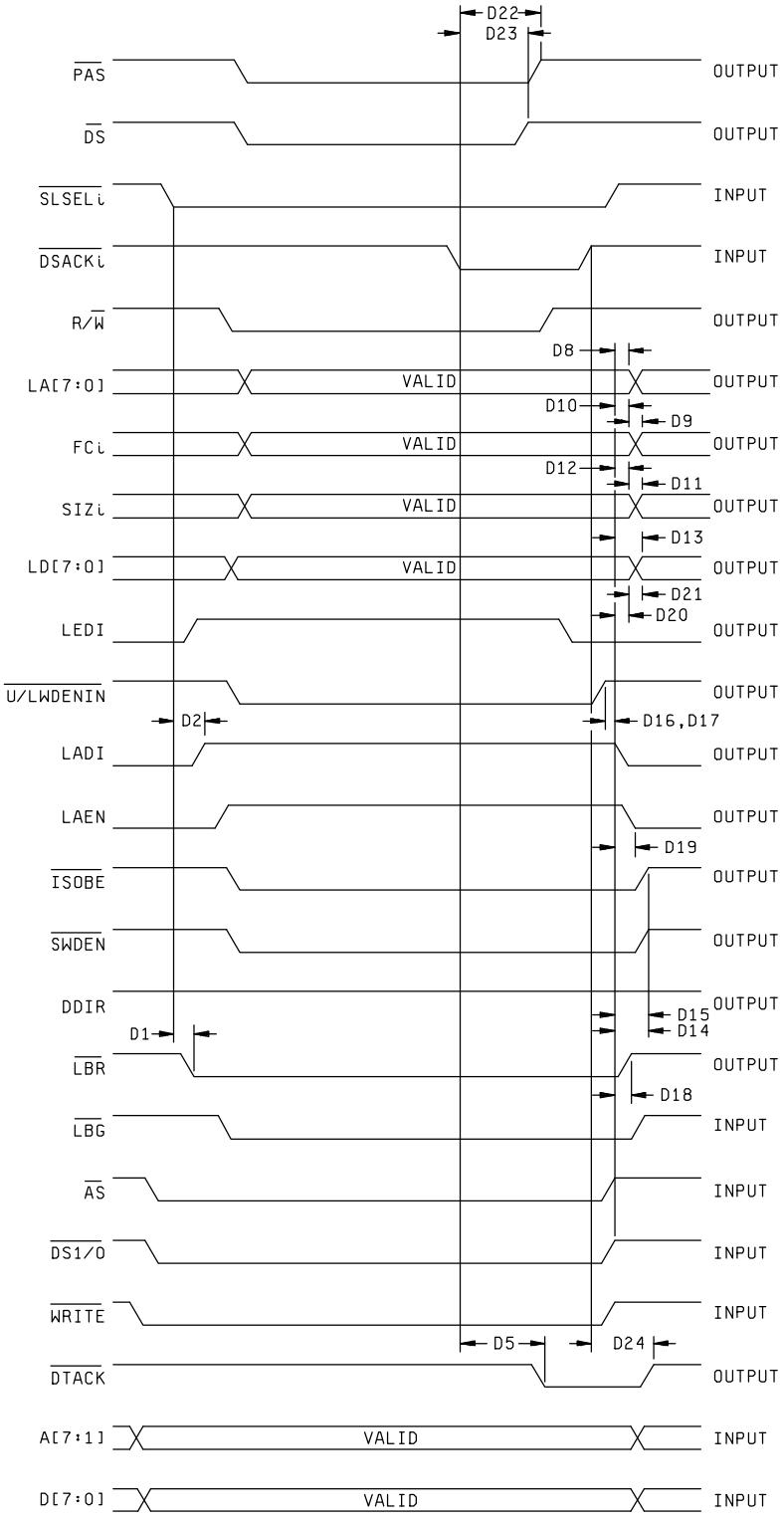


FIGURE 4. Timing waveforms - Continued.

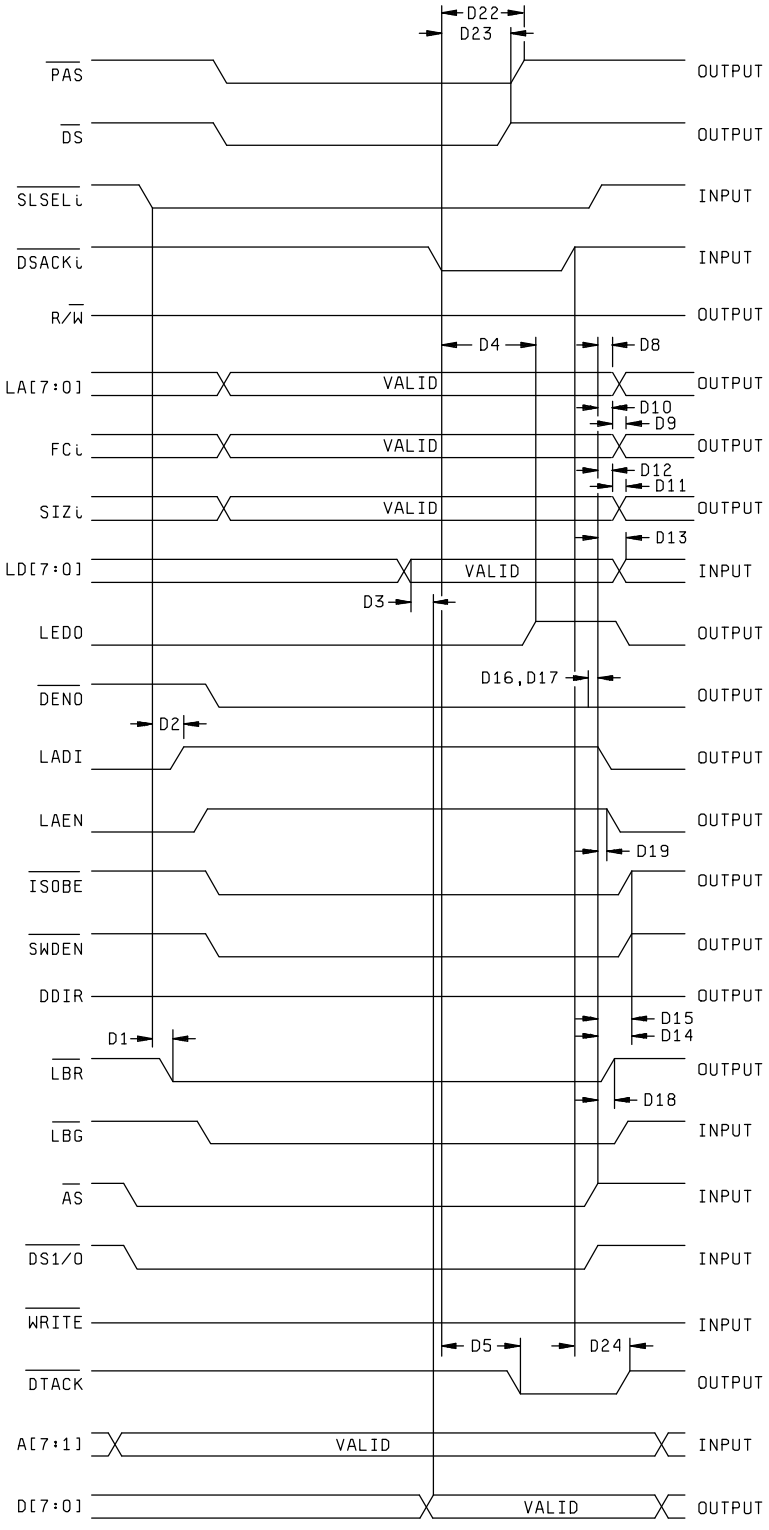


FIGURE 4. Timing waveforms - Continued.

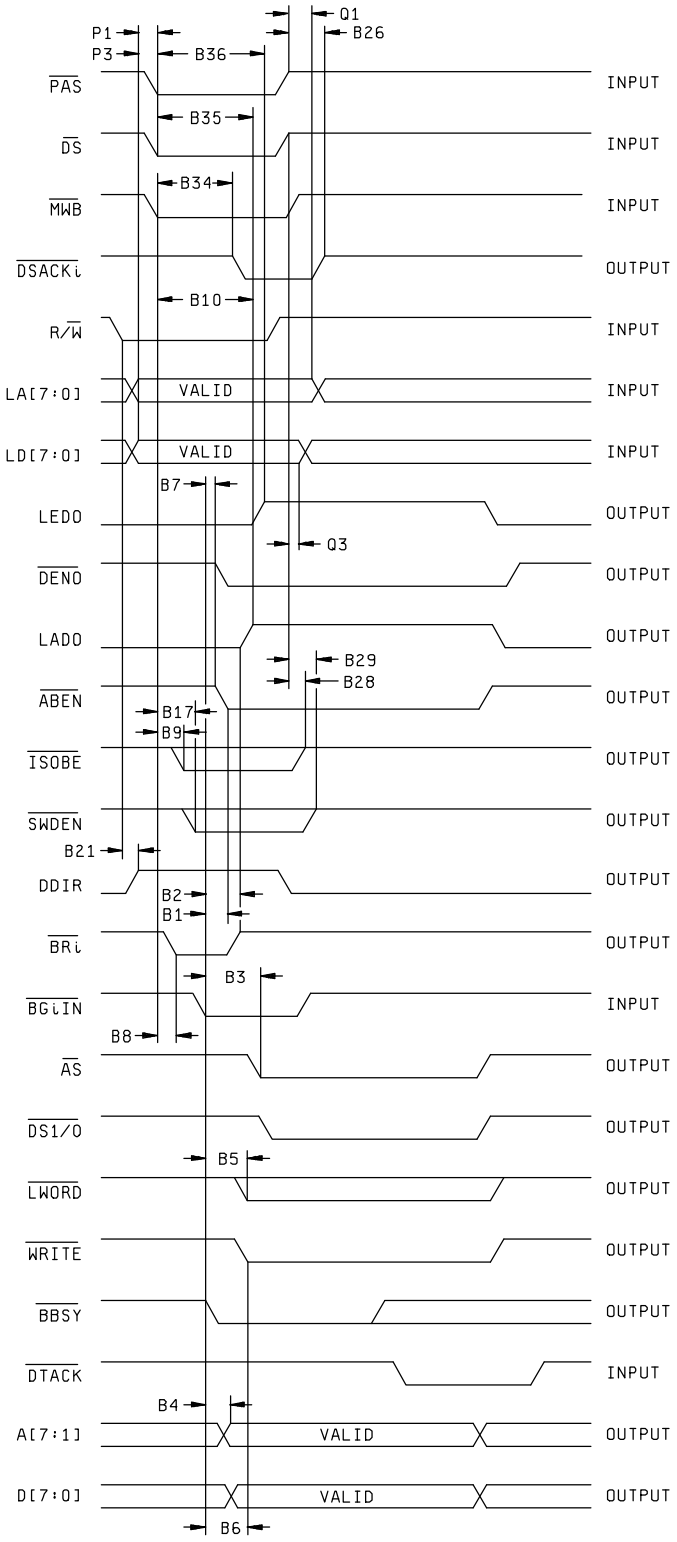


FIGURE 4. Timing waveforms - Continued.

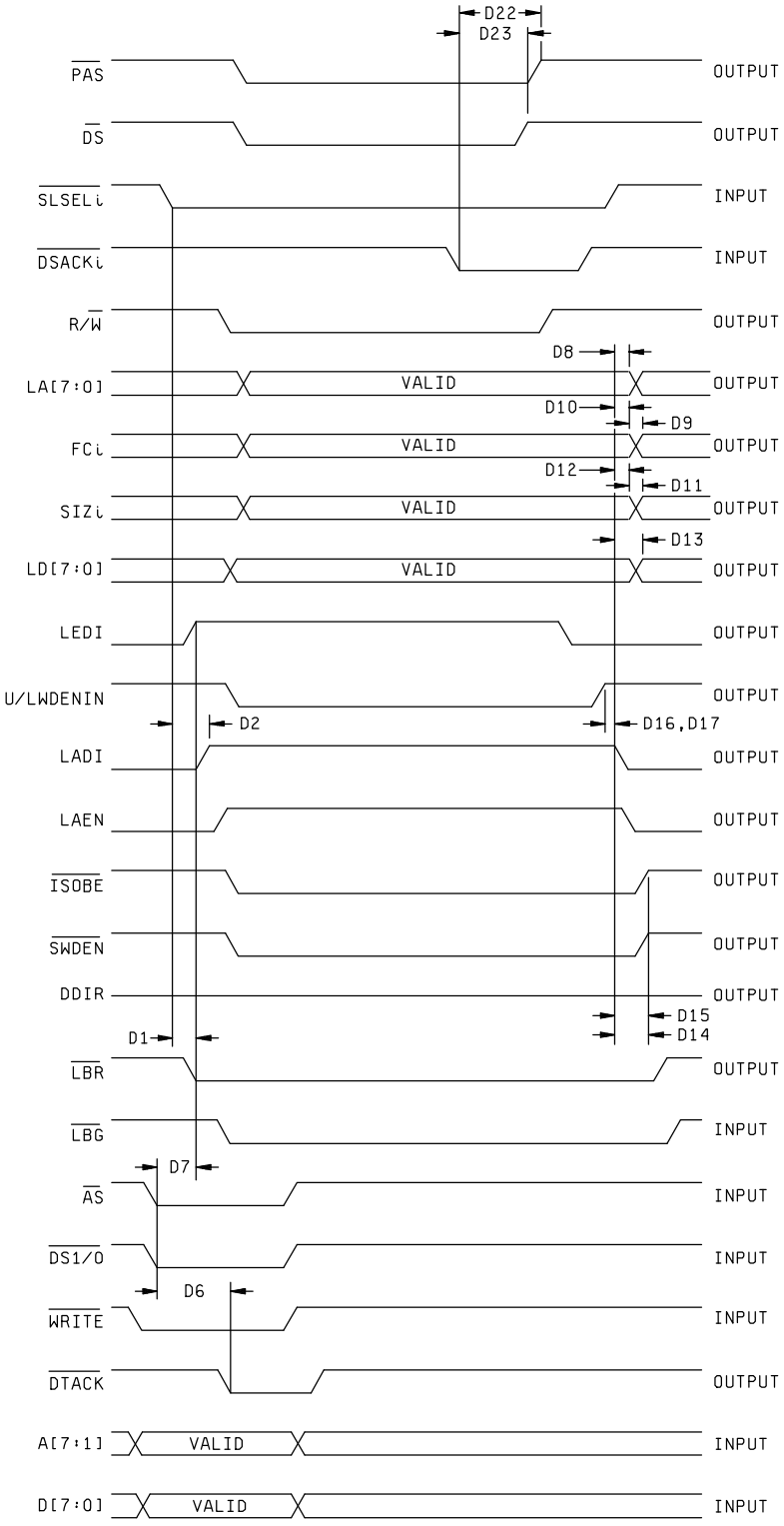


FIGURE 4. Timing waveforms - Continued.

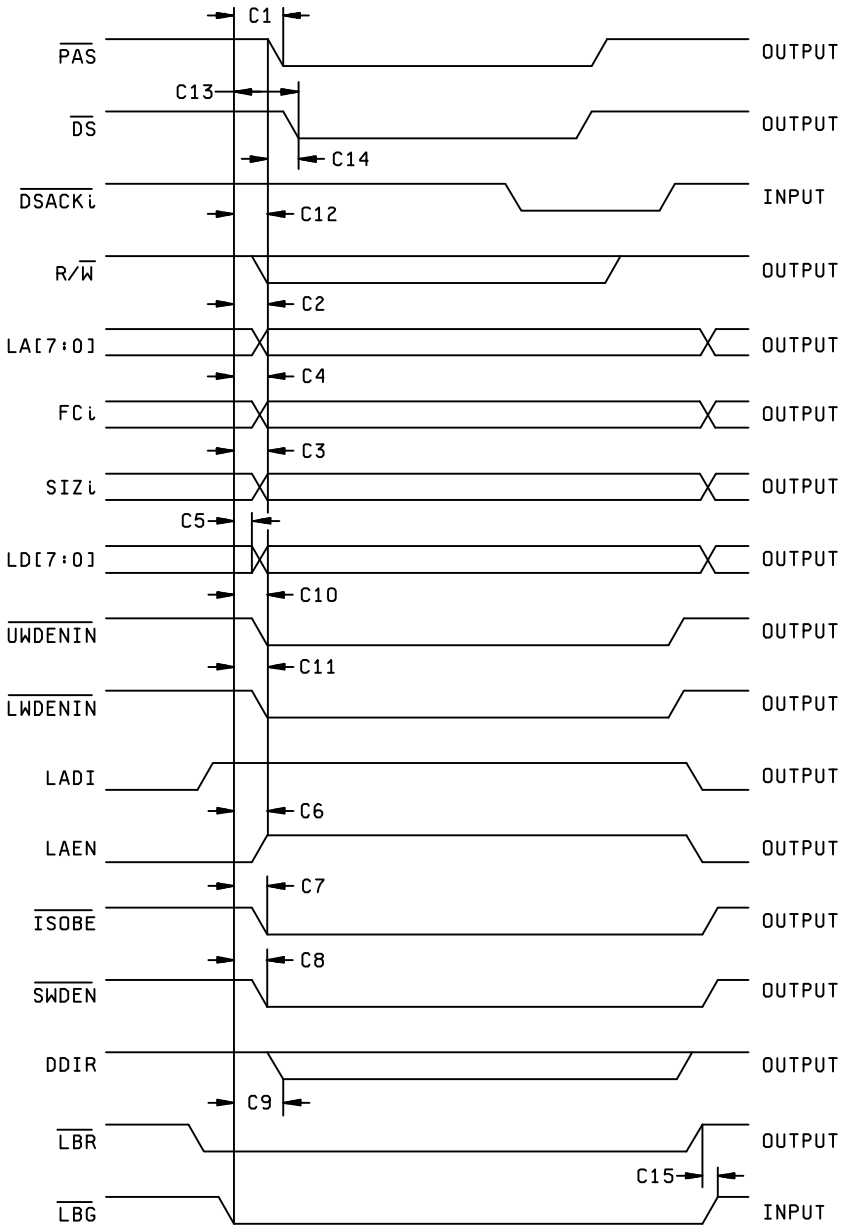


FIGURE 4. Timing waveforms - Continued.

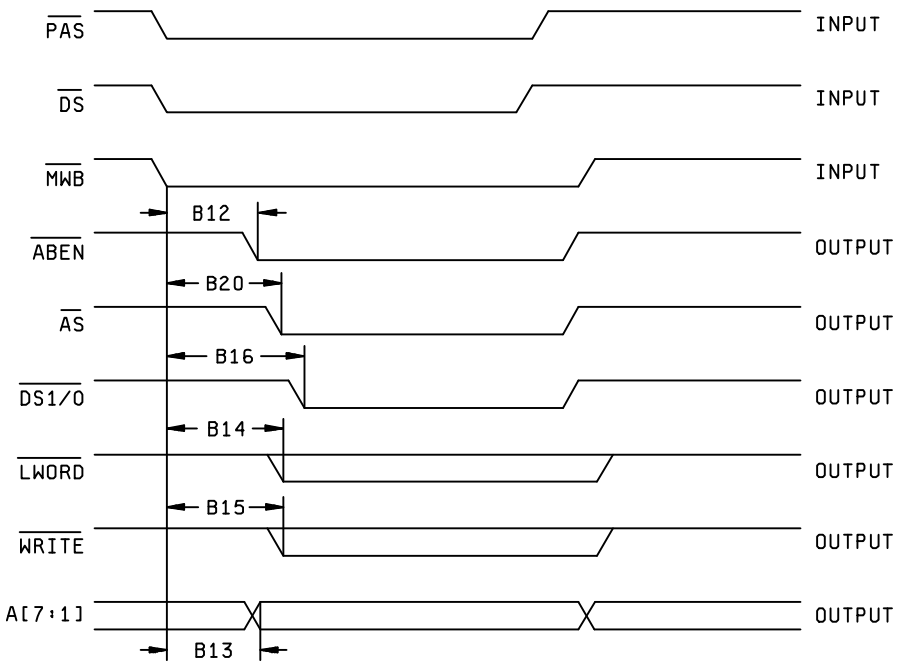


FIGURE 4. Timing waveforms - Continued.

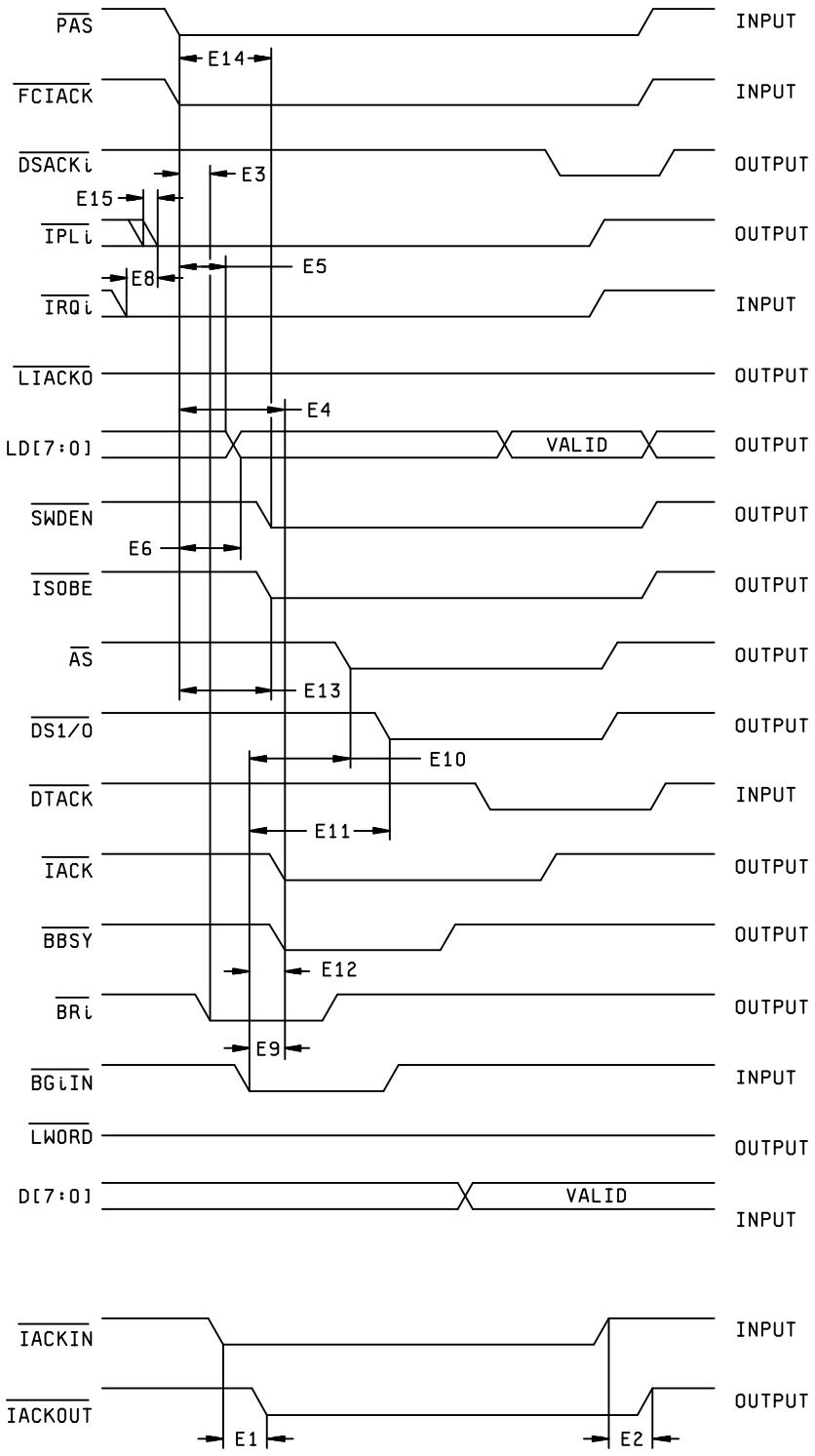
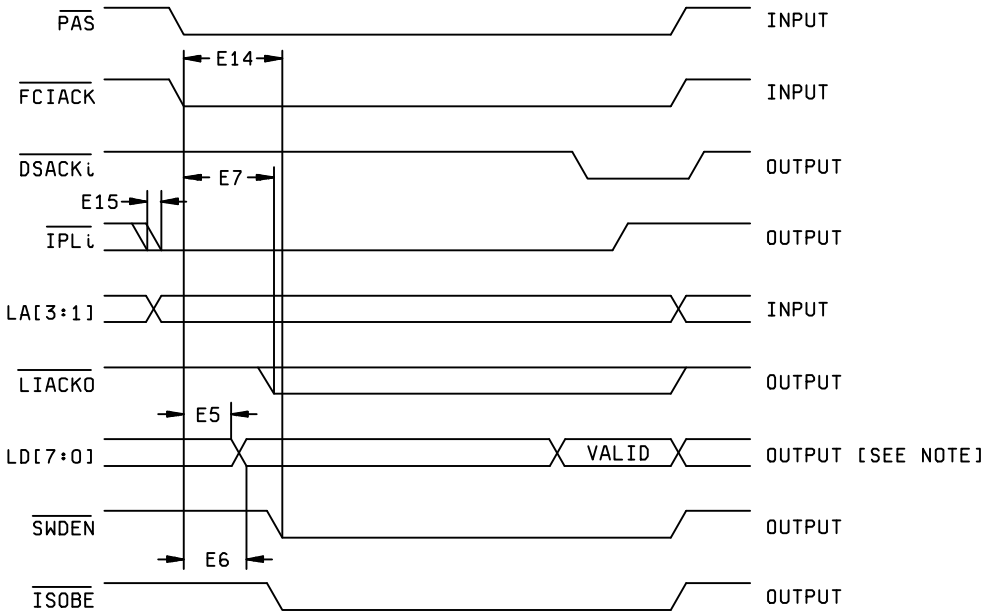


FIGURE 4. Timing waveforms - Continued.



NOTE: IF THE DEVICE IS CONFIGURED TO SUPPLY VECTOR.

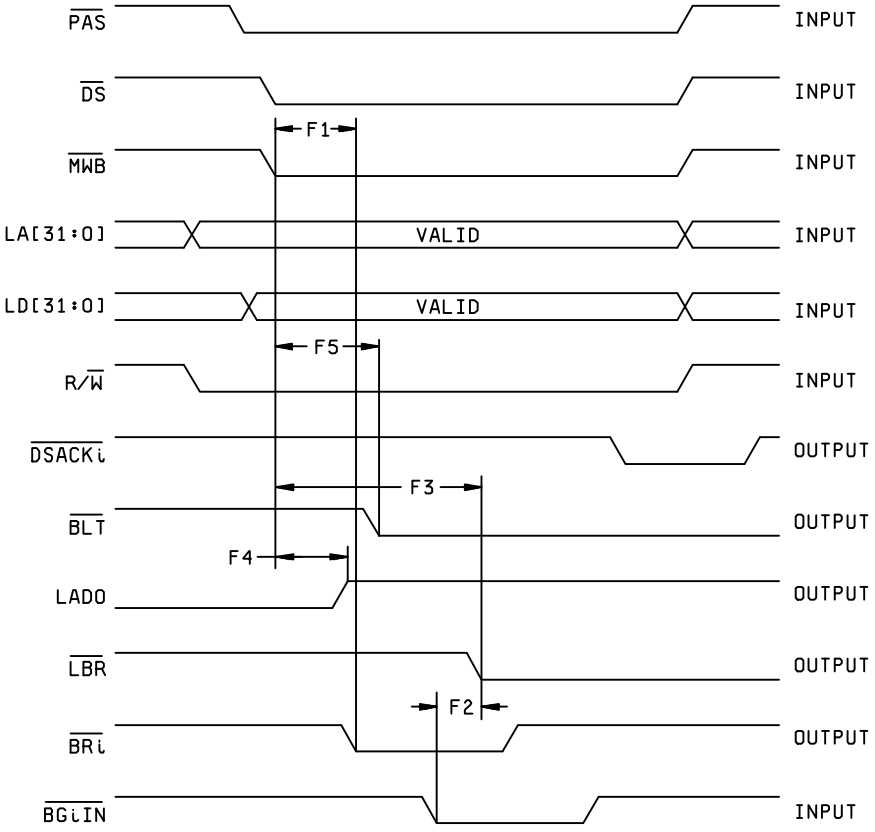


FIGURE 4. Timing waveforms - Continued.

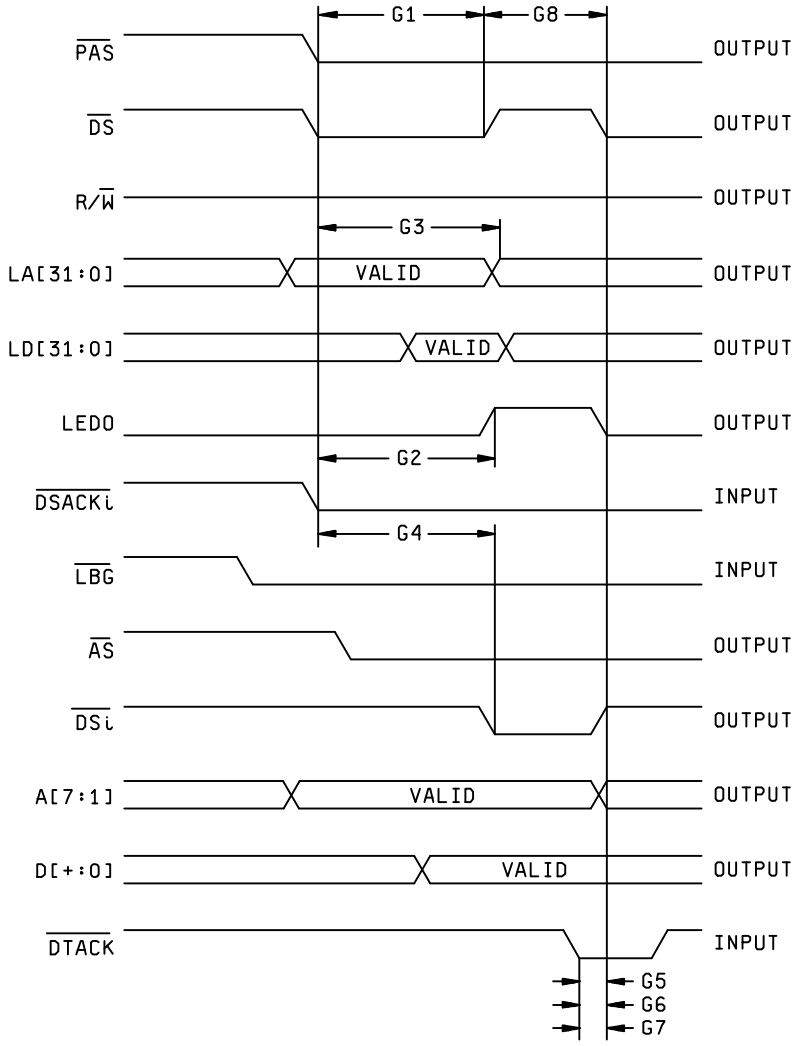


FIGURE 4. Timing waveforms - Continued.

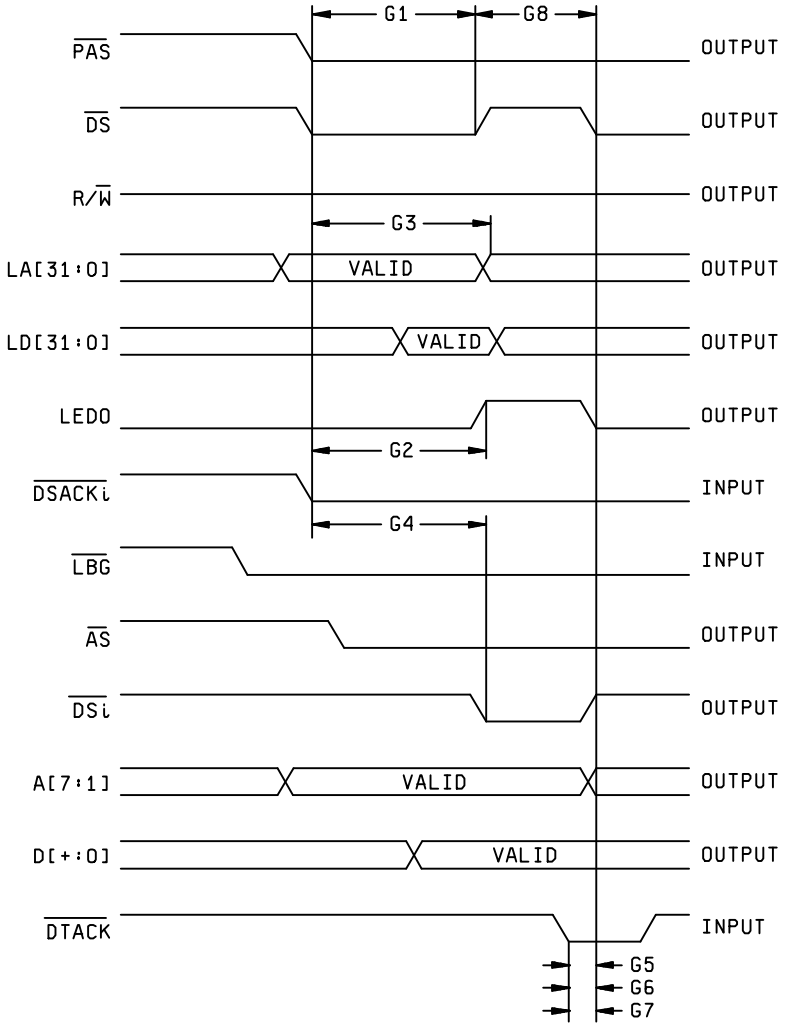


FIGURE 4. Timing waveforms - Continued.

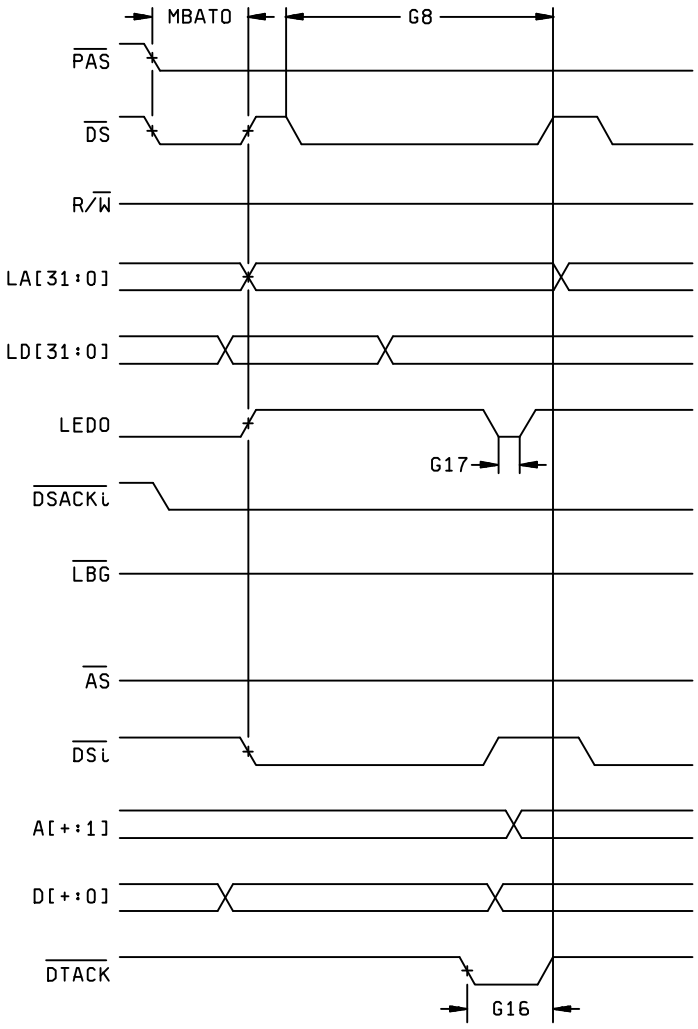


FIGURE 4. Timing waveforms - Continued.

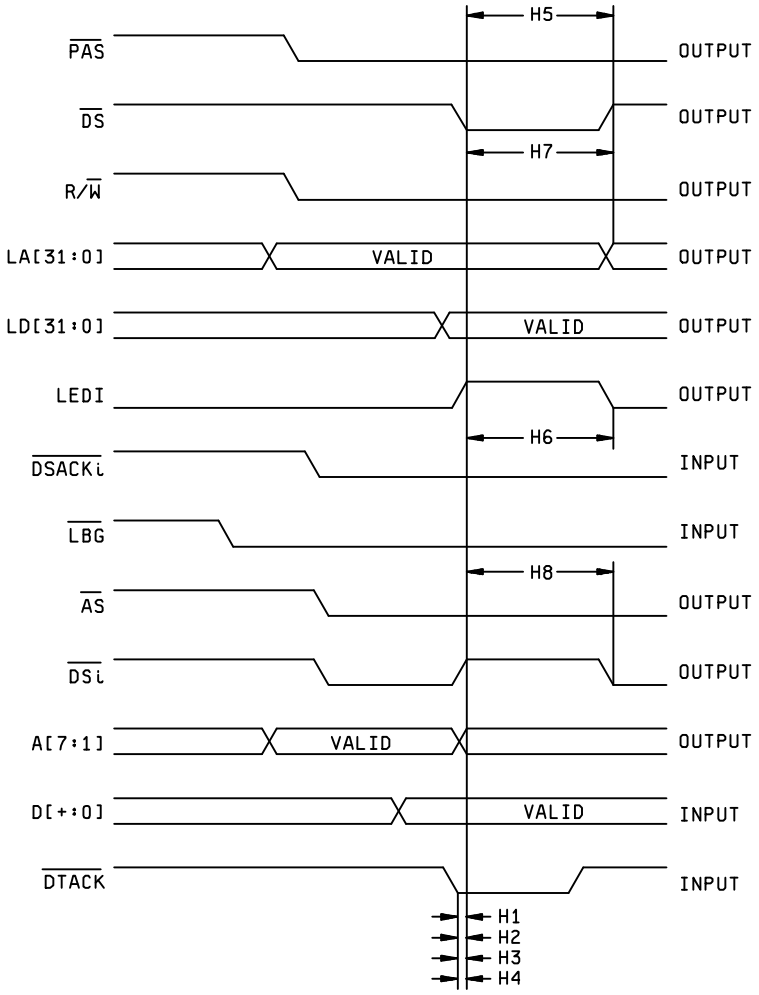
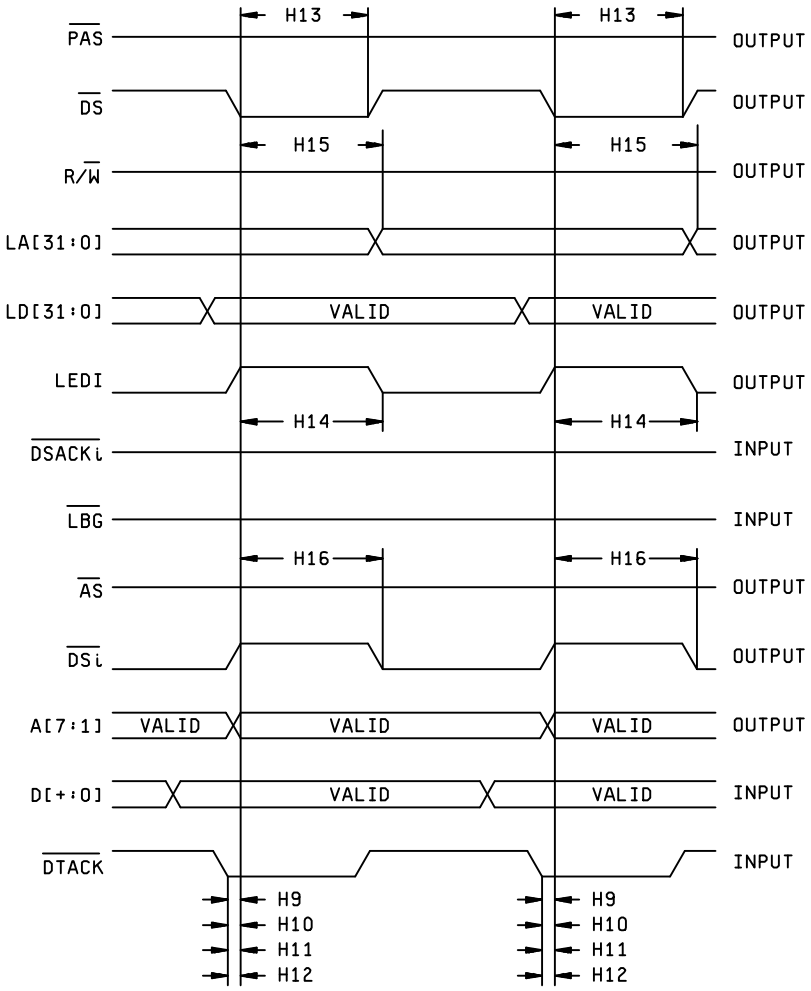


FIGURE 4. Timing waveforms - Continued.



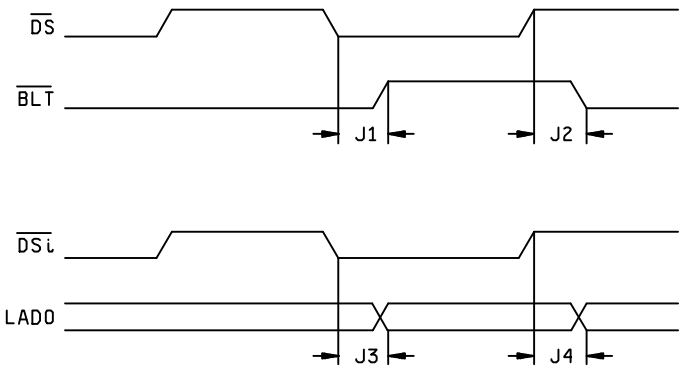


FIGURE 4. Timing waveforms - Continued.

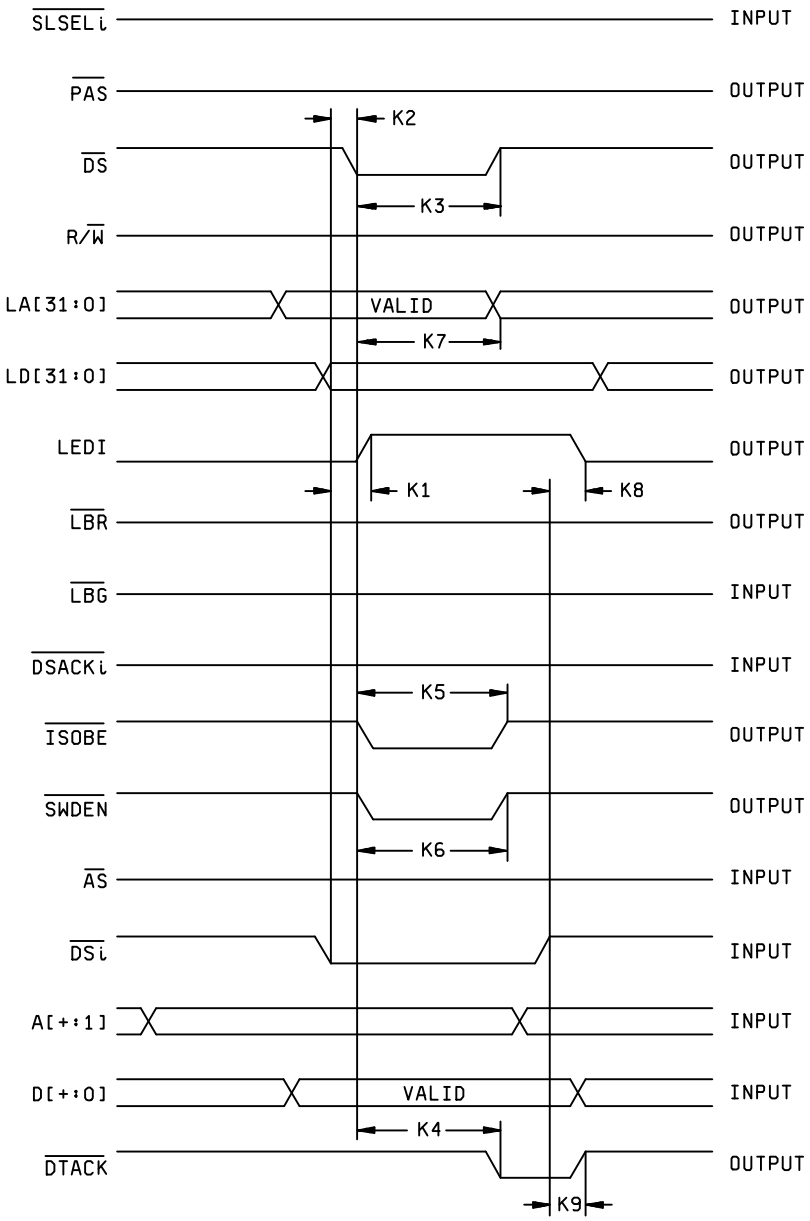


FIGURE 4. Timing waveforms - Continued.

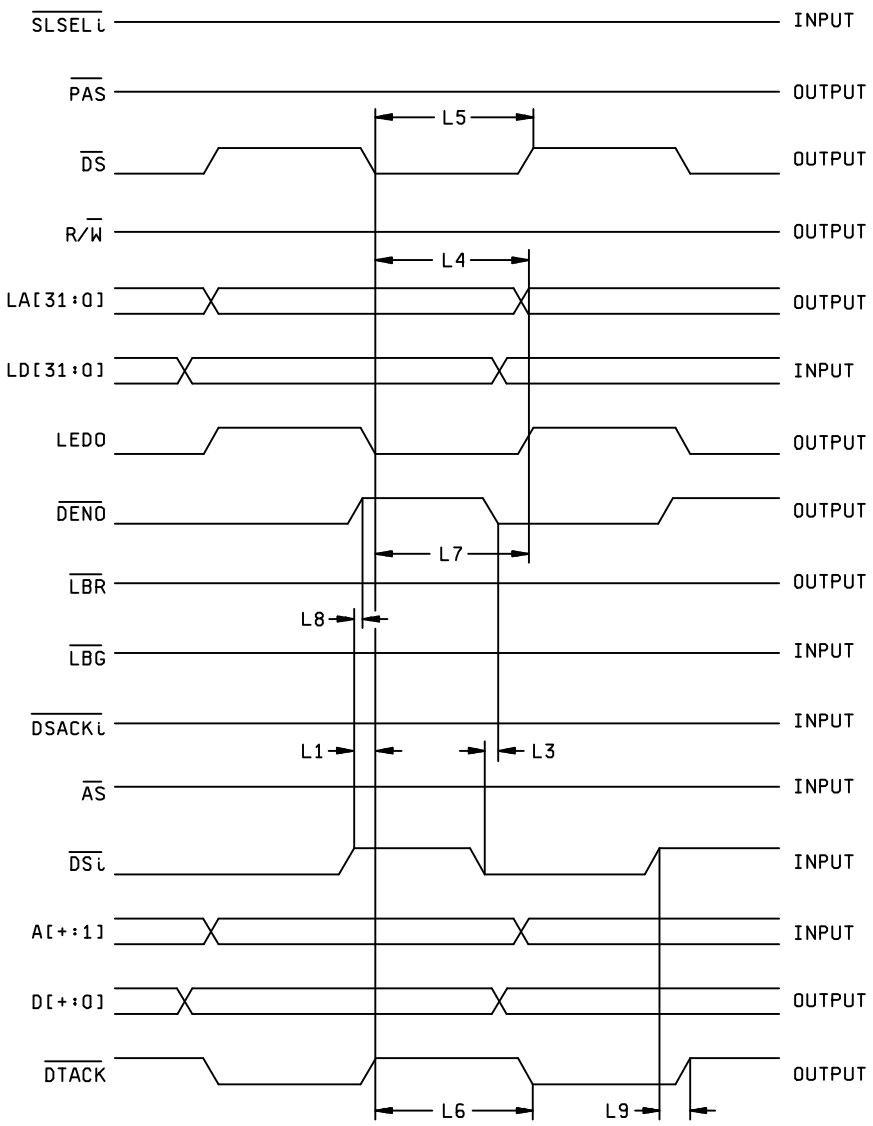


FIGURE 4. Timing waveforms - Continued.

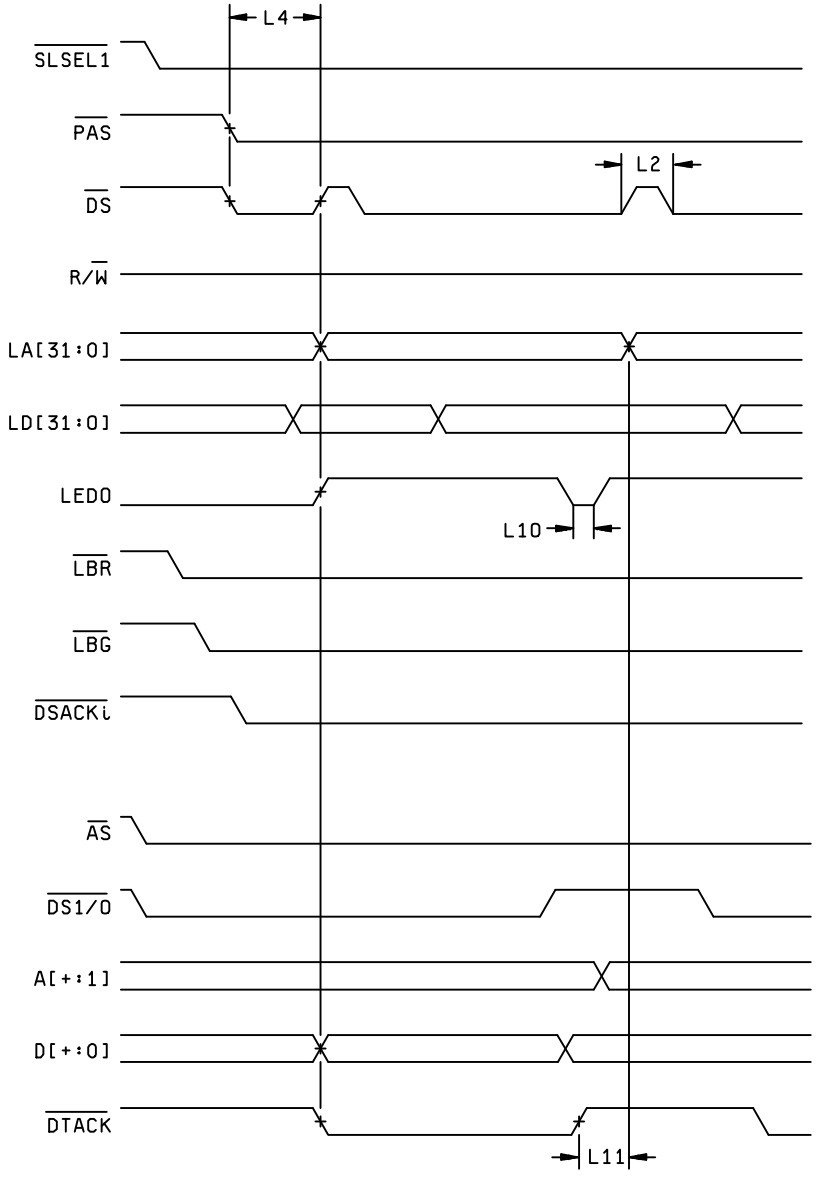


FIGURE 4. Timing waveforms - Continued.

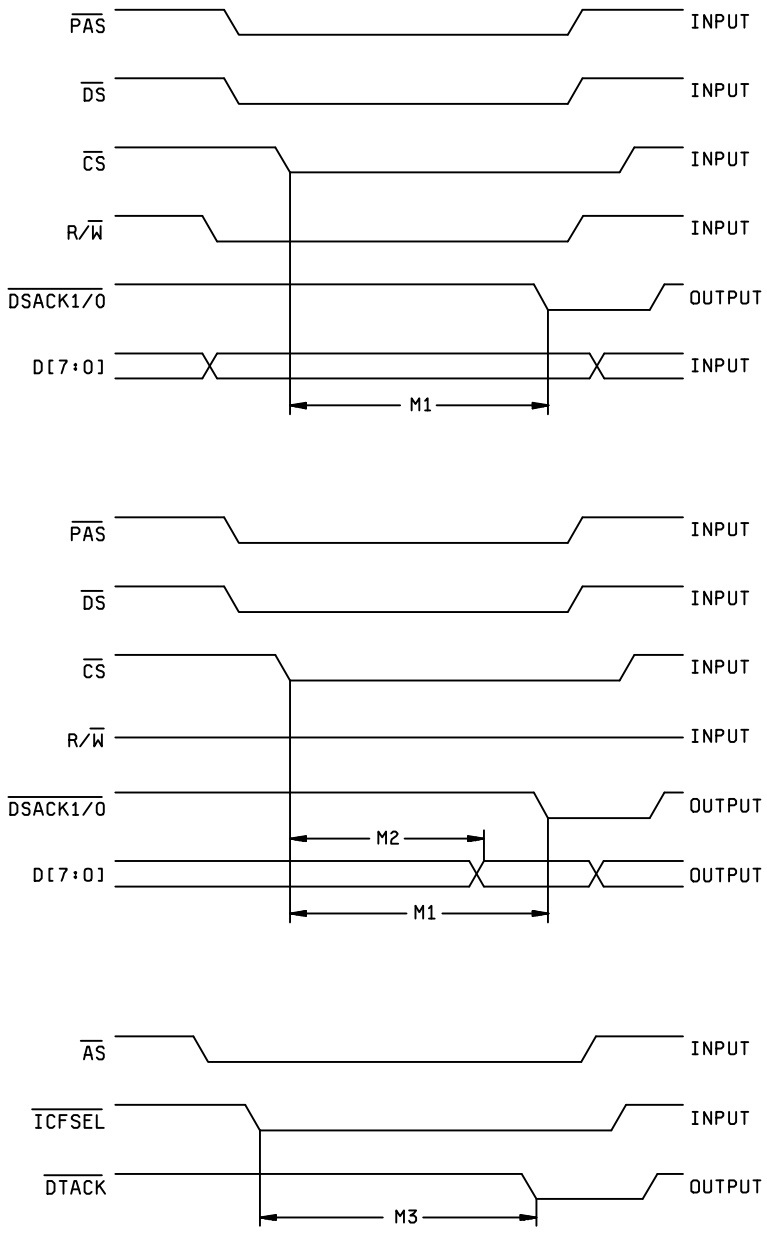


FIGURE 4. Timing waveforms - Continued.

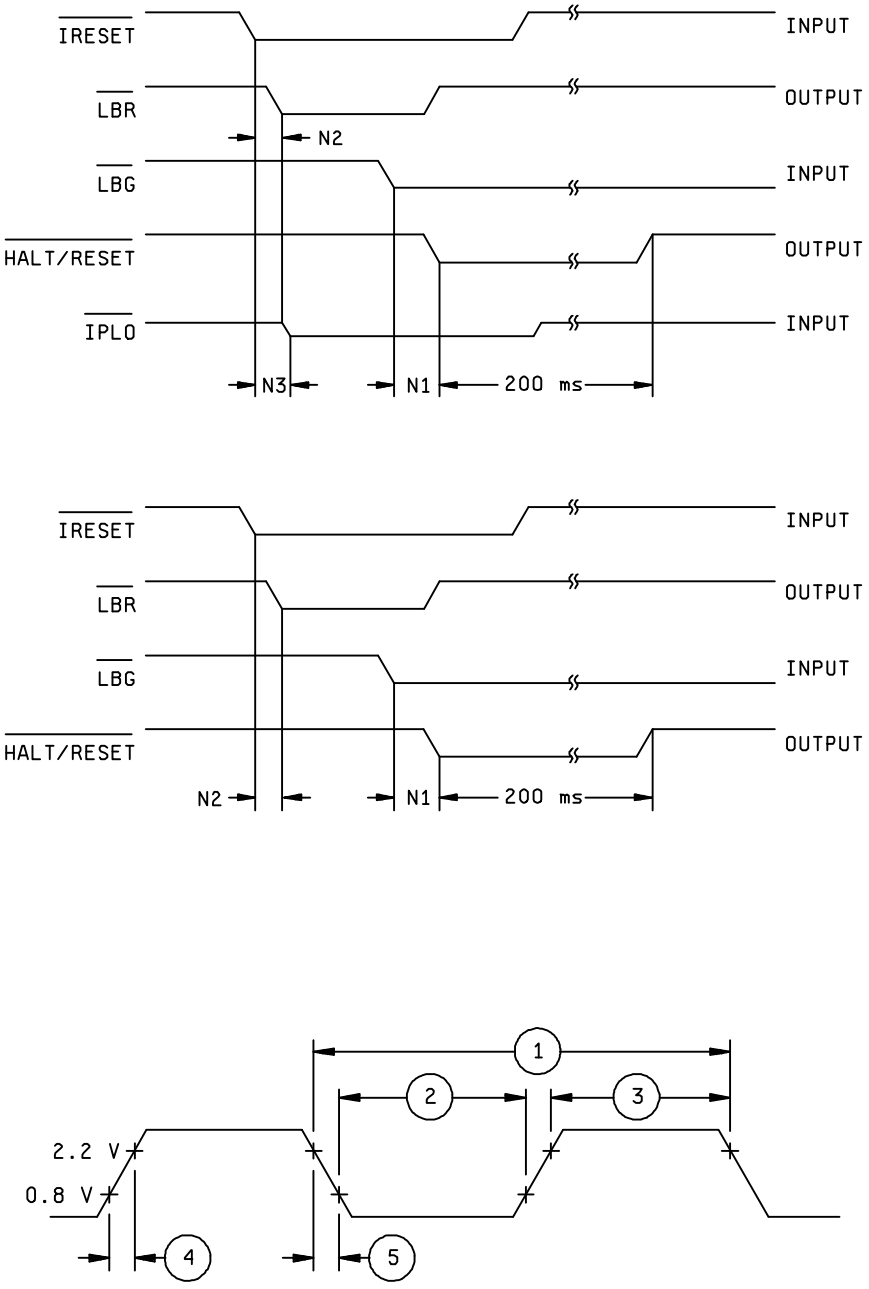


FIGURE 4. Timing waveforms - Continued.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample of five devices with zero failures shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)			1, 7
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8A, 10	2, 8A, 10
Group D end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8A, 10	2, 7, 8A, 10
Group E end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8A, 10	2, 8A, 10

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and table III herein.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

TABLE III. Pin description.

Symbol	Name and function
$\overline{\text{SYSRESET}}$	The VMEbus system reset signal is both an input and an open collector output. A LOW level on this signal resets the internal logic of the device and asserts the signals $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$. These signals remain asserted for a minimum of 200 ms. If the device is configured as VMEbus system controller, a LOW level on $\overline{\text{IRESET}}$ asserts $\overline{\text{SYSRESET}}$ for a minimum of 200 ms.
$\overline{\text{ACFAIL}}$	The VME AC fail signal is an input. This should be driven by the VMEbus power monitor (if installed). The device can be enabled to provide a local interrupt on the assertion of this signal.
$\overline{\text{SYSFAIL}}$	The VMEbus system fail signal is both an input and an open collector output. As an output the $\overline{\text{SYSFAIL}}$ signal is asserted when $\overline{\text{HALT}}$ has been detected asserted for more than 6 µs (by a source other than the device). This signal is asserted by the device after a global reset. It may be masked by clearing ICR6[6] or by setting ICR7[7]. The device can also be enabled to provide a local interrupt on the assertion of this signal.
SYSCLK	The VMEbus system clock is a three-state output. This signal is driven by the device when configured as system controller ($\overline{\text{SCON}}$ asserted). The frequency driven is 1/4 of the frequency delivered to the device CLK64M signal. To deliver the required 16 MHz on this signal, the device must run at 64 MHz. The device does not use this signal internally for any purpose.
$\overline{\text{BR3}}$ - $\overline{\text{BR0}}$	The VMEbus bus request signals are both inputs and open collector outputs.
$\overline{\text{BGIN3}}$ - $\overline{\text{BGIN0}}$	The VMEbus daisy-chained bus-grant-in signals are inputs.
$\overline{\text{BGOUT3}}$ - $\overline{\text{BGOUT0}}$	The VMEbus daisy-chained bus-grant-out signals are outputs.
$\overline{\text{BBSY}}$	The VMEbus bus-busy signal is both an input and a rescinding output.
$\overline{\text{BCLR}}$	The VMEbus bus-clear signal is both an input and a three-state output.
D7 – D0	The VMEbus low-order data lines are both inputs and three-state outputs.
A7 – A1	The VMEbus low-order address lines are both inputs and three-state outputs.
$\overline{\text{AS}}$	The VMEbus address strobe signal is both an input and rescinding output.
$\overline{\text{DS1}}$ - $\overline{\text{DS0}}$	The VMEbus data strobe signals are both inputs and rescinding outputs.
$\overline{\text{DTACK}}$	The VMEbus data-transfer-acknowledge signal is both an input and a rescinding output.
$\overline{\text{BERR}}$	The VMEbus bus-error signal is both an input and a rescinding output.
$\overline{\text{WRITE}}$	The VMEbus data-direction signal is both an input and a three-state output.
$\overline{\text{LWORD}}$	The VMEbus long-word signal is both an input and a three-state output.
AM5 - AM0	The VMEbus address-modifier signals are both inputs and three-state outputs.
$\overline{\text{IACK}}$	The VMEbus interrupt acknowledge signal is both an input and a three-state output.
$\overline{\text{IACK IN}}$	The VMEbus daisy-chained interrupt-acknowledge-in signal is an input.

TABLE III. Pin description - Continued.

Symbol	Name and function
$\overline{\text{IACKOUT}}$	The VMEbus daisy-chained interrupt-acknowledge-out signal is an output.
$\overline{\text{IRQ7}}$ - $\overline{\text{IRQ1}}$	The VMEbus interrupt request signals are both inputs and open collector outputs.
LD7 – LD0	The local data 7 - 0 signals are both inputs and three-state outputs. These signals are typically connected to the local processor data lines D[7:0] through an isolation buffer. Device register accesses are also made through these data signals.
LA7 - LA0	The local address 7 - 0 signals are both inputs and three-state outputs. These signals are typically connected to the local processor address lines. VIC068A registers are also addressed through these signals. When acting as the local bus master, the device drives these lines with the LAEN signal to supply the local address.
$\overline{\text{CS}}$	The device chip select signal is an input. This signal should be asserted whenever access to the device internal registers is required.
$\overline{\text{PAS}}$	The physical/processor address strobe signal is both an input and a rescinding output. This signal is used to qualify an incoming address when performing VMEbus master operations or register operations. This signal is driven when becoming the local bus master and performing slave transfers, DRAM refresh, slave block transfers, and block transfers with local DMA. When acting as an output, the minimum assertion and negation timing for this signal is directed by the Local Bus Timing Register.
$\overline{\text{DS}}$	The local data strobe signal is both an input and a rescinding output. This signal is used to qualify incoming data when performing VMEbus master operations or register operations. This signal is driven when becoming the local bus master and performing slave transfers, DRAM refresh, slave block transfers, and block transfers with local DMA. When acting as an output, the minimum assertion and negation timing for this signal is directed by the Local Bus Timing Register.
$\overline{\text{DSACK1}}$, $\overline{\text{DSACK0}}$	The local data-size-acknowledge signals are both inputs and rescinding outputs. One or both $\overline{\text{DSACK0}}$ of these signals should be asserted to the device whenever the device is local bus master to acknowledge the successful completion of each cycle of a slave transfer, slave block transfer, or block transfers with local DMA. The device asserts one or both of these signals to acknowledge the successful completion of a VMEbus master operation (after receiving the VMEbus $\overline{\text{DTACK}}$ signal. The following should be noted about the $\overline{\text{DSACK1/0}}$ signals: * The device only asserts a 16 bit $\overline{\text{DSACK i}}$ code when the $\overline{\text{WORD}}$ signal is asserted indicating access to a D16 VMEbus resource is complete. * The device treats the assertion of any $\overline{\text{DSACK i}}$ signal as a 32-bit acknowledge for slave accesses. * The device does not directly support 16 or 8-bit local port sizes. * The device always asserts both $\overline{\text{DSACKs}}$ for register accesses, as well as for interrupt acknowledge cycles.
$\overline{\text{LBERR}}$	The local bus-error signal is both an input and a rescinding output. This signal should be asserted to the device whenever the device is local bus master to acknowledge the unsuccessful completion of a cycle of a slave transfer, slave block transfer, and block transfers with local DMA in which case the device asserts the VMEbus $\overline{\text{BERR}}$ signal. The device asserts this signal to acknowedge the unsuccessful completion of a VMEbus master operation (after receiving the VME-bus $\overline{\text{BERR}}$ signal).
$\overline{\text{RESET}}$	The local reset indication signal is an open collector output. This signal is asserted whenever the device is in a reset condition. An internal global, or system reset causes the device to assert $\overline{\text{RESET}}$ for a minimum of 200 ms. If the reset condition continues for longer than 200 ms, $\overline{\text{RESET}}$ begins additional 200 ms timeouts until all reset conditions are cleared.

TABLE III. Pin description - Continued.

Symbol	Name and function
R/$\overline{W}$	The local data direction signal is both an input and a rescinding output. This signal is driven while device is a local bus master to indicate local data direction. As an input, R/$\overline{W}$ indicates data direction for VMEbus master cycles. In this case, $\overline{WRITE}$ reflects the value of R/$\overline{W}$. An asserted condition indicates a write operation.
$\overline{HALT}$	The halt condition indication signal is an input and an open collector output. This signal, $\overline{HALT}$ along with $\overline{RESET}$, is asserted during reset conditions. An internal, global and system reset causes the device to assert $\overline{HALT}$ for a minimum of 200 ms. If the reset condition continues for longer than 200 ms, $\overline{HALT}$ begins an additional 200 ms timeouts until all reset conditions are cleared. Assertion of $\overline{HALT}$ for greater than 4 ms by anything other than the device causes the device to assert $\overline{SYSFAIL}$. $\overline{HALT}$ may be configured to assert during dead-lock conditions along with $\overline{LBERR}$ to initiate a retry sequence for Motorola 68K processors.
SIZ1, SIZ0	The local data size signals are both inputs and rescinding outputs. As inputs, these signals should identify the width of the VMEbus data to be transferred. The SIZi signals should not be used to indicate the physical port size of the slave device (D16 or D32). This is done with the $\overline{WORD}$ signal. As outputs, they are driven by the device as local bus master to identify the width of the incoming data. SIZ1 SIZ0 Data Width 0 0 Long Word 0 1 Byte 1 0 Word 1 1 3-Byte
FC2, FC1	The local function code signals are both inputs and rescinding outputs. These signals identify the type of local cycle in progress. As inputs, they should reflect the type of operations in terms of User/Supervisory Code/Data. They may be connected directly to the Motorola FC2/1 outputs for 68000-30 processors. For the 68040, FC2/1 inputs may be connected to the TM2/1 outputs, respectively. Addition qualification may be required for 68040 applications since the 68040 uses previously reserved/unused function codes. FC2 FC1 Description 0 0 User Data 0 1 User Program 1 0 Supervisory Data 1 1 Supervisory Program As outputs, the device drives these signals whenever local bus master to indicate the type of local bus master to indicate the type of local cycle the device is performing. FC2 FC1 Description 0 0 Slave Block Transfer 0 1 Local DMA 1 0 Slave Access 1 1 DRAM refresh

TABLE III. Pin description - Continued.

Symbol	Name and function
$\overline{LBR}$	The local bus request signal is an output. This signal is asserted whenever the device desires mastership of the local bus. This signal remains asserted for the entire bus tenure. Local bus mastership is requested when each of the following operations is desired: * Standard slave accesses * Slave block transactions * Block transfers with local DMA * DRAM refresh
$\overline{ICFSEL}$	The interprocessor communication facility (ICF) select signal. This signal is used to indicate that the ICF functions of the device have been selected. These include the ICF registers and the ICF switch interrupts. This signal is qualified with $\overline{AS}$ and A16 AM codes (A16/Supervisory for global switches).
$\overline{LBG}$	The local bus grant signal is an input. The signal should be asserted in response to the assertion of the $\overline{LBR}$ signal. The device does not incorporate a local bus grant acknowledge protocol so the $\overline{LBG}$ signal should remain asserted for the duration of $\overline{LBR}$.
$\overline{MWB}$	The module-wants-bus signal. This signal should be asserted by local resources to begin a VMEbus transaction. When qualified by the $\overline{PAS}$ signal, the device asserts the VMEbus $\overline{BRi}$ signal. This signal is usually asserted by local-to-VMEbus address decoders.
$\overline{FCIACK}$	The local interrupt acknowledge signal is an input. This signal should be asserted (qualified by $\overline{PAS}$) to acknowledge all device-generated local interrupts.
$\overline{SLSEL1}$, $\overline{SLSEL0}$	The slave select signals. These signals indicate the device has been selected to perform a $\overline{SLSEL0}$ VMEbus $\overline{SLSEL0}$ slave operation. When qualified by $\overline{AS}$ and valid AM codes, the device requests the local bus to perform the slave cycle. These signals are usually asserted by VMEbus-to- local address decoders. The $\overline{SLSEL1/0}$ signals may be used independently of each other to provide unique slave characteristics as defined by the Slave Select Control registers.
ASIZ1, ASIZ0	The VMEbus address size signals are inputs. These signals should be driven to indicate the ASIZ0 VMEbus address size of master VMEbus transfers. The address size information is issued on the VMEbus AM codes. The assertion of ASIZ0 indicates an A16 transaction. The assertion of ASIZ1 indicates an A32 transaction. Asserting neither indicates an A24 transaction. User-defined address spaces may be accessed by asserting both ASIZ1/0 signals. In this case, the AM codes are issued according to the programming of the Address Modifier Source Register. ASIZ1 / ASIZ0 / Address Size 0 / 0 / User Defined 0 / 1 / A32 1 / 0 / A16 1 / 1 / A24 The ASIZ1/0 signals are also used for cycle acknowledge signals for module-based DMA transfers. During a module-based DMA transfer, the ASIZ0 signal is used as a data-transfer acknowledge signal (analogous to $\overline{DTACK}$). The ASIZ1 signal is used as a bus-error signal (analogous to $\overline{BERR}$).

TABLE III. Pin description - Continued.

Symbol	Name and function
$\overline{\text{WORD}}$	The VMEbus data-width control signal is an input. This signal, when asserted indicates the requested VMEbus transaction should be treated as a D16 data path. When negated, the VMEbus data path is assumed to be D32. This signal should be used to configure VMEbus data-width for master cycles only. Data-width for slave cycles is configured in the Slave Select Control Registers. This signal is also used to configure the data-width for block transfers with local DMA. When this signal is asserted during the block transfer initiation cycle, the block transfer is assumed to be a D16 block transfer. This signal may be changed dynamically for individual transfers, or strapped LOW at power-up for permanent D16 operation. If $\overline{\text{WORD}}$ is strapped LOW at power-up, the device is configured as a D16 slave independent of the slave configuration in the Slave Select Control Registers. $\overline{\text{WORD}}$ should not be used to indicate data size (i.e., byte, word, or long-word) only local data port size (i.e., D16 or D32).
$\overline{\text{LIRQ7}}$ - $\overline{\text{LIRQ1}}$	The local interrupt request signals are inputs with $\overline{\text{LIRQ2}}$ also available as an output. These $\overline{\text{LIRQi}}$ signals serve as local interrupt request signals for the device. If enabled to handle the particular local interrupt, the device in turn issues a processor interrupt with the $\overline{\text{IPLi}}$ signals at the assertion of a $\overline{\text{LIRQi}}$. Extensive configuration of local interrupts is allowed through the Local Interrupt Configuration Registers. $\overline{\text{LIRQ2}}$ may also be configured to issue periodic interrupts at user defined intervals.
$\overline{\text{IPL2}}$, $\overline{\text{IPL1}}$, $\overline{\text{IPL0}}$	The local priority encoded interrupt request signals are outputs with $\overline{\text{IPL0}}$ also available as an input. These signals are asserted to interrupt the local processor. All local device interrupts are issued with these signals. These signals are meant to emulate the Motorola 68K interrupt algorithms. The assertion of one or more of these signals indicate a single interrupt with a priority given by the negative-logic value of the $\overline{\text{IPLi}}$ signals. Level 7 is the highest priority. These signals are open-collector to allow the wire-O Ring of multiple interrupt sources. During the assertion of $\overline{\text{IRESET}}$, $\overline{\text{IPL0}}$ becomes an input . If I $\overline{\text{IPL0}}$ is asserted at this time, a global reset is performed.
$\overline{\text{LIACKO}}$	The autovectoring indication signal is an input. This signal is asserted when the device is configured to allow the interrupting device to place its status/ID vector on the local data bus in response to a device-handled local interrupt acknowledge. This signal may be used to signal a autovectored interrupt acknowledge cycle for 68020/30/40 processors. This signal may be connected directly to the AVEC signal for these processors.
$\overline{\text{IRESET}}$	The Internal reset signal is an input. This signal is used to issue both internal and global resets to the device. If asserted with $\overline{\text{IPL0}}$, a global reset is performed. If asserted without $\overline{\text{IPL0}}$, an internal reset is performed. All internal state machines and selected register bits are rese during the assertion of $\overline{\text{IRESET}}$. $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ are both asserted during the assertion of $\overline{\text{IRESET}}$. If configured as system controller, $\overline{\text{SYSRESET}}$ is also asserted during the assertion of $\overline{\text{IRESET}}$. $\overline{\text{IRESET}}$ contains internal hysteresis to allow the connection of this signal to an external RC network for power-up resets.
$\overline{\text{SCON}}$	The system controller enabling signal is an input. This signal is used to configure the device as VMEbus system controller. This signal must be strapped Iow at power-up and remain LOW for device to reliably assume the role of VMEbus system controller.

TABLE III. Pin description - Continued.

Symbol	Name and function
$\overline{BLT}$	The block transfer with local DMA indication signal is both an input and an open-collector output. This signal is used to indicate that a block transfer with local DMA is in progress. This signal remains asserted for the entire block transfer including interleave periods with the exception of local page boundary crossings. $\overline{BLT}$ toggles during local boundary crossings to increment the external LA(+:8) counters. The $\overline{BLT}$ signal is asserted simultaneously with the $\overline{MWB}$ signal and BTCR signal is asserted simultaneously with the $\overline{MWB}$ signal and BTCR[7] is set, a module-based DMA transfer is performed.
$\overline{DEDLK}$	The dead-lock indication signal is an output. This signal is used to indicate a dead-lock condition has occured. This signal should be used by local logic to remove its request for the VMEbus. $\overline{DEDLK}$ remains asserted until the slave transaction is complete. $\overline{DEDLK}$ is also asserted to indicate that a VMEbus master cycle is being attempted during the interleave period of a block transfer with local DMA, without the dual path feature enabled. In this case, $\overline{DEDLK}$ is asserted while $\overline{MWB}$ signal is asserted. If, during the interleave period, the $\overline{MWB}$ signal is asserted after the VMEbus has been re-obtained, the device will assert $\overline{DEDLK}$ for the duration of the burst.
CLK64M	The device master clock is an input. This 64-MHz clock input is used to clock internal arbitration, timing, and delay functions within the device.
$\overline{ABEN}$	The VMEbus address bus enable signal is an output. This signal is used to enable the external VMEbus address drivers for VMEbus master operations. It is typically connected to the QEAB input of a '543 address transceiver.
LAEN	The local address enable signal is an input. This signal is used to enable the external local address drivers for slave accesses. It is typically connected to the OEBA input of a '543 address transceivers through an inverter. This signal is an active HIGH signal.
LADO	The latch address out signal is an output. This signal is used to latch the outgoing VMEbus address for VMEbus master operations. When this signal is asserted (HIGH), it is assumed that the latches are in a latched state. When negated, the latches should be in a fall-through state. This allows direct connection to the '543 address driver LEAB input. LADO is very important for proper operation of master write posting and block transfers with interleave periods. For these operations, device may use LADO in combination with LADI and $\overline{ABEN}$ to temporarily store the contents of a VMEbus address during intervening slave accesses.
LADI	The latch address in signal is an input. This signal is used to latch the incoming VMEbus address for slave accesses. When this signal is asserted (HIGH), it is assumed that the latches should be in a latched state. When negated, the latches should be in a fall-through state. This allows direct connection to the '543 address driver LEAB input. LADI is used in conjunction with LADO to temporarily store outgoing VMEbus master transaction addresses during intervening slave accesses.

TABLE III. Pin description - Continued.

Symbol	Name and function
$\overline{\text{LWDENIN}}$	The lower word data enable in signal is an output. This signal enables data onto the lower word of the local data bus LD[15:8] for master read and slave write cycles. This signal is typically connected to the OEBA input of the '543 lower data latch.
$\overline{\text{UWDENIN}}$	The upper word data enable in signal is an output. This signal enables data onto the upper word of the local data bus LD[31:16] for master read and slave write cycles. This signal is typically connected to the OEBA input of the upper '543 data latches.
LEDO	The latch data out signal is an output. This signal latches the outgoing VMEbus data for master write slave read cycles. When this signal is asserted (HIGH), it is assumed that the latches are in a latched state. When negated, the latches should be in a fall-through state. This allows direct connection to the '543 address driver LEAB input. This signal is used in conjunction with LEDI to temporarily store outgoing master write post data (data switch-back).
LEDI	The latch data in signal is an output. This signal latches the incoming VMEbus data for master read slave write cycles. When this signal is asserted (HIGH), it is assumed that the latches are in a latched state. When negated, the latches should be in a fall-through state. This allows direct connection to the '543 address driver LEBA input. This signal is used in conjunction with LEDO to temporarily store outgoing master write post data.
$\overline{\text{ISOBE}}$	The isolation buffer enable signal. This signal, along with the $\overline{\text{SWDEN}}$ signal, provides byte lane switching. This signal is typically connected to the EN input of the '245 isolation buffer.
$\overline{\text{SWDEN}}$	The swap data enable signal is an output. This signal, along with the $\overline{\text{ISOBE}}$ signal, provides byte lane switching. It provides for swapping LD[31:16] to LD[15:0]. This signal is typically connected to the EN input of the '245 swap buffer.
DDIR	The data direction signal is an output. This signal provides the data direction (i.e., read/write) information to the isolation and swap buffers. When asserted, buffers should be configured in the local-to-VME-bus (A-to-B) direction. This signal is typically connected to the DIR input of the ‘245 isolation swap buffers.
$\overline{\text{RMC}}$	This is the read-modify-write control signal. This signal may be used to control indivisible cycles on the VMEbus. Its operation is controlled with the interface configuration register, bits 5-7
$\overline{\text{DENO}}$	The Data Enable Out signal is an output. This signal enables data onto the VMEbus data bus for Master Write and Slave Read cycles. The signal is typically connected to the OAEB input of the ‘543 data latches.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-02-23

Approved sources of supply for SMD 5962-92010 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9201001MXC	65786	VIC068A-GMB
5962-9201001MYC	65786	VIC068A-UMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65786	Cypress Semiconductor 3901 North First Street San Jose, CA 95134

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.