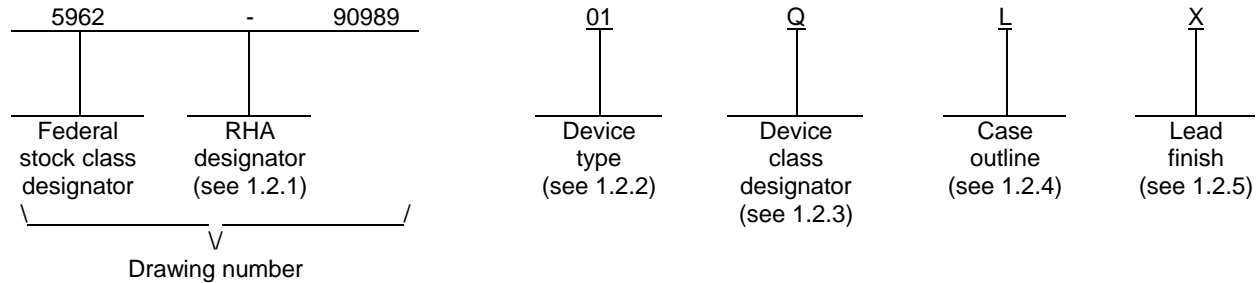


REVISIONS																				
LTR	DESCRIPTION													DATE (YR-MO-DA)	APPROVED					
A	Boilerplate update and part of five year review. Add QP Semiconductor as an approved source of supply. tr													06-06-20	Raymond Monnin					
REV																				
SHEET																				
REV	A	A	A	A																
SHEET	15	16	17	18																
REV STATUS OF SHEETS				REV SHEET	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
					1	2	3	4	5	6	7	8	9	10	11	12	13	14		
PMIC N/A				PREPARED BY Raj Pithadia					<p align="center"><b>DEFENSE SUPPLY CENTER COLUMBUS</b>  <b>COLUMBUS, OHIO 43218-3990</b>  <a href="http://www.dsc.dla.mil">http://www.dsc.dla.mil</a></p> <p>MICROCIRCUIT, MEMORY, DIGITAL, CMOS            UV ERASABLE PROGRAMMABLE LOGIC ARRAY,            MONOLITHIC SILICON</p>											
<b>STANDARD MICROCIRCUIT DRAWING</b>				CHECKED BY Sandra Rooney																
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE  AMSC N/A				APPROVED BY Michael Frye																
				DRAWING APPROVAL DATE 94-03-01																
				REVISION LEVEL A					SIZE A	CAGE CODE 67268	<b>5962-90989</b>									
									SHEET 1 OF 17											

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number 1/</u>	<u>Circuit function</u>	<u>t<sub>PD</sub></u>
01	PLDC20RA10-35	Asynchronous EPLD	35 ns
02	PLDC20RA10-25	Asynchronous EPLD	25 ns
03	PLDC20RA10-20	Asynchronous EPLD	20 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line 2/
3	CQCC1-N28	28	Square leadless chip carrier 2/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Generic numbers are also listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103 and QML-38535 (see 6.6.2 herein).

2/ Lid shall be transparent to permit ultraviolet light erasure.

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1.3 Absolute maximum ratings. <sup>3/</sup>

Supply voltage to ground potential .....	-0.5 V dc to +7.0 V dc
DC voltage range applied to outputs in high-Z state .....	-0.5 V dc to +7.0 V dc
DC input voltage .....	-3.0 V dc to +7.0 V dc
Maximum power dissipation (P <sub>D</sub> ) <sup>4/</sup> .....	1.0 W
Lead temperature (soldering, 10 seconds).....	+260°C
Thermal resistance, junction-to-case (θ <sub>JC</sub> ) .....	See MIL-STD-1835
Junction temperature (T <sub>J</sub> ).....	+175°C
Storage temperature range .....	-65°C to +150°C
Temperature under bias .....	-55°C to +125°C
Output current into outputs (low) .....	-16 mA
Data retention .....	10 years (minimum)
Endurance.....	25 erase/write cycles (minimum)

1.4 Recommended operating conditions.

Supply voltage (V <sub>CC</sub> ) .....	+4.5 V dc to +5.5 V dc
Ground voltage (GND) .....	0 V dc
Input high voltage (V <sub>IH</sub> ).....	2.2 V dc minimum
Input low voltage (V <sub>IL</sub> ) .....	0.8 V dc maximum
Case operating temperature range (T <sub>C</sub> ).....	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-00                      Standard Guide for the Measurement of Single Event Phenomena (SEP)  
 Induced by Heavy Ion Irradiation of Semiconductor Devices

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; <http://www.astm.org>.)

<sup>3/</sup> Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

<sup>4/</sup> Must withstand the added P<sub>D</sub> due to short circuit test; e.g., I<sub>OS</sub>.

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ELECTRONICS INDUSTRIES ALLIANCE (EIA)

JEDEC Standard EIA/JESD 78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201; <http://www.jedec.org>.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in screening (see 4.2 herein) or qualification conformance inspection, groups A, C, D, or E (see 4.4), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at least 25 percent of the total number of cells to any altered item drawing.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.2.4 Radiation exposure circuit. The radiation exposure circuit will be provided when RHA product becomes available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

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3.6 Processing EPLDS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.6.1 Erasure of EPLDS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.6.

3.6.2 Programmability of EPLDS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.7.

3.6.3 Verification of erasure or programmed EPLDS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.7 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract.

3.7.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.7.2 Manufacturer programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.8 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.9 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.10 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.11 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.12 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.13 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitor. This reprogrammability test shall be done only for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but will guarantee the number of program/erase endurance cycles listed in section 1.3 herein. The vendors procedure shall be under document control and shall be made available upon request.

3.14 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.
- b. Prior to burn-in, the devices shall be programmed (see 4.7 herein) with a checkerboard pattern or equivalent (manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern). The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be included in the Percent Defective Allowable (PDA) calculation and shall be removed from the lot. The manufacturer as an option may use built-in test circuitry by testing the entire lot to verify programmability and AC performance without programming the user array.
- c. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

- d. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output high voltage	V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -2.0 mA, V <sub>IN</sub> = V <sub>IH</sub> , V <sub>IL</sub>	1, 2, 3	All	2.4		V
Output low voltage	V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 8.0 mA, V <sub>IN</sub> = V <sub>IH</sub> , V <sub>IL</sub>	1, 2, 3	All		0.5	V
Input high voltage <u>1/</u>	V <sub>IH</sub>		1, 2, 3	All	2.0		V
Input low voltage <u>1/</u>	V <sub>IL</sub>		1, 2, 3	All		0.8	V
Input leakage current	I <sub>IX</sub>	V <sub>IN</sub> = 5.5 V to GND	1, 2, 3	All	-10	10	μA
Output leakage current	I <sub>OZ</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 5.5 V and GND	1, 2, 3	All	-40	40	μA
Output short circuit Current <u>2/ 3/</u>	I <sub>OS</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0.5 V	1, 2, 3	All	-30	-90	mA
Standby power supply current	I <sub>CC1</sub>	V <sub>CC</sub> = 5.5 V, I <sub>OUT</sub> = 0 mA, V <sub>IN</sub> = GND	1, 2, 3	All		80	mA
Power supply current at frequency <u>3/</u>	I <sub>CC2</sub>	V <sub>CC</sub> = 5.5 V, I <sub>OUT</sub> = 0 mA, V <sub>IN</sub> = 0 to 3 V, f = f <sub>MAX</sub>	1, 2, 3	All		85	mA
Input capacitance <u>3/</u>	C <sub>IN</sub>	V <sub>CC</sub> = 5.0 V T <sub>A</sub> = +25°C, f = 1 MHz	4	All		10	pF
Output capacitance <u>3/</u>	C <sub>OUT</sub>	(see 4.4.1e)	4	All		10	pF
Functional tests		See 4.4.1c	7, 8A, 8B	All			
Input or feedback to nonregistered output <u>4/</u>	t <sub>PD</sub>		9, 10, 11	01		35	ns
				02		25	
				03		20	
Input to output enable <u>3/ 5/</u>	t <sub>EA</sub>		9, 10, 11	01		35	ns
				02		30	
				03		20	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input to output disable <u>3/ 5/</u>	t <sub>ER</sub>		9, 10, 11	01		35	ns
				02		30	
				03		20	
$\overline{\text{OE}}$ to output enable <u>5/</u>	t <sub>PZX</sub>		9, 10, 11	01		25	ns
				02		20	
				03		15	
$\overline{\text{OE}}$ to output disable <u>3/ 5/</u>	t <sub>PXZ</sub>		9, 10, 11	01		25	ns
				02		20	
				03		15	
Clock to output <u>4/</u>	t <sub>CO</sub>		9, 10, 11	01		35	ns
				02		25	
				03		20	
Input or feedback setup time <u>4/</u>	t <sub>SU</sub>		9, 10, 11	01	20		ns
				02	15		
				03	10		
Hold time <u>4/</u>	t <sub>H</sub>		9, 10, 11	01, 02	5		ns
				03	3		
Clock period (t <sub>SU</sub> + t <sub>CO</sub> ) <u>4/</u>	t <sub>P</sub>		9, 10, 11	01	55		ns
				02	40		
				03	30		
Clock width high <u>3/ 4/</u>	t <sub>WH</sub>		9, 10, 11	01	25		ns
				02	18		
				03	12		
Clock width low <u>3/ 4/</u>	t <sub>WL</sub>		9, 10, 11	01	25		ns
				02	18		
				03	12		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Maximum frequency (1/(t <sub>p</sub> )) <u>3/ 4/</u>	f <sub>MAX</sub>		9, 10, 11	01	18.1		MHz
				02	25.0		
				03	33.3		
Input of asynchronous set to registered output <u>3/ 4/</u>	t <sub>S</sub>		9, 10, 11	01		40	ns
				02		25	
				03		20	
Input of asynchronous reset to registered output <u>3/ 4/</u>	t <sub>R</sub>		9, 10, 11	01		40	ns
				02		25	
				03		20	
Asynchronous reset width <u>3/ 4/</u>	t <sub>ARW</sub>		9, 10, 11	01, 02	25		ns
				03	20		
Asynchronous set width <u>3/ 4/</u>	t <sub>ASW</sub>		9, 10, 11	01, 02	25		ns
				03	20		
Asynchronous set/reset recovery time <u>3/ 4/</u>	t <sub>AR</sub>		9, 10, 11	01	20		ns
				02	15		
				03	12		
Preload pulse width <u>3/ 4/</u>	t <sub>WP</sub>		9, 10, 11	All	15		ns
Preload setup time <u>3/ 4/</u>	t <sub>SUP</sub>		9, 10, 11	All	15		ns
Preload hold time <u>3/ 4/</u>	t <sub>HP</sub>		9, 10, 11	All	15		ns

1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

2/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 1 second. V<sub>OUT</sub> = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

3/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

4/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load on figure 3, circuit A. See figure 4 for waveforms.

5/ Measured using the test load on figure 3, circuit B. See figure 4 for waveforms.

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Device types	01 through 03	
Case outlines	L	3
Terminal number	Terminal symbol	
1	$\overline{PL}$	$\overline{PL}$
2	$I_0$	$I_0$
3	$I_1$	$I_1$
4	$I_2$	NC
5	$I_3$	$I_2$
6	$I_4$	$I_3$
7	$I_5$	$I_4$
8	$I_6$	$I_5$
9	$I_7$	$I_6$
10	$I_8$	$I_7$
11	$I_9$	NC
12	GND	$I_8$
13	$\overline{OE}$	$I_9$
14	$I/O_9$	GND
15	$I/O_8$	$\overline{OE}$
16	$I/O_7$	$I/O_9$
17	$I/O_6$	$I/O_8$
18	$I/O_5$	NC
19	$I/O_4$	$I/O_7$
20	$I/O_3$	$I/O_6$
21	$I/O_2$	$I/O_5$
22	$I/O_1$	$I/O_4$
23	$I/O_0$	$I/O_3$
24	$V_{CC}$	$I/O_2$
25	----	NC
26	----	$I/O_1$
27	----	$I/O_0$
28	----	$V_{CC}$

FIGURE 1. Terminal connections.

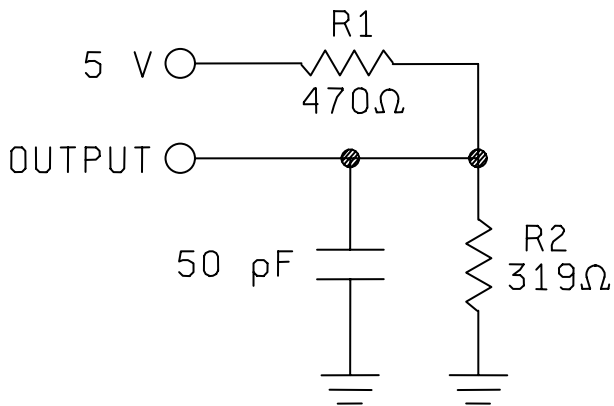
<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-90989</b>
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Truth Table			
Input pins			Output pins
$\overline{OE}$	$\overline{PL}$	I	O
X	X	X	Z

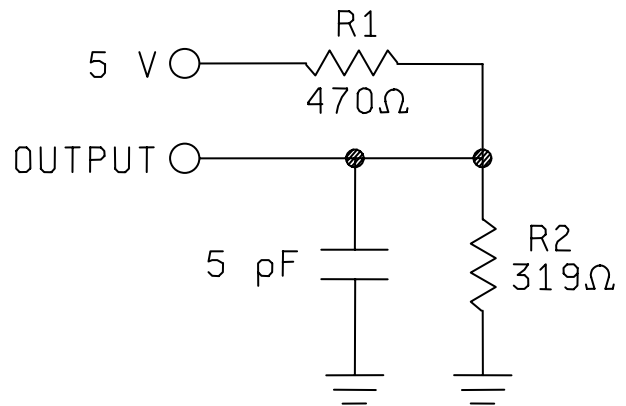
Notes:

1. Z = High impedance
2. X = Don't care

FIGURE 2. Truth table (unprogrammed).



CIRCUIT A  
OUTPUT LOAD



CIRCUIT B  
OUTPUT LOAD

\* Including scope and jig (minimum values)

FIGURE 3. Output load circuit and test conditions.

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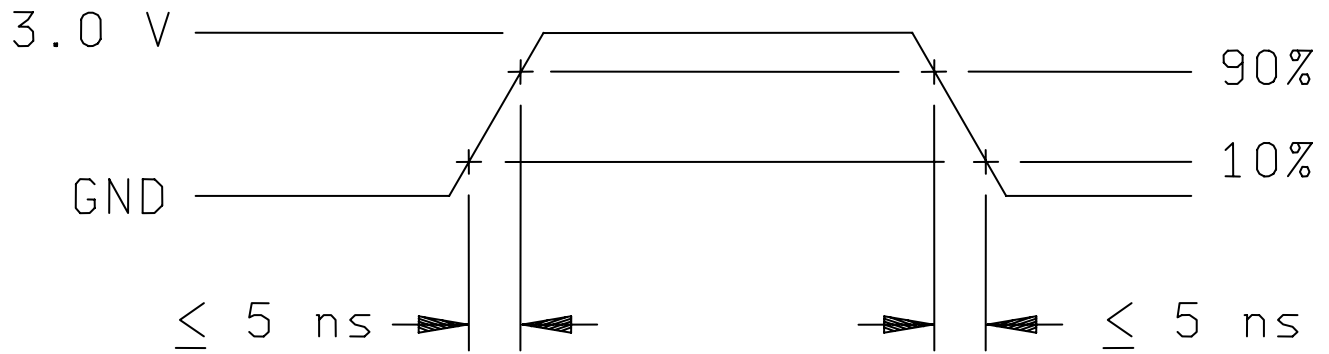
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## INPUT PULSES



### AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times	$\le 5\text{ ns}$
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 3. Output load circuit and test conditions (continued).

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Output control switching waveform

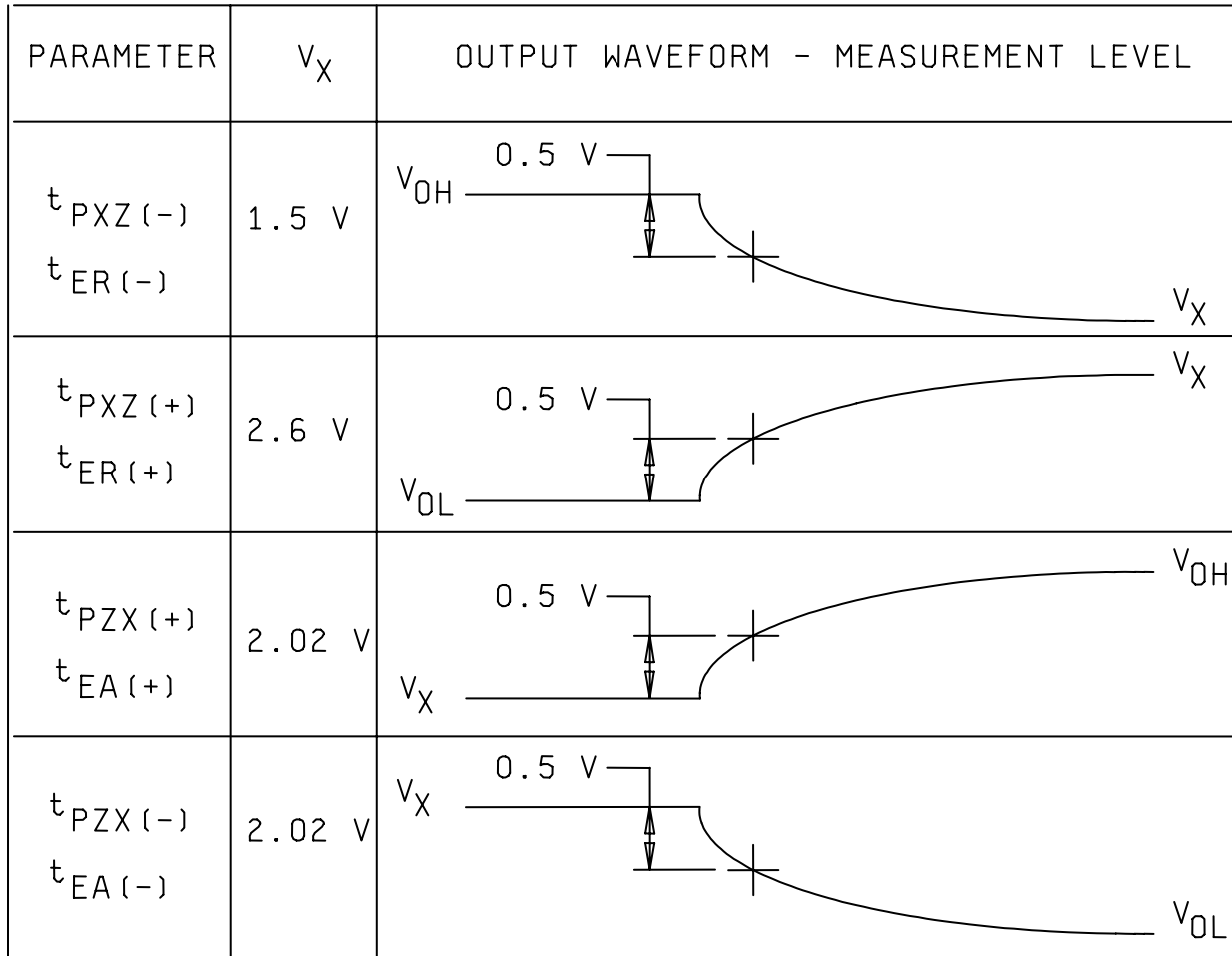


FIGURE 4. Switching waveform.

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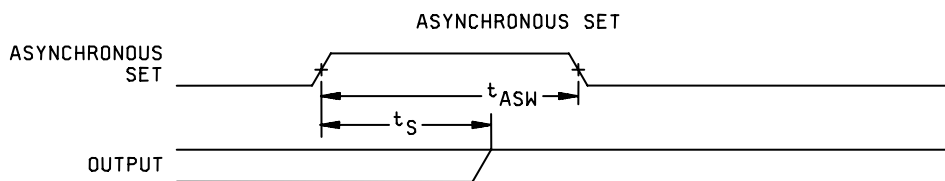
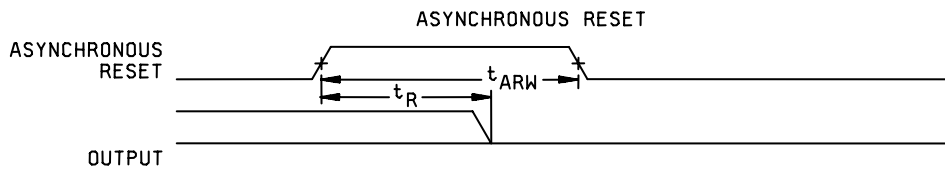
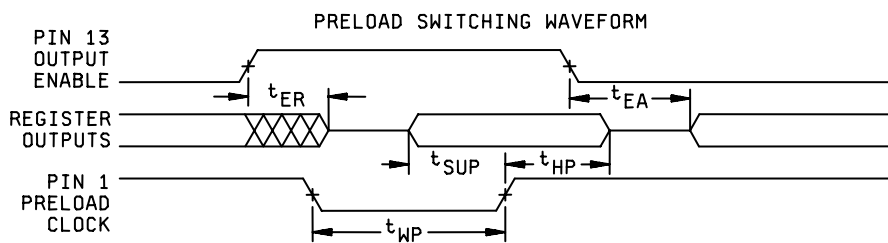
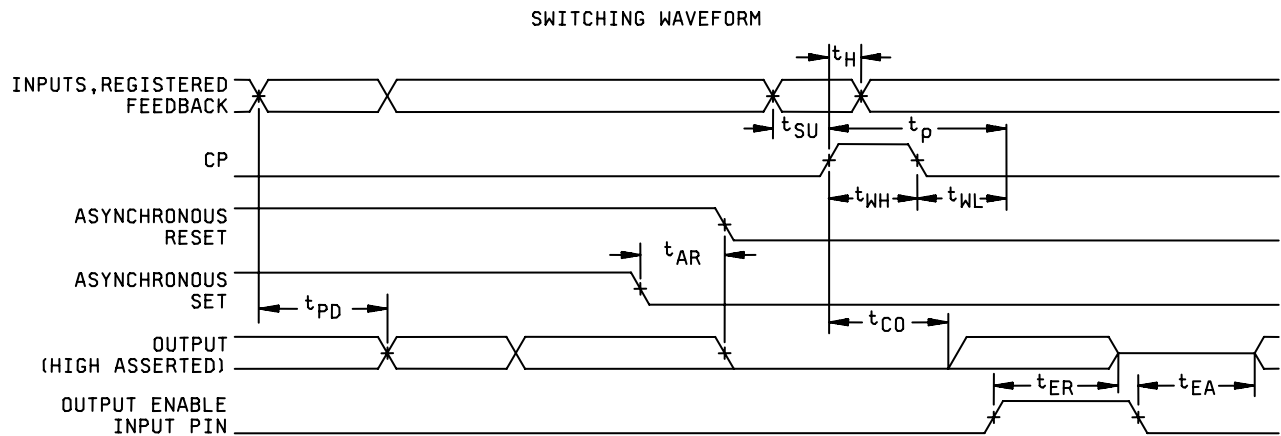


FIGURE 4. Switching waveform - continued.

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4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 ( $C_{IN}$  and  $C_{OUT}$  measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.
- d. For device class M, subgroups 7, 8A, and 8B tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- e. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD 78 may be used for reference.
- f. Devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:
  - (1) Testing all devices submitted for test using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.
  - (2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.3.1). If any device fails to program, the lot shall be rejected. At the manufacturers option, the sample may be increased to 24 total devices with no more than one total device failure allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If any device fails, the lot shall be rejected. At the manufacturers option, the sample may be increased to 20 total devices with no more than one total device failure allowable. After completion of all testing, the devices shall be erased and verified except devices submitted to groups C and D testing.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply to group C inspection and shall consist of tests specified in table IIB herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b.  $T_A = +125^{\circ}\text{C}$ , minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (per MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9	1, 7, 9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B Δ	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters	1, 7, 9	1, 7, 9	1, 7, 9

- 1/ Blank spaces indicate tests are not applicable.
- 2/ Any or all subgroups may be combined when using high-speed testers.
- 3/ Subgroups 7 and 8 functional tests shall verify the truth table.
- 4/ \* indicates PDA applies to subgroup 1 and 7.
- 5/ \*\* see 4.4.1c.
- 6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
- 7/ See 4.4.1e.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	All device types
I <sub>cc1</sub> Standby	±1% of specified limit in table I
I <sub>IX</sub> , I <sub>OZ</sub>	±1% of specified limit in table I

- 1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

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4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ , after exposure, to the subgroups specified in table IIA herein.

4.5 Delta measurements for device classes Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Erasing procedure. The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2,537 Angstroms (Å). The integrated dose (i.e., ultraviolet intensity times exposure time) for erasure should be minimum of 15 Ws/cm<sup>2</sup>. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 μW/cm<sup>2</sup> power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7,258 Ws/cm<sup>2</sup> (1 week at 12,000 μW/cm<sup>2</sup>). Exposure of the device to high intensity ultraviolet light for long periods may cause permanent damage.

4.7 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

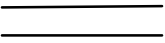

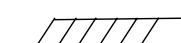

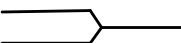
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6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

- C<sub>IN</sub>, C<sub>OUT</sub> ..... Input and bidirectional output, terminal-to-GND capacitance
- GND ..... Ground zero voltage potential.
- I<sub>CC</sub> ..... Supply current
- T<sub>C</sub> ..... Case temperature
- T<sub>A</sub> ..... Ambient temperature
- V<sub>CC</sub> ..... Positive supply voltage

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. For example, address setup time would be shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. For example, the access time would be shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.8 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.8 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-06-20

Approved sources of supply for SMD 5962-90989 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9098901M3A	0C7V7	PLDC20RA10-35QMB
5962-9098901MLA	0C7V7	PLDC20RA10-35WMB
5962-9098902M3A	0C7V7	PLDC20RA10-25QMB
5962-9098902MLA	0C7V7	PLDC20RA10-25WMB
5962-9098903M3A	0C7V7	PLDC20RA10-20QMB
5962-9098903MLA	0C7V7	PLDC20RA10-20WMB

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE  
number

0C7V7

Vendor name  
and address

QP Semiconductor  
2945 Oakmead Village Court  
Santa Clara, CA 95051 - 0812

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