

Features

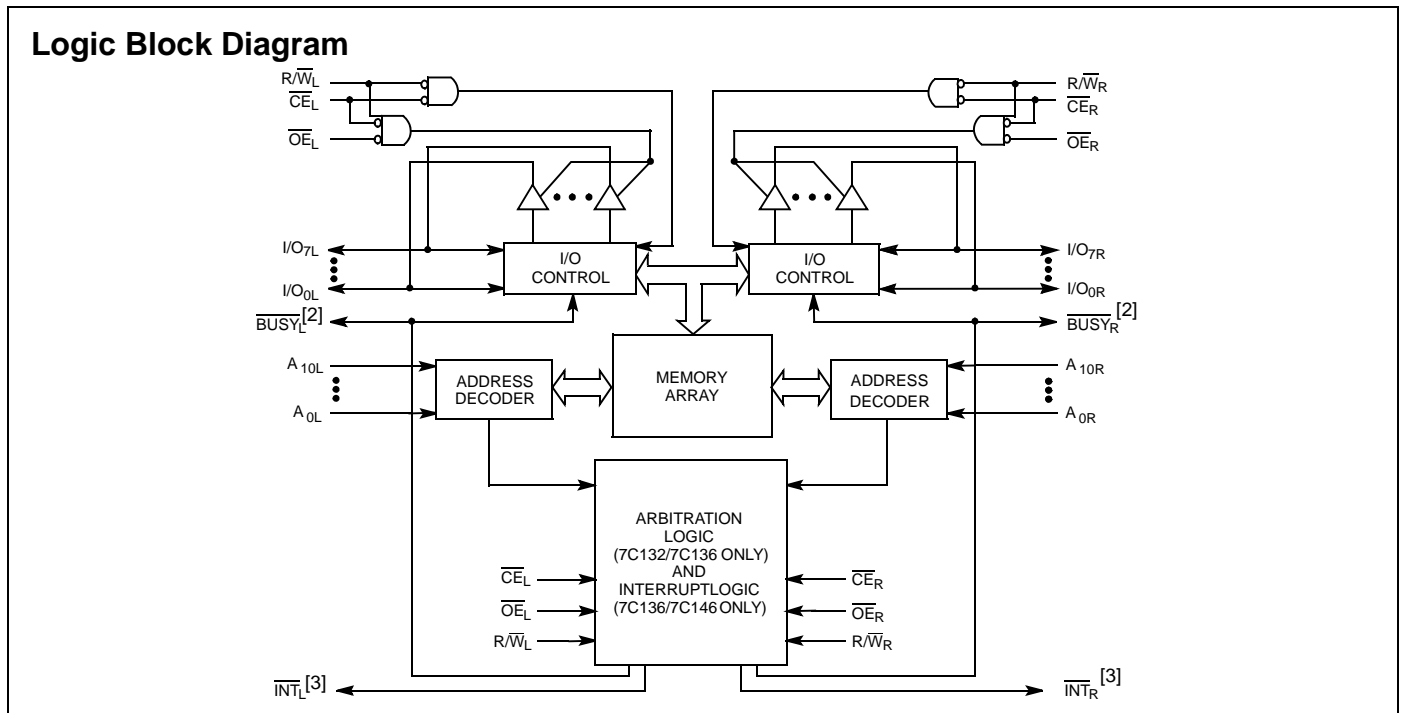
- True dual-ported memory cells that enable simultaneous reads of the same memory location
- 2K x 8 organization
- 0.65 micron CMOS for optimum speed and power
- High speed access: 15 ns
- Low operating power: $I_{CC} = 110 \text{ mA}$ (maximum)
- Fully asynchronous operation
- Automatic power down
- Master CY7C132/CY7C136/CY7C136A^[1] easily expands data bus width to 16 or more bits using slave CY7C142/CY7C146
- $\overline{\text{BUSY}}$ output flag on CY7C132/CY7C136/CY7C136A; $\overline{\text{BUSY}}$ input on CY7C142/CY7C146
- $\overline{\text{INT}}$ flag for port to port communication (52-Pin PLCC/PQFP versions)
- CY7C136, CY7C136A, and CY7C146 available in 52-pin PLCC and 52-pin PQFP packages
- Pb-free packages available

Functional Description

The CY7C132, CY7C136, CY7C136A, CY7C142, and CY7C146 are high speed CMOS 2K x 8 dual-port static RAMs. Two ports are provided to permit independent access to any location in memory. The CY7C132, CY7C136, and CY7C136A can be used as either a standalone 8-bit dual-port static RAM or as a MASTER dual-port RAM, in conjunction with the CY7C142/CY7C146 SLAVE dual-port device. They are used in systems that require 16-bit or greater word widths. This is the solution to applications that require shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ($\overline{\text{CE}}$), write enable (R/W), and output enable (OE). $\overline{\text{BUSY}}$ flags are provided on each port. In addition, an interrupt flag ($\overline{\text{INT}}$) is provided on each port of the 52-pin PLCC version. $\overline{\text{BUSY}}$ signals that the port is trying to access the same location currently being accessed by the other port. On the PLCC version, $\overline{\text{INT}}$ is an interrupt flag indicating that data is placed in a unique location (7FF for the left port and 7FE for the right port).

An automatic power down feature is controlled independently on each port by the chip enable ($\overline{\text{CE}}$) pins.



Notes

1. CY7C136 and CY7C136A are functionally identical.
2. CY7C132/CY7C136/CY7C136A (Master): $\overline{\text{BUSY}}$ is open drain output and requires pull up resistor. CY7C142/CY7C146 (Slave): $\overline{\text{BUSY}}$ is input.
3. Open drain outputs; pull up resistor required.

Pinouts

Figure 1. 52-Pin PLCC (Top View)

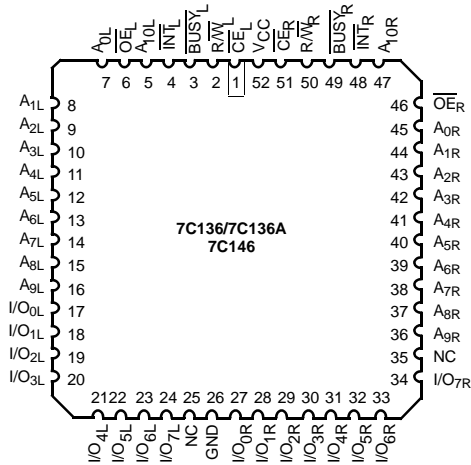
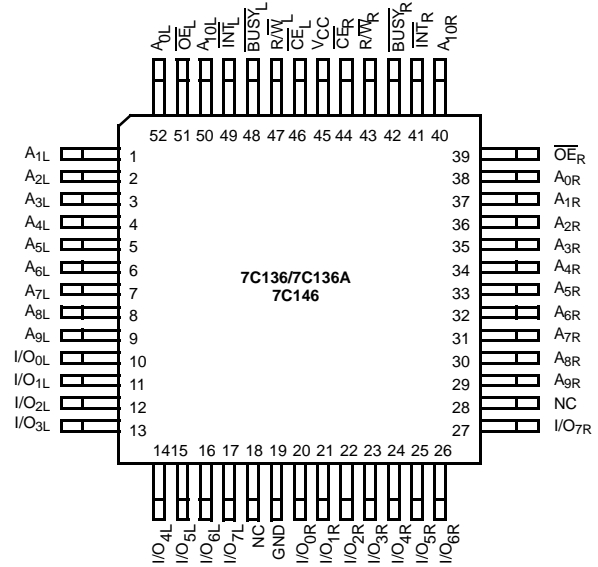


Figure 2. 52-Pin PQFP (Top View)



Selection Guide

| Specification | 7C136-15 ^[4] 7C146-15 | 7C132-25 ^[4] 7C136-25 7C142-25 7C146-25 | 7C132-30 7C136-30 7C142-30 7C146-30 | 7C132-35 7C136-35 7C142-35 7C146-35 | 7C132-45 7C136-45 7C142-45 7C146-45 | 7C132-55 7C136-55 7C136A-55 7C142-55 7C146-55 | Unit |
|---------------------------|-------------------------------------|---|--|--|--|---|------|
| Maximum Access Time | 15 | 25 | 30 | 35 | 45 | 55 | ns |
| Maximum Operating Current | Com'I/Ind | 190 | 170 | 120 | 120 | 110 | mA |
| Maximum Standby Current | Com'I/Ind | 75 | 65 | 65 | 45 | 35 | mA |

Shaded areas contain preliminary information.

Note:

4. 15 ns and 25 ns version available in PQFP and PLCC packages only.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65°C to +150°C
 Ambient Temperature with
 Power Applied..... -55°C to +125°C
 Supply Voltage to Ground Potential
 (Pin 48 to Pin 24)..... -0.5V to +7.0V
 DC Voltage Applied to Outputs
 in High Z State -0.5V to +7.0V

DC Input Voltage -3.5V to +7.0V
 Output Current into Outputs (LOW)..... 20 mA
 Static Discharge Voltage..... > 2001V
 (per MIL-STD-883, Method 3015)
 Latch up Current..... > 200 mA

Operating Range

| Range | Ambient Temperature | V _{CC} |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C | 5V ± 10% |
| Industrial | -40°C to +85°C | 5V ± 10% |

Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | 7C136-15 ^[4] 7C146-15 | | 7C132-30 ^[4] 7C136-25, 30 7C142-30 7C146-25, 30 | | 7C132-35,45 7C136-35,45 7C142-35,45 7C146-35,45 | | 7C132-55 7C136-55 7C136A-55 7C142-55 7C146-55 | | Unit |
|------------------|---|---|-------------------------------------|------|---|------|--|------|---|------|------|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| V _{OH} | Output HIGH voltage | V _{CC} = Min., I _{OH} = -4.0 mA | 2.4 | | 2.4 | | 2.4 | | 2.4 | | V |
| V _{OL} | Output LOW voltage | I _{OL} = 4.0 mA | | 0.4 | | 0.4 | | 0.4 | | 0.4 | V |
| | | I _{OL} = 16.0 mA ^[5] | | 0.5 | | 0.5 | | 0.5 | | 0.5 | V |
| V _{IH} | Input HIGH voltage | | 2.2 | | 2.2 | | 2.2 | | 2.2 | | V |
| V _{IL} | Input LOW voltage | | | 0.8 | | 0.8 | | 0.8 | | 0.8 | V |
| I _{IX} | Input load current | GND ≤ V _I ≤ V _{CC} | -5 | +5 | -5 | +5 | -5 | +5 | -5 | +5 | μA |
| I _{OZ} | Output leakage current | GND ≤ V _O ≤ V _{CC} , Output Disabled | -5 | +5 | -5 | +5 | -5 | +5 | -5 | +5 | μA |
| I _{OS} | Output short circuit current ^[6] | V _{CC} = Max., V _{OUT} = GND | | -350 | | -350 | | -350 | | -350 | mA |
| I _{CC} | V _{CC} Operating Supply Current | $\overline{CE} = V_{IL}$, Outputs Open, f = f _{MAX} ^[7] | | 190 | | 170 | | 120 | | 110 | mA |
| I _{SB1} | Standby current both ports, TTL Inputs | \overline{CE}_L and $\overline{CE}_R \geq V_{IH}$, f = f _{MAX} ^[7] | | 75 | | 65 | | 45 | | 35 | mA |
| I _{SB2} | Standby Current One Port, TTL Inputs | \overline{CE}_L or $\overline{CE}_R \geq V_{IH}$, Active Port Outputs Open, f = f _{MAX} ^[7] | | 135 | | 115 | | 90 | | 75 | mA |
| I _{SB3} | Standby Current Both Ports, CMOS Inputs | Both Ports \overline{CE}_L and $\overline{CE}_R \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0 | | 15 | | 15 | | 15 | | 15 | mA |
| I _{SB4} | Standby Current One Port, CMOS Inputs | One Port \overline{CE}_L or $\overline{CE}_R > V_{CC} - 0.2V$, V _{IN} > V _{CC} - 0.2V or V _{IN} < 0.2V, Active Port Outputs Open, f = f _{MAX} ^[7] | | 125 | | 105 | | 85 | | 70 | mA |

Shaded areas contain preliminary information.

Notes

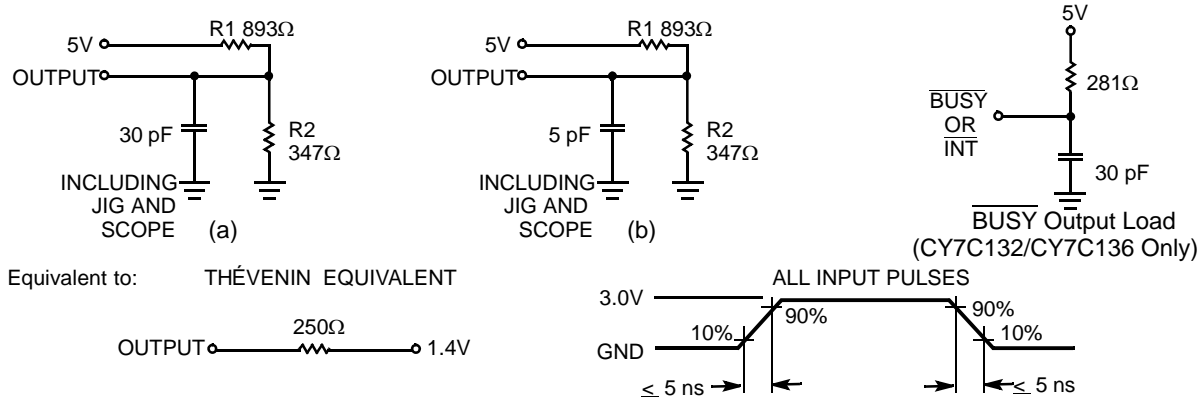
- BUSY and INT pins only.
- Duration of the short circuit should not exceed 30 seconds.
- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of 1/t_{rc} and using AC Test Waveforms input levels of GND to 3V.

Capacitance

This parameter is guaranteed but not tested.

| Parameter | Description | Test Conditions | Max | Unit |
|------------------|--------------------|--|-----|------|
| C _{IN} | Input Capacitance | T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V | 15 | pF |
| C _{OUT} | Output Capacitance | | 10 | pF |

Figure 3. AC Test Loads and Waveforms



Switching Characteristics

Over the Operating Range (Speeds -15, -25, -30) [8]

| Parameter | Description | 7C136-15 [4] 7C146-15 | | 7C132-25 [4] 7C136-25 7C142-25 7C146-25 | | 7C132-30 7C136-30 7C142-30 7C146-30 | | Unit |
|-------------------|--|--------------------------|-----|--|-----|--|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| Read Cycle | | | | | | | | |
| t _{RC} | Read Cycle Time | 15 | | 25 | | 30 | | ns |
| t _{AA} | Address to Data Valid [9] | | 15 | | 25 | | 30 | ns |
| t _{OHA} | Data Hold from Address Change | 0 | | 0 | | 0 | | ns |
| t _{ACE} | \overline{CE} LOW to Data Valid [9] | | 15 | | 25 | | 30 | ns |
| t _{DOE} | \overline{OE} LOW to Data Valid [9] | | 10 | | 15 | | 20 | ns |
| t _{LZOE} | \overline{OE} LOW to Low Z [7, 10] | 3 | | 3 | | 3 | | ns |
| t _{HZOE} | \overline{OE} HIGH to High Z [7, 10, 11] | | 10 | | 15 | | 15 | ns |
| t _{LZCE} | \overline{CE} LOW to Low Z [7, 10] | 3 | | 5 | | 5 | | ns |
| t _{HZCE} | \overline{CE} HIGH to High Z [7, 10, 11] | | 10 | | 15 | | 15 | ns |
| t _{PU} | \overline{CE} LOW to Power Up [7] | 0 | | 0 | | 0 | | ns |
| t _{PD} | \overline{CE} HIGH to Power Down [7] | | 15 | | 25 | | 25 | ns |

Shaded areas contain preliminary information.

Notes

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30 pF load capacitance.
- AC test conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
- At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
- t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE}, and t_{HZWE} are tested with C_L = 5pF as in (b) of AC Test Loads and Waveforms. Transition is measured ± 500 mV from steady state voltage.

Switching Characteristics

Over the Operating Range (Speeds -15, -25, -30) ^[8] (continued)

| Parameter | Description | 7C136-15 ^[4] 7C146-15 | | 7C132-25 ^[4] 7C136-25 7C142-25 7C146-25 | | 7C132-30 7C136-30 7C142-30 7C146-30 | | Unit |
|---|--|-------------------------------------|---------|---|---------|--|---------|------|
| | | Min | Max | Min | Max | Min | Max | |
| Write Cycle ^[12] | | | | | | | | |
| t _{WC} | Write Cycle Time | 15 | | 25 | | 30 | | ns |
| t _{SCE} | $\overline{\text{CE}}$ LOW to Write End | 12 | | 20 | | 25 | | ns |
| t _{AW} | Address Setup to Write End | 12 | | 20 | | 25 | | ns |
| t _{HA} | Address Hold from Write End | 2 | | 2 | | 2 | | ns |
| t _{SA} | Address Setup to Write Start | 0 | | 0 | | 0 | | ns |
| t _{PWE} | R/W Pulse Width | 12 | | 15 | | 25 | | ns |
| t _{SD} | Data Setup to Write End | 10 | | 15 | | 15 | | ns |
| t _{HD} | Data Hold from Write End | 0 | | 0 | | 0 | | ns |
| t _{HZWE} | R/W LOW to High Z ^[7] | | 10 | | 15 | | 15 | ns |
| t _{LZWE} | R/W HIGH to Low Z ^[7] | 0 | | 0 | | 0 | | ns |
| Busy/Interrupt Timing | | | | | | | | |
| t _{BLA} | BUS $\overline{\text{Y}}$ LOW from Address Match | | 15 | | 20 | | 20 | ns |
| t _{BHA} | BUS $\overline{\text{Y}}$ HIGH from Address Mismatch ^[13] | | 15 | | 20 | | 20 | ns |
| t _{BLC} | BUS $\overline{\text{Y}}$ LOW from $\overline{\text{CE}}$ LOW | | 15 | | 20 | | 20 | ns |
| t _{BHC} | BUS $\overline{\text{Y}}$ HIGH from CE HIGH ^[13] | | 15 | | 20 | | 20 | ns |
| t _{PS} | Port Set Up for Priority | 5 | | 5 | | 5 | | ns |
| t _{WB} | R/W LOW after BUS $\overline{\text{Y}}$ LOW ^[14] | 0 | | 0 | | 0 | | ns |
| t _{WH} | R/W HIGH after BUS $\overline{\text{Y}}$ HIGH | 13 | | 20 | | 30 | | ns |
| t _{BDD} | BUS $\overline{\text{Y}}$ HIGH to Valid Data | | 15 | | 25 | | 30 | ns |
| t _{DDD} | Write Data Valid to Read Data Valid | | Note 15 | | Note 15 | | Note 15 | ns |
| t _{WDD} | Write Pulse to Data Delay | | Note 15 | | Note 15 | | Note 15 | ns |
| Interrupt Timing ^[16] | | | | | | | | |
| t _{WINS} | R/W to $\overline{\text{INTERRUPT}}$ Set Time | | 15 | | 25 | | 25 | ns |
| t _{EINS} | CE to $\overline{\text{INTERRUPT}}$ Set Time | | 15 | | 25 | | 25 | ns |
| t _{INS} | Address to $\overline{\text{INTERRUPT}}$ Set Time | | 15 | | 25 | | 25 | ns |
| t _{OINR} | OE to $\overline{\text{INTERRUPT}}$ Reset Time ^[13] | | 15 | | 25 | | 25 | ns |
| t _{EINR} | CE to $\overline{\text{INTERRUPT}}$ Reset Time ^[13] | | 15 | | 25 | | 25 | ns |
| t _{INR} | Address to $\overline{\text{INTERRUPT}}$ Reset Time ^[13] | | 15 | | 25 | | 25 | ns |

Shaded areas contain preliminary information.

Notes

12. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and R/W LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing must be referenced to the rising edge of the signal that terminates the write.

13. These parameters are measured from the input signal changing, until the output pin goes to a high impedance state.

14. CY7C142/CY7C146 only.

15. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:

BUS $\overline{\text{Y}}$ on Port B goes HIGH.

Port B's address toggled.

CE for Port B is toggled.

R/W for Port B is toggled during valid read.

16. 52-pin PLCC and PQFP versions only.

Switching Characteristics

Over the Operating Range (Speeds -35, -45, -55) ^[8]

| Parameter | Description | 7C132-35 7C136-35 7C142-35 7C146-35 | | 7C132-45 7C136-45 7C142-45 7C146-45 | | 7C132-55 7C136-55 7C136A-55 7C142-55 7C146-55 | | Unit |
|-----------------------------------|--|--|---------|--|---------|---|---------|------|
| | | Min | Max | Min | Max | Min | Max | |
| Read Cycle | | | | | | | | |
| t _{RC} | Read Cycle Time | 35 | | 45 | | 55 | | ns |
| t _{AA} | Address to Data Valid ^[9] | | 35 | | 45 | | 55 | ns |
| t _{OHA} | Data Hold from Address Change | 0 | | 0 | | 0 | | ns |
| t _{ACE} | $\overline{\text{CE}}$ LOW to Data Valid ^[9] | | 35 | | 45 | | 55 | ns |
| t _{DOE} | OE LOW to Data Valid ^[9] | | 20 | | 25 | | 25 | ns |
| t _{LZOE} | OE LOW to Low Z ^[7, 10] | 3 | | 3 | | 3 | | ns |
| t _{HZOE} | OE HIGH to High Z ^[7, 10, 11] | | 20 | | 20 | | 25 | ns |
| t _{LZCE} | $\overline{\text{CE}}$ LOW to Low Z ^[7, 10] | 5 | | 5 | | 5 | | ns |
| t _{HZCE} | $\overline{\text{CE}}$ HIGH to High Z ^[7, 10, 11] | | 20 | | 20 | | 25 | ns |
| t _{PU} | $\overline{\text{CE}}$ LOW to Power Up ^[7] | 0 | | 0 | | 0 | | ns |
| t _{PD} | $\overline{\text{CE}}$ HIGH to Power Down ^[7] | | 35 | | 35 | | 35 | ns |
| Write Cycle^[12] | | | | | | | | |
| t _{WC} | Write Cycle Time | 35 | | 45 | | 55 | | ns |
| t _{SCE} | $\overline{\text{CE}}$ LOW to Write End | 30 | | 35 | | 40 | | ns |
| t _{AW} | Address Setup to Write End | 30 | | 35 | | 40 | | ns |
| t _{HA} | Address Hold from Write End | 2 | | 2 | | 2 | | ns |
| t _{SA} | Address Setup to Write Start | 0 | | 0 | | 0 | | ns |
| t _{PWE} | R/W Pulse Width | 25 | | 30 | | 30 | | ns |
| t _{SD} | Data Setup to Write End | 15 | | 20 | | 20 | | ns |
| t _{HD} | Data Hold from Write End | 0 | | 0 | | 0 | | ns |
| t _{HZWE} | R/W LOW to High Z ^[7] | | 20 | | 20 | | 25 | ns |
| t _{LZWE} | R/W HIGH to Low Z ^[7] | 0 | | 0 | | 0 | | ns |
| Busy/Interrupt Timing | | | | | | | | |
| t _{BLA} | BUSY LOW from Address Match | | 20 | | 25 | | 30 | ns |
| t _{BHA} | BUSY HIGH from Address Mismatch ^[13] | | 20 | | 25 | | 30 | ns |
| t _{BLC} | BUSY LOW from $\overline{\text{CE}}$ LOW | | 20 | | 25 | | 30 | ns |
| t _{BHC} | BUSY HIGH from $\overline{\text{CE}}$ HIGH ^[13] | | 20 | | 25 | | 30 | ns |
| t _{PS} | Port Set Up for Priority | 5 | | 5 | | 5 | | ns |
| t _{WB} | R/W LOW after BUSY LOW ^[14] | 0 | | 0 | | 0 | | ns |
| t _{WH} | R/W HIGH after BUSY HIGH | 30 | | 35 | | 35 | | ns |
| t _{BDD} | BUSY HIGH to Valid Data | | 35 | | 45 | | 45 | ns |
| t _{DDD} | Write Data Valid to Read Data Valid | | Note 15 | | Note 15 | | Note 15 | ns |
| t _{WDD} | Write Pulse to Data Delay | | Note 15 | | Note 15 | | Note 15 | ns |

Switching Characteristics

Over the Operating Range (Speeds -35, -45, -55) [8] (continued)

| Parameter | Description | 7C132-35 7C136-35 7C142-35 7C146-35 | | 7C132-45 7C136-45 7C142-45 7C146-45 | | 7C132-55 7C136-55 7C136A-55 7C142-55 7C146-55 | | Unit |
|------------------------------|--------------------------------------|--|-----|--|-----|---|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| Interrupt Timing [16] | | | | | | | | |
| t_{WINS} | R/W to INTERRUPT Set Time | | 25 | | 35 | | 45 | ns |
| t_{EINS} | CE to INTERRUPT Set Time | | 25 | | 35 | | 45 | ns |
| t_{INS} | Address to INTERRUPT Set Time | | 25 | | 35 | | 45 | ns |
| t_{OINR} | OE to INTERRUPT Reset Time [13] | | 25 | | 35 | | 45 | ns |
| t_{EINR} | CE to INTERRUPT Reset Time [13] | | 25 | | 35 | | 45 | ns |
| t_{INR} | Address to INTERRUPT Reset Time [13] | | 25 | | 35 | | 45 | ns |

Switching Waveforms

Figure 4. Read Cycle No. 1 (Either Port-Address Access) [17, 18]

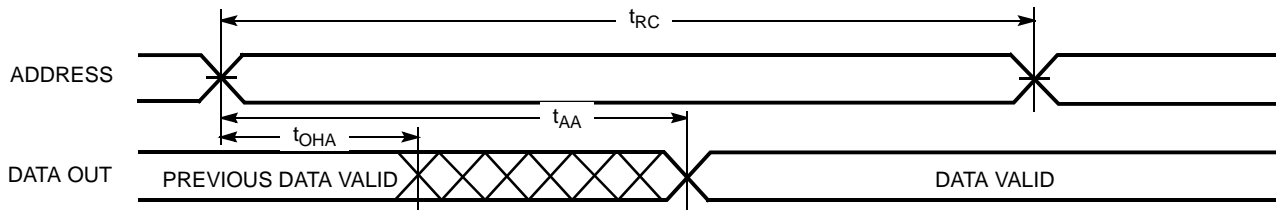
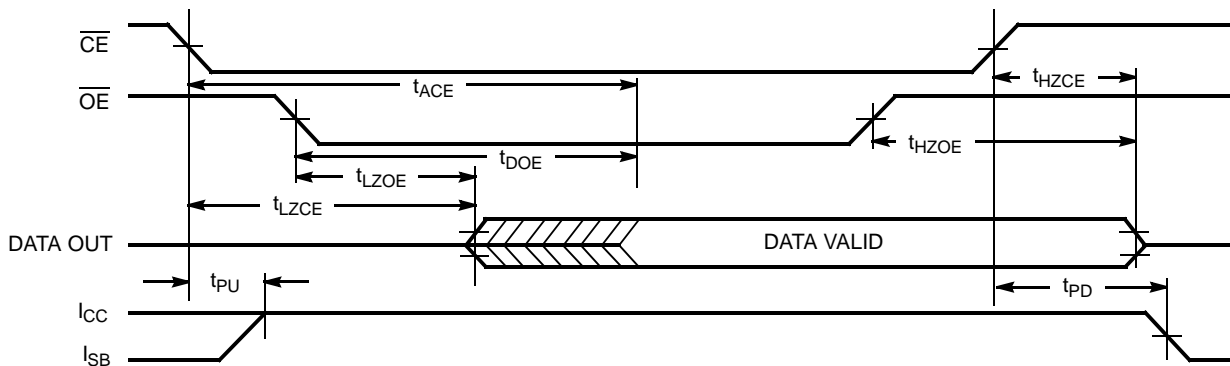


Figure 5. Read Cycle No. 2 (Either Port-CE/OE) [17, 19]



Notes

17. R/W is HIGH for read cycle.
18. Device is continuously selected, $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IL}$.
19. Address valid prior to or coincident with CE transition LOW.

Switching Waveforms (continued)

Figure 6. Read Cycle No. 3 (Read with $\overline{\text{BUSY}}$ Master: CY7C132 and CY7C136/CY7C136A)

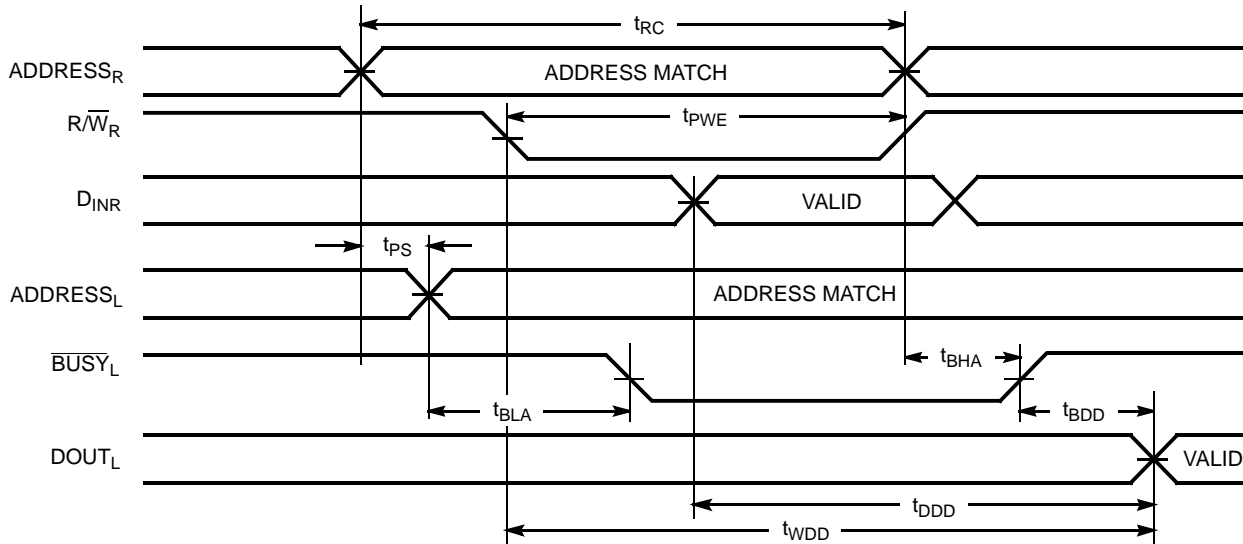
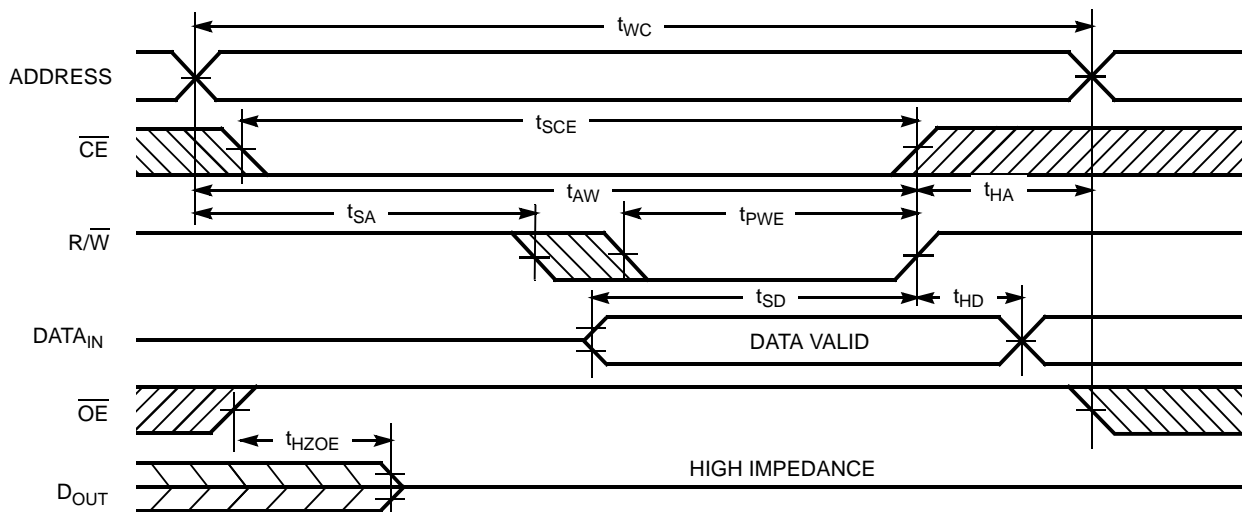


Figure 7. Write Cycle No.1 ($\overline{\text{OE}}$ Three-States Data I/Os—Either Port) [12, 20]



Note

20. If $\overline{\text{OE}}$ is LOW during a $\overline{\text{R/W}}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or $t_{\text{HZOE}} + t_{\text{SD}}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD} .

Switching Waveforms (continued)

Figure 8. Write Cycle No. 2 (R/W Three-States Data I/Os—Either Port)^[12, 21]

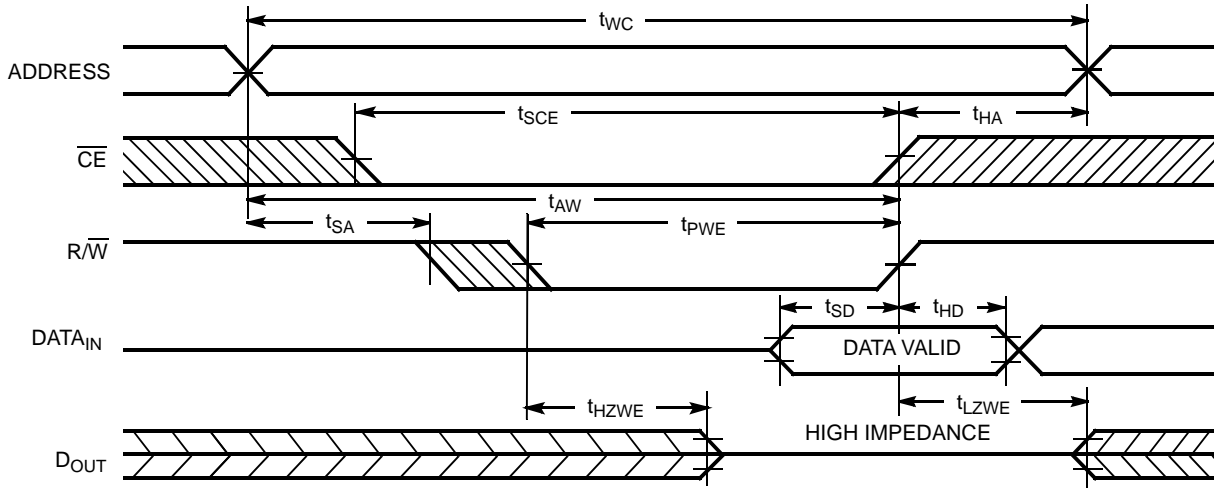
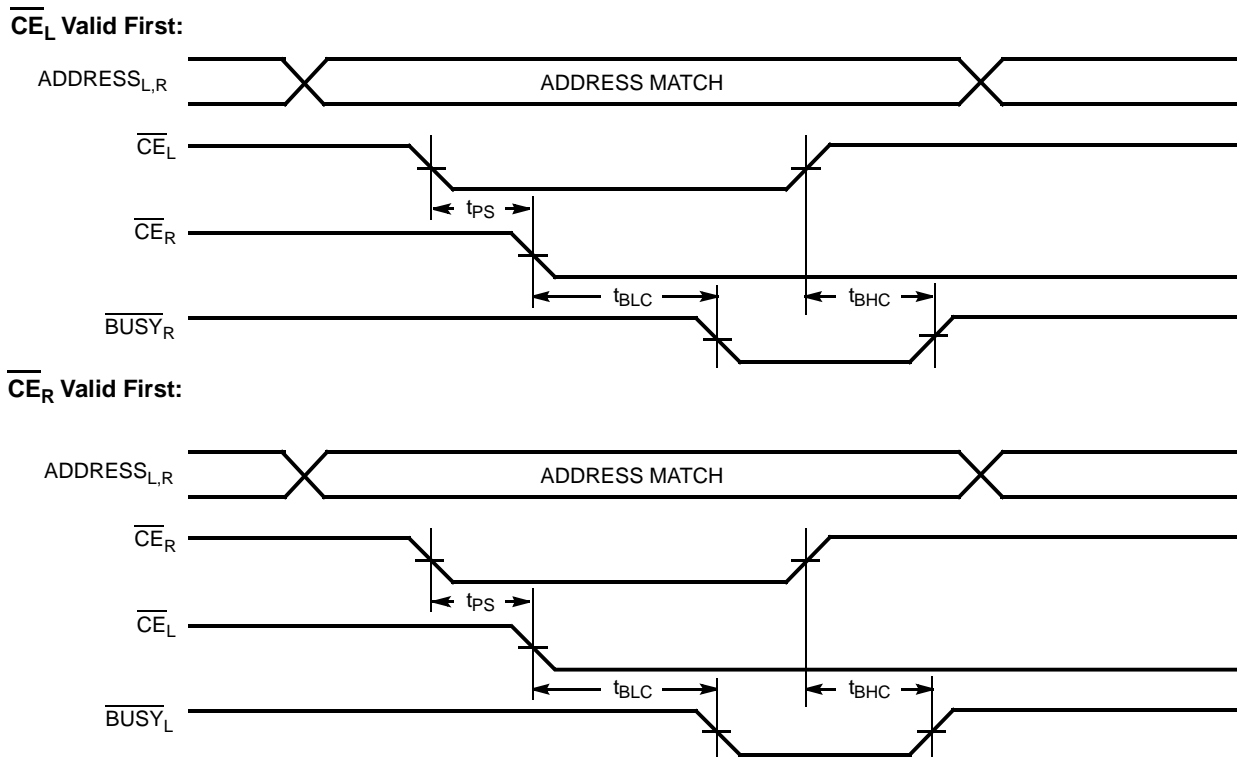


Figure 9. Busy Timing Diagram No. 1 (CE Arbitration)



Note

21. If the CE LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in a high impedance state.

Switching Waveforms (continued)

Figure 10. Busy Timing Diagram No. 2 (Address Arbitration)

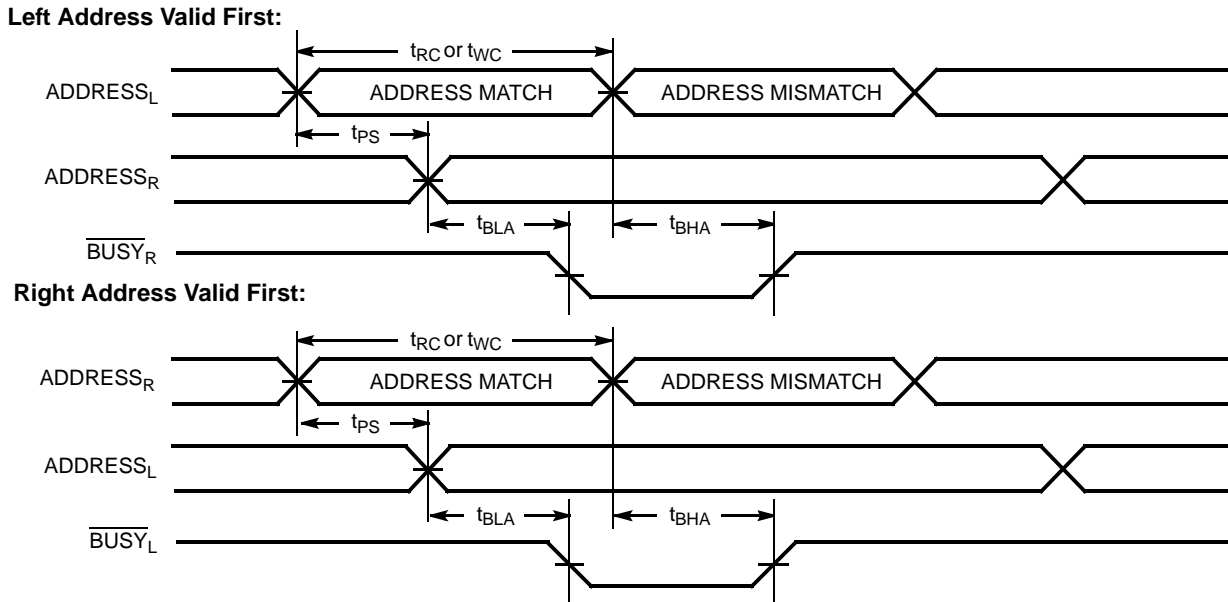
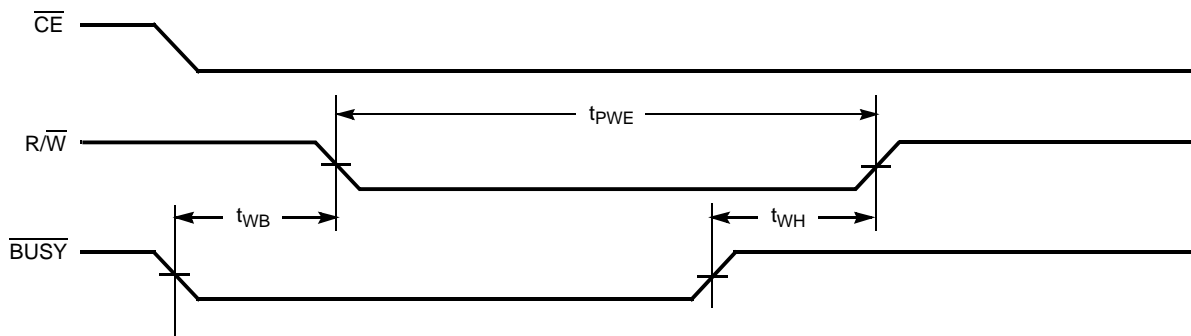


Figure 11. Busy Timing Diagram No. 3 (Write with $\overline{\text{BUSY}}$, Slave: CY7C142/CY7C146)



Switching Waveforms (continued)

Interrupt Timing Diagrams [16]

Figure 12. Left Side Sets $\overline{\text{INT}}_R$

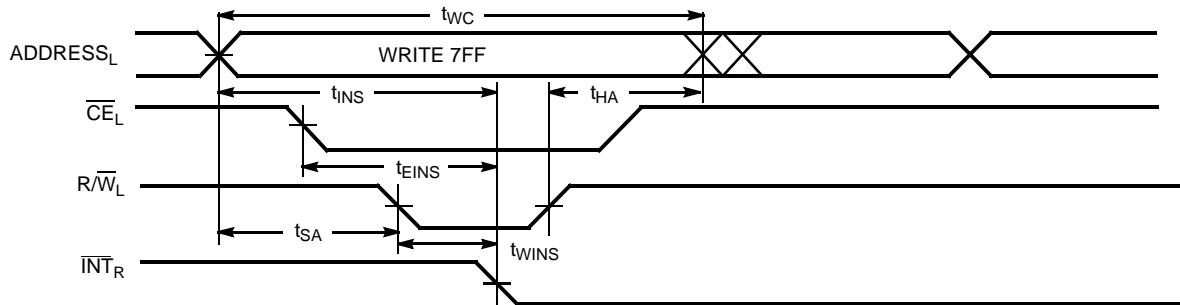


Figure 13. Right Side Clears $\overline{\text{INT}}_R$

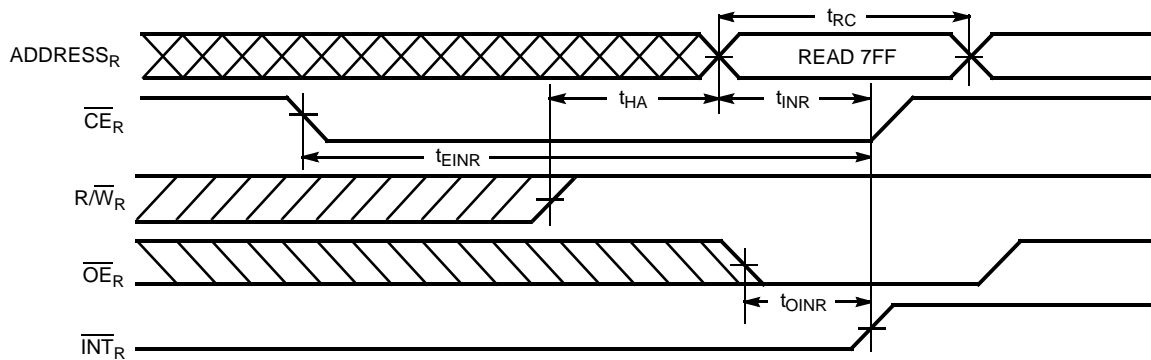


Figure 14. Right Side Sets $\overline{\text{INT}}_L$

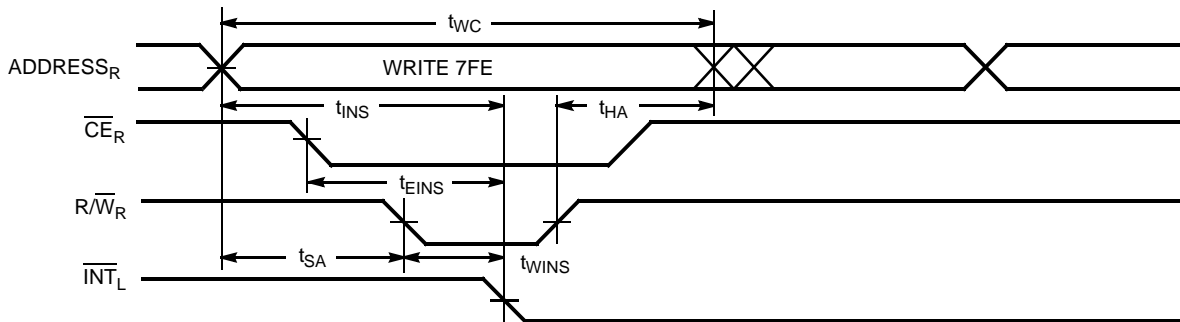


Figure 15. Right Side Clears $\overline{\text{INT}}_L$

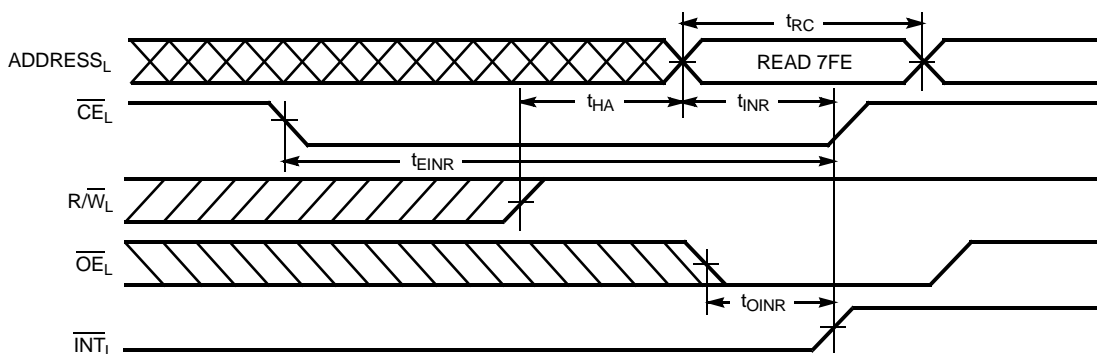
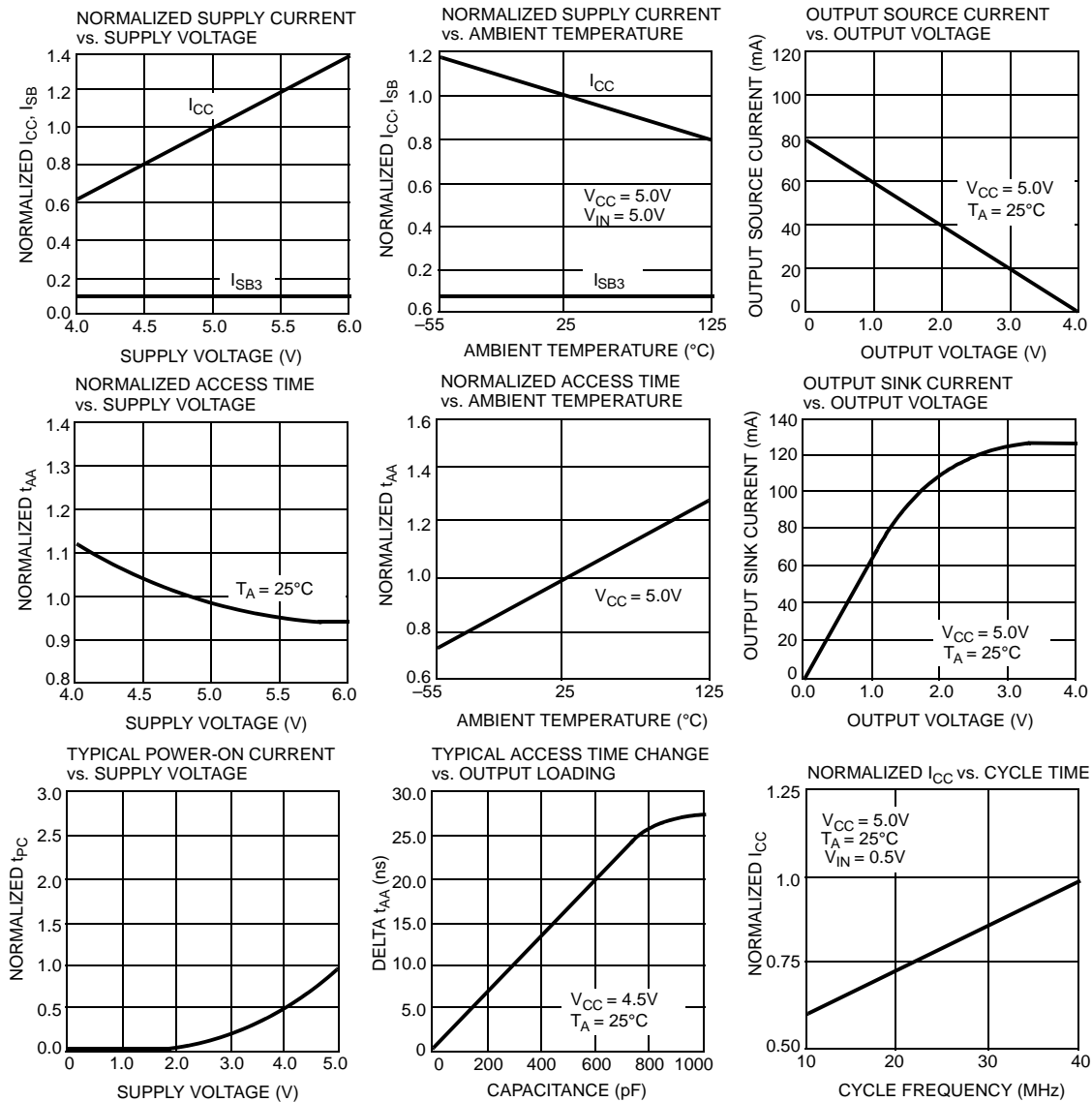


Figure 16. Typical DC and AC Characteristics

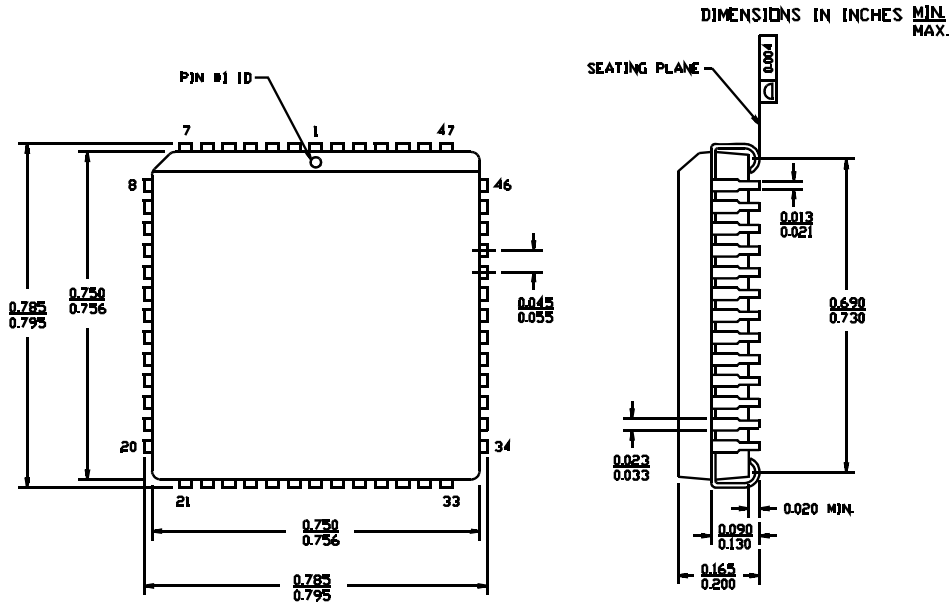


Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range | |
|------------|----------------|-----------------|--|-----------------|------------|
| 15 | CY7C136-15JC | 51-85004 | 52-Pin Plastic Leaded Chip Carrier | Commercial | |
| | CY7C136-15NC | 51-85042 | 52-Pin Plastic Quad Flatpack | | |
| 25 | CY7C136-25JC | 51-85004 | 52-Pin Plastic Leaded Chip Carrier | Commercial | |
| | CY7C136-25JXC | | 52-Pin Plastic Leaded Chip Carrier (Pb-Free) | | |
| | CY7C136-25NC | 51-85042 | 52-Pin Plastic Quad Flatpack | | |
| | CY7C136-25NXC | | 52-Pin Plastic Quad Flatpack (Pb-Free) | | |
| | CY7C136-25JXI | 51-85004 | 52-Pin Plastic Leaded Chip Carrier (Pb-Free) | | Industrial |
| 30 | CY7C136-30JC | 51-85004 | 52-Pin Plastic Leaded Chip Carrier | Commercial | |
| | CY7C136-30NC | 51-85042 | 52-Pin Plastic Quad Flatpack | | |
| | CY7C136-30JI | 51-85004 | 52-Pin Plastic Leaded Chip Carrier | Industrial | |
| 35 | CY7C136-35JC | 51-85004 | 52-Pin Plastic Leaded Chip Carrier | Commercial | |
| | CY7C136-35NC | 51-85042 | 52-Pin Plastic Quad Flatpack | | |
| | CY7C136-35JI | 51-85004 | 52-Pin Plastic Leaded Chip Carrier | Industrial | |
| 45 | CY7C136-45JC | 51-85004 | 52-Pin Plastic Leaded Chip Carrier | Commercial | |
| | CY7C136-45NC | 51-85042 | 52-Pin Plastic Quad Flatpack | | |
| | CY7C136-45JI | 51-85004 | 52-Pin Plastic Leaded Chip Carrier | Industrial | |
| 55 | CY7C136-55JC | 51-85004 | 52-Pin Plastic Leaded Chip Carrier | Commercial | |
| | CY7C136-55JXC | | 52-Pin Plastic Leaded Chip Carrier (Pb-Free) | | |
| | CY7C136-55NC | 51-85042 | 52-Pin Plastic Quad Flatpack | | |
| | CY7C136-55NXC | | 52-Pin Plastic Quad Flatpack (Pb-Free) | | |
| | CY7C136-55JI | 51-85004 | 52-Pin Plastic Leaded Chip Carrier | | Industrial |
| | CY7C136A-55JXI | | 52-Pin Plastic Leaded Chip Carrier (Pb-Free) | | |
| | CY7C136-55NI | 51-85042 | 52-Pin Plastic Quad Flatpack | | |
| | CY7C136A-55NXI | | 52-Pin Plastic Quad Flatpack (Pb-Free) | | |
| 15 | CY7C146-15JC | 51-85004 | 52-Pin Plastic Leaded Chip Carrier | Commercial | |
| | CY7C146-15NC | 51-85042 | 52-Pin Plastic Quad Flatpack | | |
| 25 | CY7C146-25JC | 51-85004 | 52-Pin Plastic Leaded Chip Carrier | Commercial | |
| | CY7C146-25JXC | | 52-Pin Plastic Leaded Chip Carrier (Pb-Free) | | |
| | CY7C146-25NC | 51-85042 | 52-Pin Plastic Quad Flatpack | | |
| 30 | CY7C146-30JC | 51-85004 | 52-Pin Plastic Leaded Chip Carrier | Commercial | |
| | CY7C146-30NC | 51-85042 | 52-Pin Plastic Quad Flatpack | | |
| | CY7C146-30JI | 51-85004 | 52-Pin Plastic Leaded Chip Carrier | Industrial | |
| 35 | CY7C146-35JC | 51-85004 | 52-Pin Plastic Leaded Chip Carrier | Commercial | |
| | CY7C146-35NC | 51-85042 | 52-Pin Plastic Quad Flatpack | | |
| | CY7C146-35JI | 51-85004 | 52-Pin Plastic Leaded Chip Carrier | Industrial | |
| 45 | CY7C146-45JC | 51-85004 | 52-Pin Plastic Leaded Chip Carrier | Commercial | |
| | CY7C146-45NC | 51-85042 | 52-Pin Plastic Quad Flatpack | | |
| | CY7C146-45JI | 51-85004 | 52-Pin Plastic Leaded Chip Carrier | Industrial | |
| 55 | CY7C146-55JC | 51-85004 | 52-Pin Plastic Leaded Chip Carrier | Commercial | |
| | CY7C146-55JXC | | 52-Pin Plastic Leaded Chip Carrier (Pb-Free) | | |
| | CY7C146-55NC | 51-85042 | 52-Pin Plastic Quad Flatpack | | |
| | CY7C146-55JI | 51-85004 | 52-Pin Plastic Leaded Chip Carrier | | Industrial |

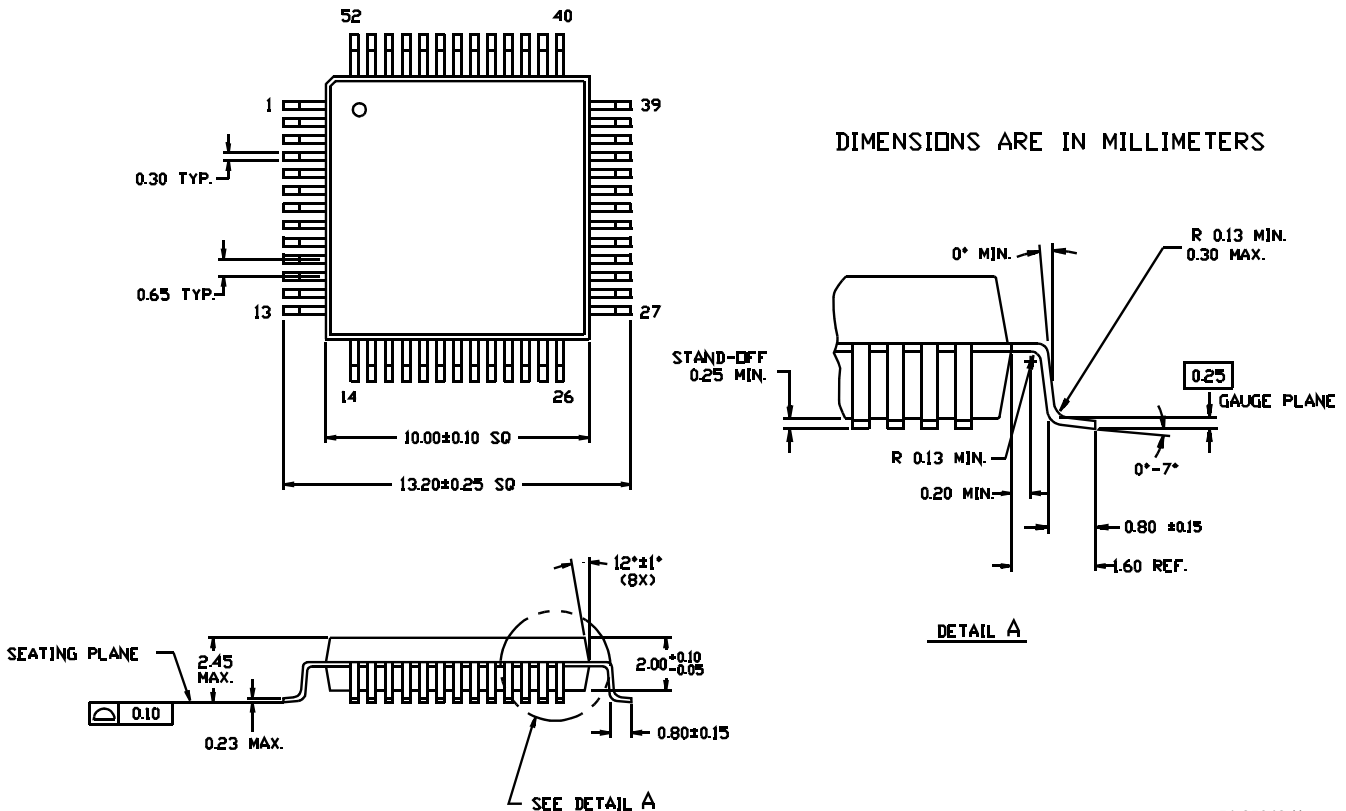
Package Diagrams

Figure 17. 52-Pin Plastic Leaded Chip Carrier, 51-85004



51-85004-*A

Figure 18. 52-Pin Plastic Quad Flatpack, 51-85042



51-85042-**

Document History Page

| Document Title: CY7C132, CY7C136, CY7C136A, CY7C142, CY7C146 2K x 8 Dual-Port Static RAM | | | | |
|--|---------|-----------------|-----------------|---|
| Document Number: 38-06031 | | | | |
| Revision | ECN | Submission Date | Orig. of Change | Description of Change |
| ** | 110171 | 10/21/01 | SZV | Change from Spec number: 38-06031 |
| *A | 128959 | 09/03/03 | JFU | Added CY7C136-55NI to Order Information |
| *B | 236748 | See ECN | YDT | Removed cross information from features section |
| *C | 393184 | See ECN | YIM | Added Pb-Free Logo Added Pb-Free parts to ordering information: CY7C136-25JXC, CY7C136-25NXC, CY7C136-55JXC, CY7C136-55NXC, CY7C136-55JXI, CY7C136-55NXI, CY7C146-25JXC, CY7C146-55JXC |
| *D | 2623658 | 12/17/08 | VKN/PYRS | Added CY7C136-25JXI part Removed CY7C132/142 from the Ordering information table Removed 48-Pin DIP and 52-Pin Square LCC package from the data sheet |
| *E | 2678221 | 03/24/2009 | VKN/AESA | Added CY7C136A-55JXI, and CY7C136A-55NXI parts. |

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products

| | |
|------------------|--|
| PSoC | psoc.cypress.com |
| Clocks & Buffers | clocks.cypress.com |
| Wireless | wireless.cypress.com |
| Memories | memory.cypress.com |
| Image Sensors | image.cypress.com |

PSoC Solutions

| | |
|-----------------------|--|
| General | psoc.cypress.com/solutions |
| Low Power/Low Voltage | psoc.cypress.com/low-power |
| Precision Analog | psoc.cypress.com/precision-analog |
| LCD Drive | psoc.cypress.com/lcd-drive |
| CAN 2.0b | psoc.cypress.com/can |
| USB | psoc.cypress.com/usb |

© Cypress Semiconductor Corporation, 2005-2009. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and/or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.