CY7C1069AV33

2M x 8 Static RAM

Features

- High Speed
  - t_{AA} = 10, 12 ns
- Low Active Power
  - 990 mW (max.)
- Operating Voltages of 3.3 ± 0.3V
- 2.0V Data Retention
- Automatic Power Down when deselected
- TTL-compatible Inputs and Outputs
- Easy Memory Expansion with $\overline{CE}_1$ and CE_2 features
- Available in Pb-free and non Pb-free 54-pin TSOP II, non Pb-free 60-ball Fine-Pitch Ball Grid Array (FBGA) package

Functional Description

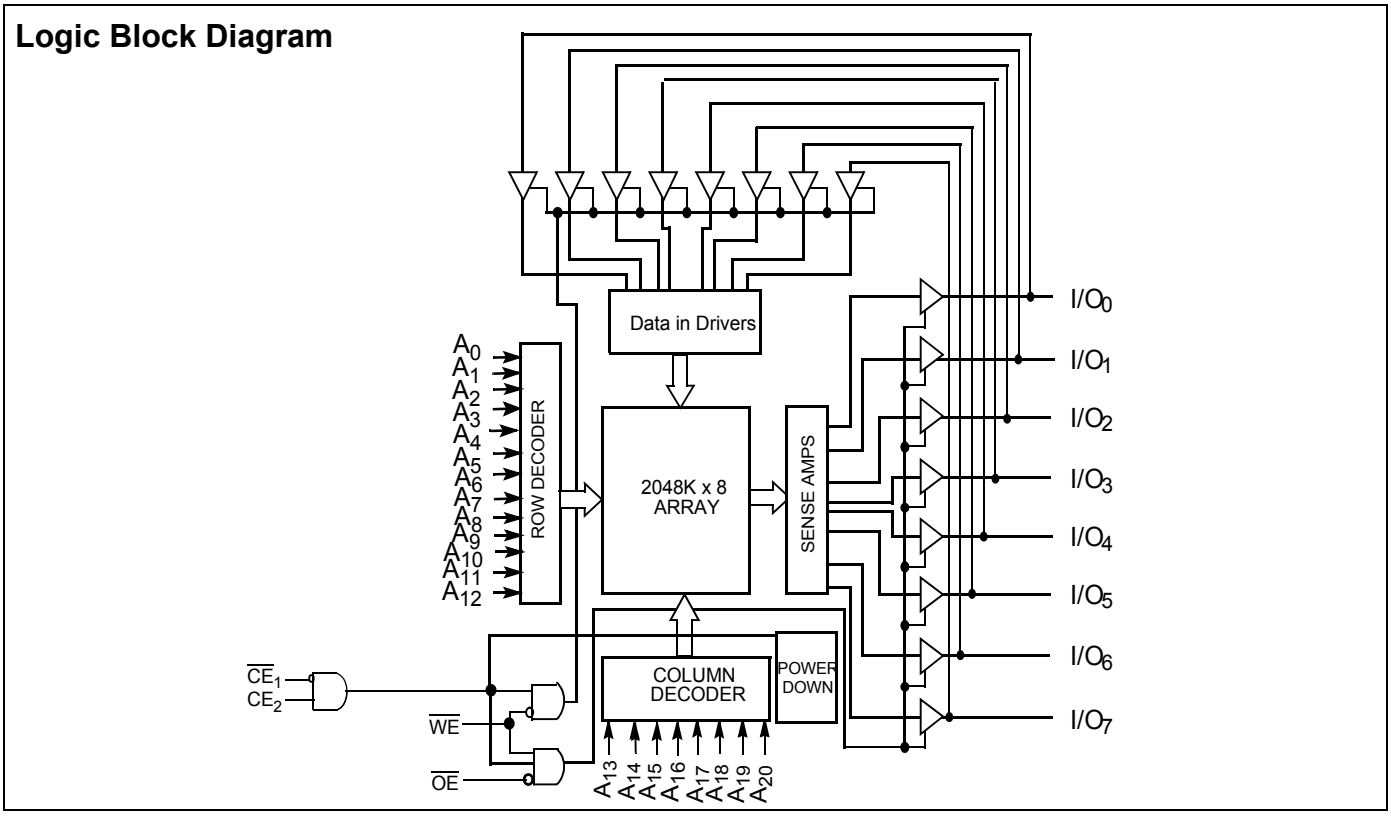
The CY7C1069AV33 is a high performance CMOS Static RAM organized as 2,097,152 words by 8 bits. Writing to the device is accomplished by enabling the chip (by taking $\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) inputs LOW.

Reading from the device is accomplished by enabling the chip ($\overline{CE}_1$ LOW and CE_2 HIGH) as well as forcing the Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. See "Truth Table" on page 8 for a complete description of Read and Write modes.

The input/output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a Write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

The CY7C1069AV33 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout and a 60-ball fine-pitch ball grid array (FBGA) package.

Logic Block Diagram

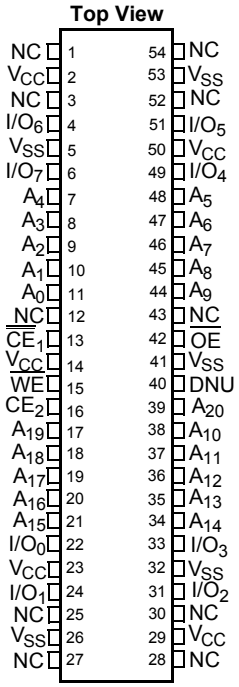


Selection Guide

Description	–10	–12	Unit
Maximum Access Time	10	12	ns
Maximum Operating Current	275	260	mA
Maximum CMOS Standby Current	50	50	mA

Pin Configuration

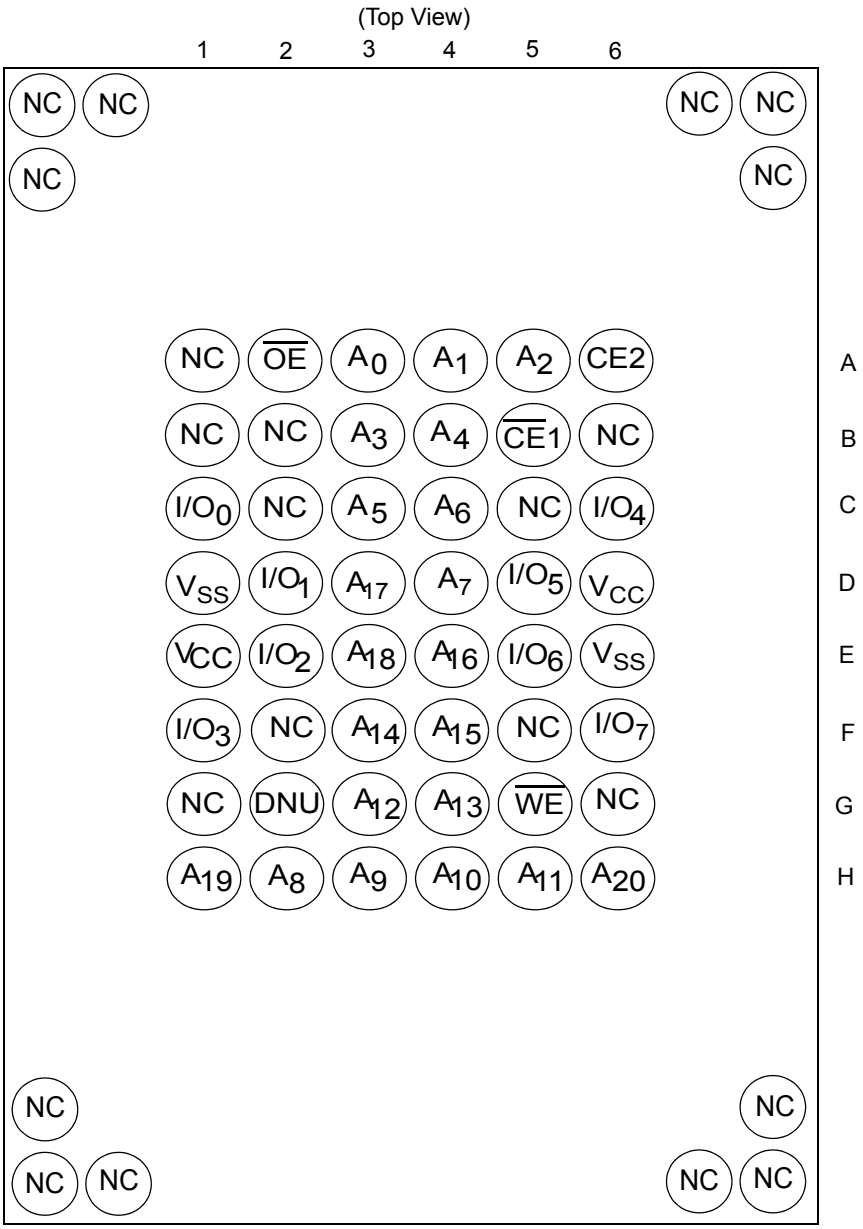
Figure 1. 54-Pin TSOP II [1, 2]



Notes
1. NC pins are not connected on the die.
2. DNU pins have to be left floating or tied to VSS to ensure proper application.

Pin Configuration

Figure 2. 54-Pin TSOP II [1, 2]



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[3] .....–0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State[3] ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage[3] ..... –0.5V to V_{CC} + 0.5V

Current into Outputs (LOW)..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	–10		–12		Unit
			Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[3]		–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled	–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = $1/t_{RC}$		275		260	mA
I_{SB1}	Automatic CE Power Down Current —TTL Inputs	CE_2 ≤ V_{IL}, Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		70		70	mA
I_{SB2}	Automatic CE Power Down Current —CMOS Inputs	$\underline{CE}_2$ ≤ 0.3V, Max. V_{CC}, CE_1 ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0		50		50	mA

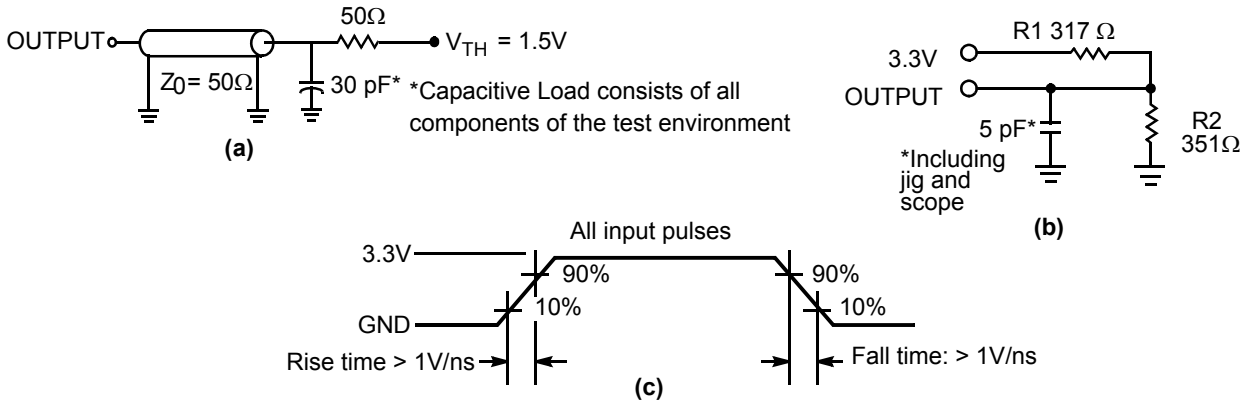
Capacitance

Tested initially and after any design or process changes that may affect these parameters.[4]

Parameter	Description	Test Conditions	TSOP II	FBGA	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	6	8	pF
C_{OUT}	I/O Capacitance		8	10	pF

Notes
3. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
4. Tested initially and after any design or process changes that may affect these parameters.

Figure 3. AC Test Loads and Waveforms[5]



AC Switching Characteristics Over the Operating Range [7]

Parameter	Description	–10		–12		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{power}	V_{CC}(typical) to the First Access[8]	1		1		ms
t_{RC}	Read Cycle Time	10		12		ns
t_{AA}	Address to Data Valid		10		12	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}_1$ LOW/CE_2 HIGH to Data Valid		10		12	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[9]	1		1		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[9]		5		6	ns
t_{LZCE}	$\overline{CE}_1$ LOW/CE_2 HIGH to Low-Z[9]	3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH/CE_2 LOW to High-Z[9]		5		6	ns
t_{PU}	$\overline{CE}_1$ LOW/CE_2 HIGH to Power Up[10]	0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH/CE_2 LOW to Power Down[10]		10		12	ns
Write Cycle[10, 11]						
t_{WC}	Write Cycle Time	10		12		ns
t_{SCE}	$\overline{CE}_1$ LOW/CE_2 HIGH to Write End	7		8		ns
t_{AW}	Address Setup to Write End	7		8		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Setup to Write Start	0		0		ns

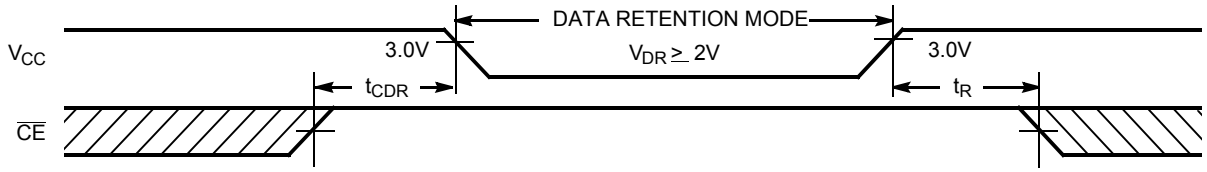
Notes

5. Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0V). As soon as 1ms (T_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation can begin including reduction in V_{DD} to the data retention (V_{CCDR}, 2.0V) voltage.
6. Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0V). As soon as 1ms (T_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation can begin including reduction in V_{DD} to the data retention (V_{CCDR}, 2.0V) voltage.
7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and transmission line loads. Test conditions for the Read cycle use output loading shown in part a) of the AC test loads, unless specified otherwise.
8. This part has a voltage regulator which steps down the voltage from 3V to 2V internally. t_{power} time has to be provided initially before a Read/Write operation is started.
9. t_{HZOE}, t_{HZCE}, t_{HZWE} and t_{LZOE}, t_{LZCE}, and t_{LZWE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
10. These parameters are guaranteed by design and are not tested.
11. The internal Write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW/CE_2 HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ must be LOW along with CE_2 HIGH to initiate a Write, and the transition of any of these signals can terminate the Write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the Write.
12. The minimum Write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

AC Switching Characteristics Over the Operating Range (continued)[7]

Parameter	Description	–10		–12		Unit
		Min	Max	Min	Max	
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		ns
t_{SD}	Data Setup to Write End	5.5		6		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[9]	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[9]		5		6	ns

Figure 4. Data Retention Waveform



Switching Waveforms

Figure 5. Read Cycle No. 1[13, 14]

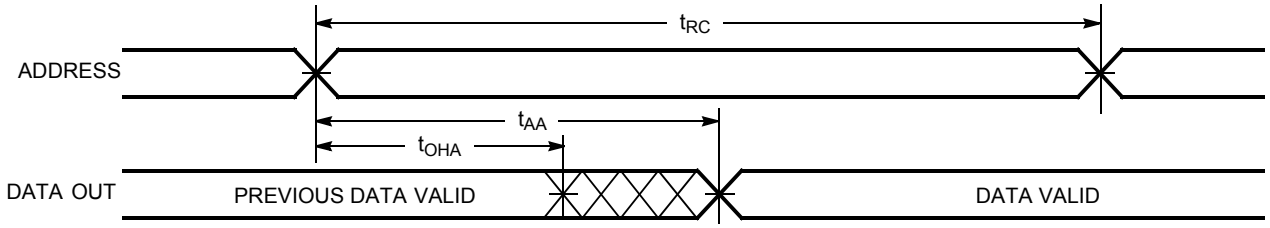
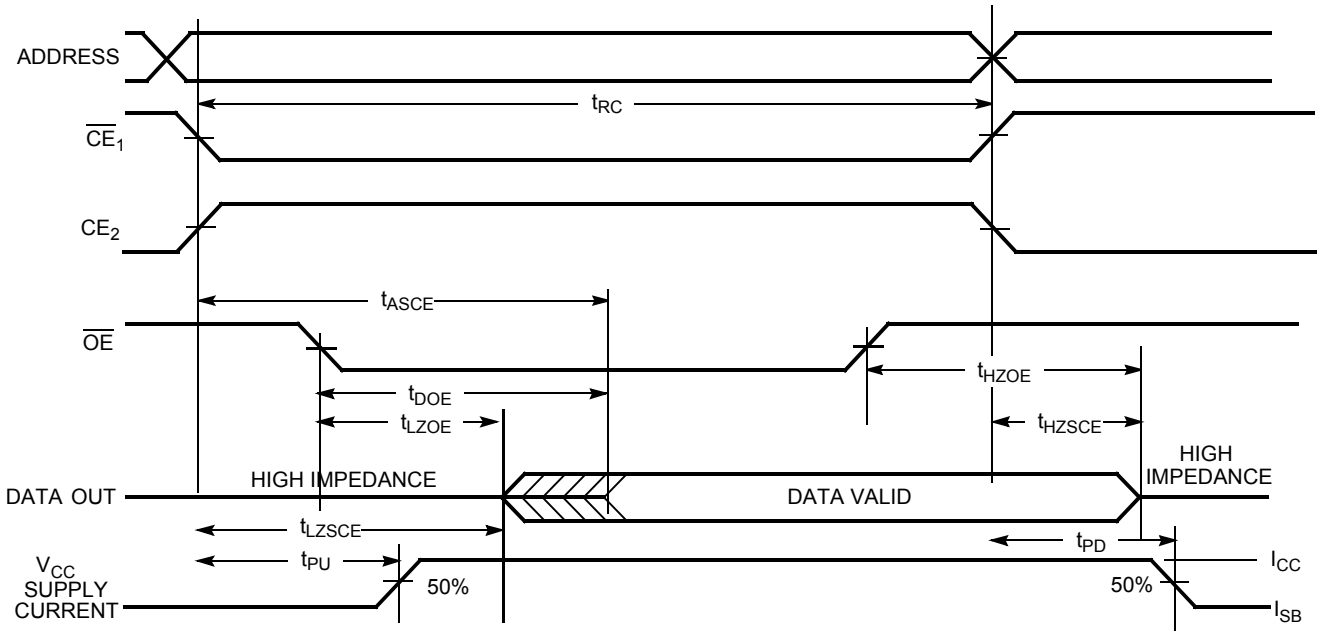


Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled)[14, 15]



Notes
13. Device is continuously selected. $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
14. $\overline{WE}$ is HIGH for Read cycle.
15. Address valid prior to or coincident with $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ($\overline{CE}_1$ Controlled)[16, 17, 18]

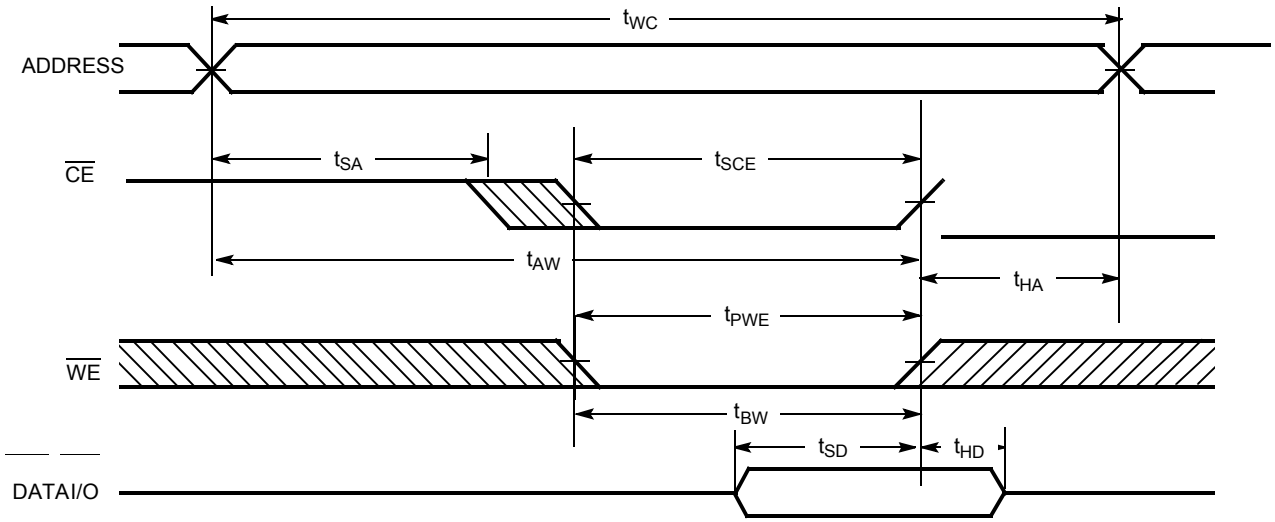
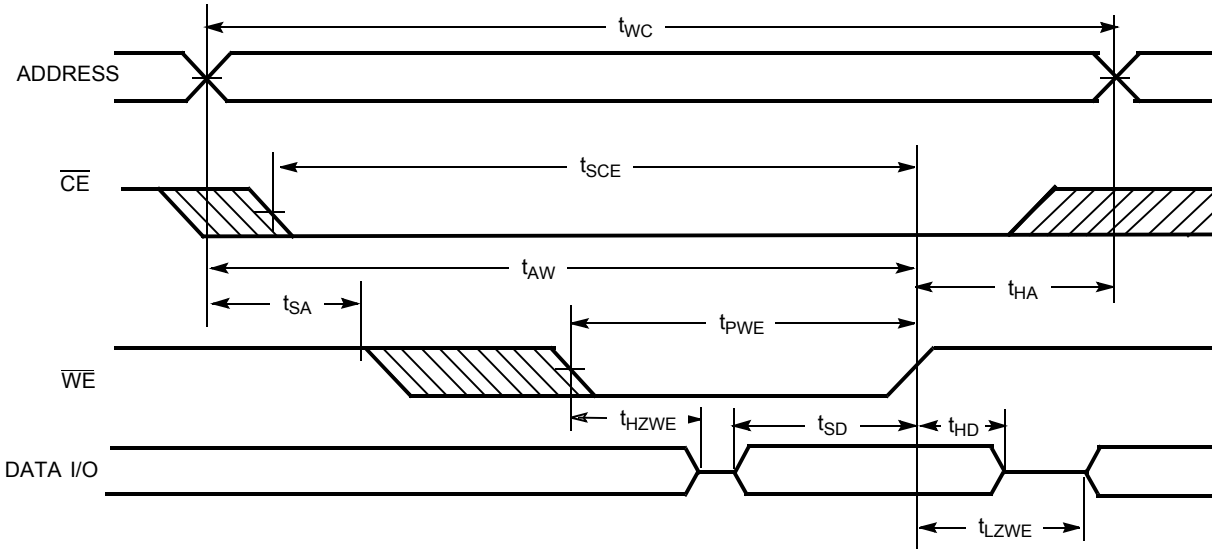


Figure 8. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[16, 17, 18]



Truth Table

$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	X	High-Z	Power Down	Standby (I_{SB})
X	L	X	X	High-Z	Power Down	Standby (I_{SB})
L	H	L	H	Data Out	Read All Bits	Active (I_{CC})
L	H	X	L	Data In	Write All Bits	Active (I_{CC})
L	H	H	H	High-Z	Selected, Outputs Disabled	Active (I_{CC})

Notes
16. Data I/O is high-impedance if $\overline{OE}$ = V_{IH}.
17. If $\overline{CE}_1$ goes HIGH/CE_2 LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high–impedance state.
18. $\overline{CE}$ above is defined as a combination of $\overline{CE}_1$ and CE_2. It is active low.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1069AV33-10ZC	51-85160	54-pin TSOP II	Commercial
	CY7C1069AV33-10ZXC		54-pin TSOP II (Pb-free)	
	CY7C1069AV33-10BAC	51-85162	60-ball (8 mm x 20 mm x 1.2 mm) FBGA	
	CY7C1069AV33-10ZXI		54-pin TSOP II (Pb-free)	
	CY7C1069AV33-10BAI	51-85162	60-ball (8 mm x 20 mm x 1.2 mm) FBGA	
12	CY7C1069AV33-12ZC	51-85160	54-pin TSOP II	Commercial
	CY7C1069AV33-12ZXC		54-pin TSOP II (Pb-free)	
	CY7C1069AV33-12ZI	51-85160	54-pin TSOP II	Industrial

Package Diagrams

Figure 9. 54-Pin TSOP II (51-85160)

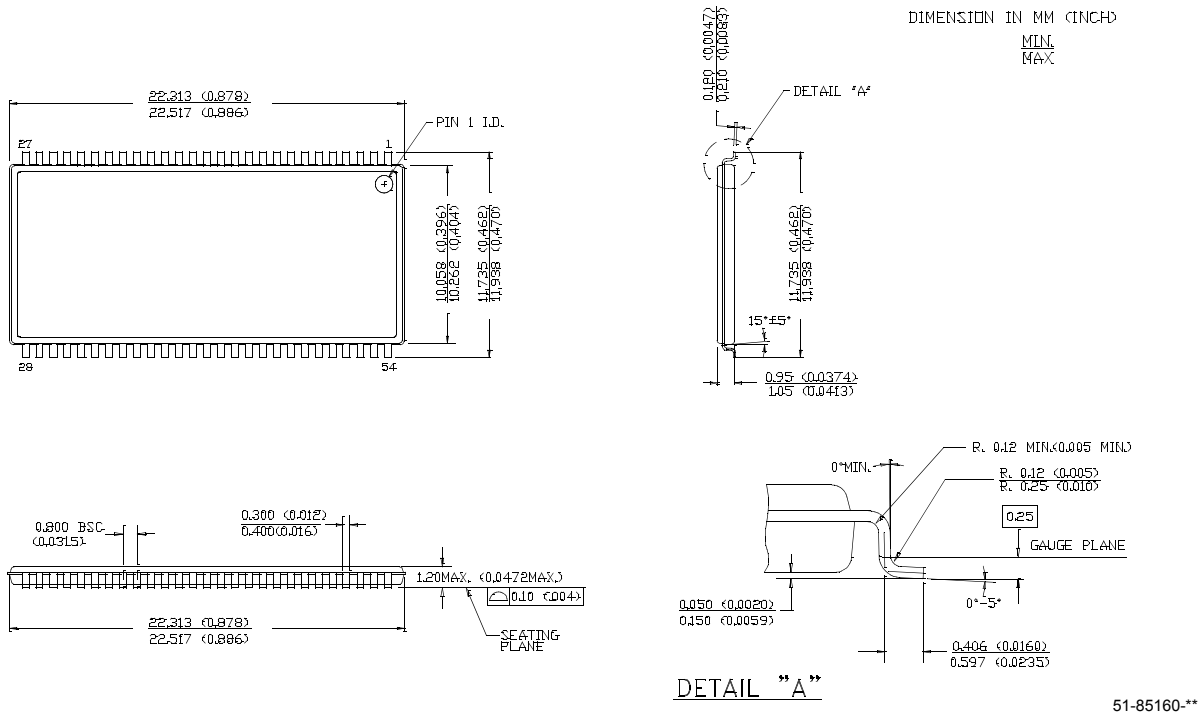
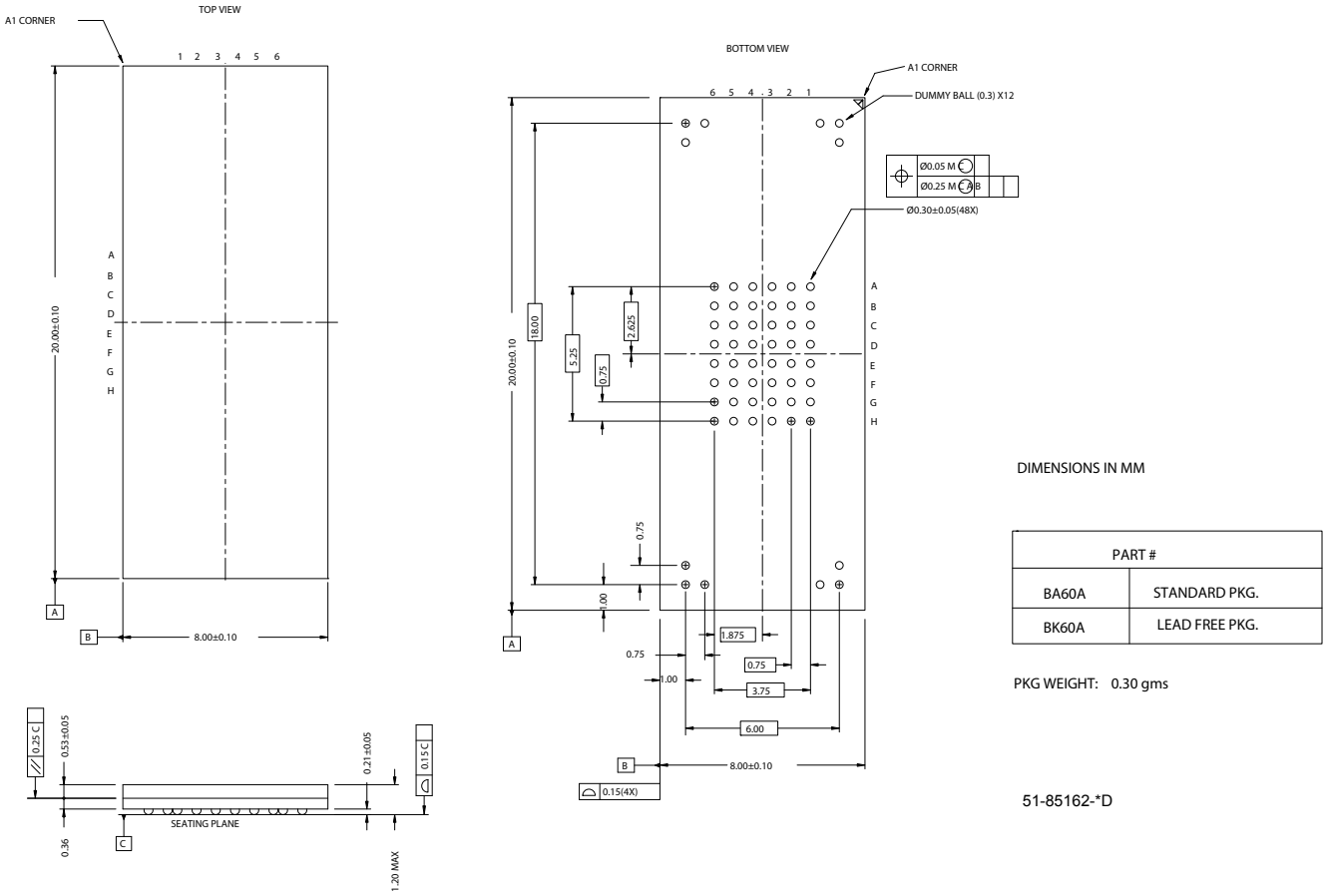


Figure 10. 60-Ball FBGA (8 mm x 20 mm x 1.2 mm) (51-85162)



Document History Page

Document Title: CY7C1069AV33 2M x 8 Static RAM Document Number: 38-05255				
REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	113724	03/27/02	NSL	New Data Sheet
*A	117060	07/31/02	DFP	Removed 15-ns bin
*B	117990	08/30/02	DFP	Added 8-ns bin Changing I_{CC} for 8, 10, 12 bins t_{power} changed from 1 µs to 1 ms Load Cap Comment changed (for Tx line load) t_{SD} changed to 5.5 ns for the 10-ns bin Changed some 8-ns bin #'s (t_{HZ}, t_{DOE}, t_{DBE}) Removed hz < lz comments
*C	120385	11/13/02	DFP	Final Data Sheet Added note 4 to “AC Test Loads and Waveforms” and note 7 to t_{pu} and t_{pd} Updated Input/Output Caps (for 48BGA only) to 8 pf/10 pf and for the 54-pin TSOP to 6/8 pf
*D	124441	2/25/03	MEG	Changed ISB1 from 100 mA to 70 mA Shaded the 48fBGA product offering information
*E	403984	See ECN	NXR	Changed the Logic Block Diagram On page # 1 Added notes under Pin Configuration Changed the Package diagram of 51-85162 from Rev *A to Rev *D Changed 48-Ball FBGA to 60-Ball FBGA in Pin Configuration Updated the Ordering Information
*F	492137	See ECN	NXR	Removed 8 ns speed bin from product offering Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated the Ordering Information
*G	2784946	10/12/2009	VKN/PYRS	Updated template Corrected typo in footnote 9 Updated Ordering Information table

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