

**1M (64K x 16) Static RAM**
**Features**

- **High Speed: 55 ns and 70 ns**
- **Wide voltage range: 2.7V–3.6V**
- **Low active power**  
— 54 mW (max.) (15 mA)
- **Low standby power (70 ns)**  
— 54 μW (max.) (15 μA)
- **Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Package available in a 44-pin TSOP Type II (forward pinout) and a 48-ball fBGA package**

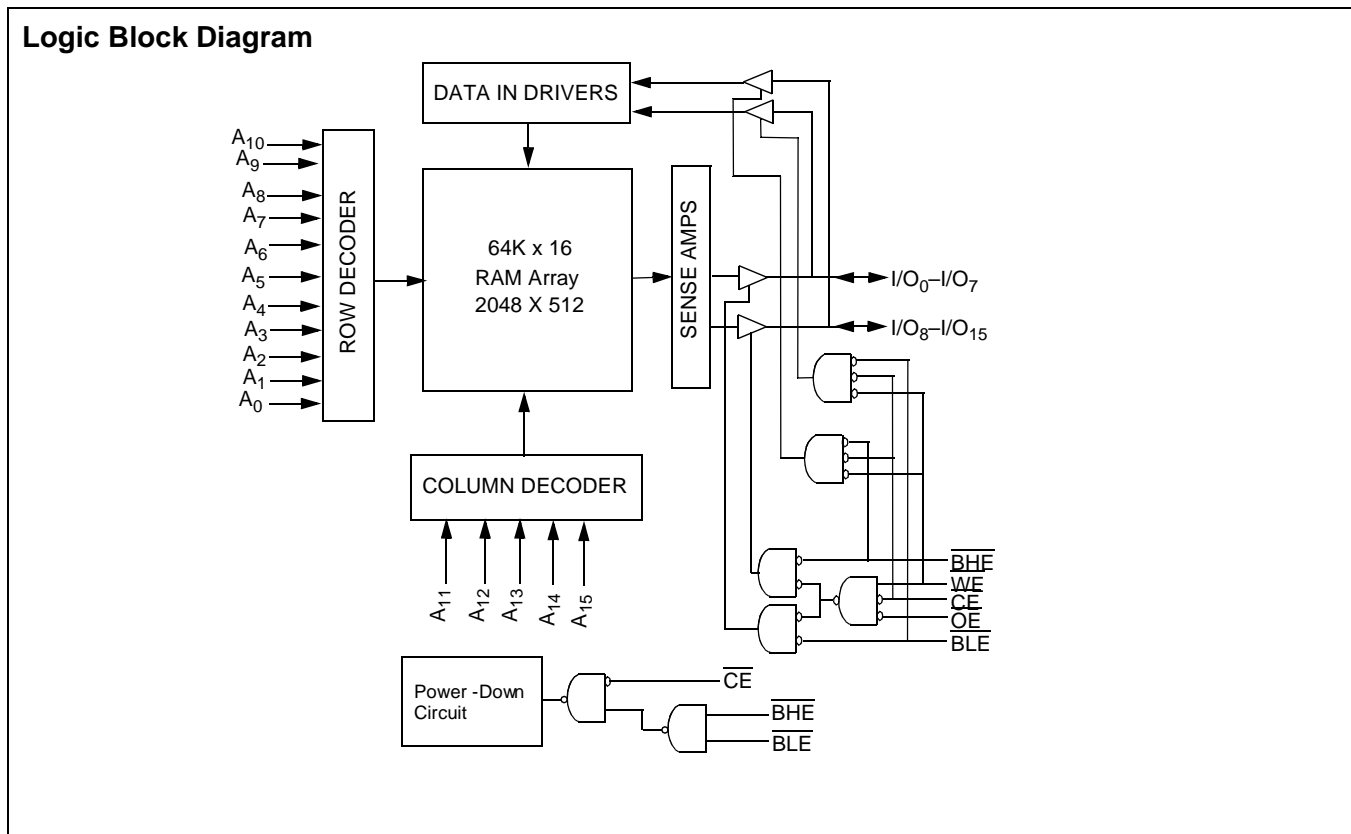
**Functional Description<sup>[1]</sup>**

The CY62127BV MoBL<sup>®</sup> MoBL<sup>®</sup> is a high-performance CMOS static RAM organized as 64K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL) in portable applications such as cellular telephones. The device also has an automatic power-down feature that

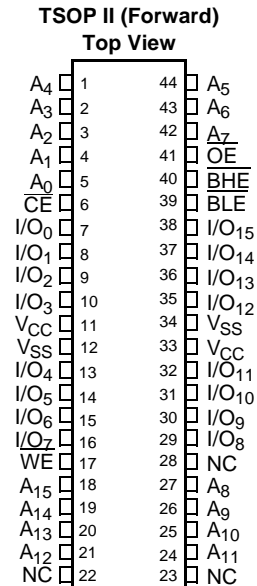
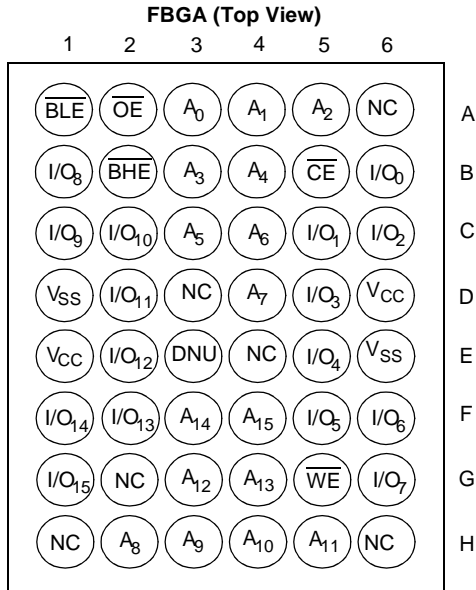
significantly reduces power consumption when addresses are not toggling, or when deselected ( $\overline{CE}$  HIGH or both  $\overline{BLE}$  and  $\overline{BHE}$  are HIGH). The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when: deselected ( $\overline{CE}$  HIGH), outputs are disabled ( $\overline{OE}$  HIGH), both Byte High Enable and Byte Low Enable are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins (I/O<sub>1</sub> through I/O<sub>8</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins (I/O<sub>9</sub> through I/O<sub>16</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the back of this data sheet for a complete description of read and write modes.


**Note:**

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

**Pin Configurations<sup>[2]</sup>**

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied ..... -55°C to +125°C  
 Supply Voltage to Ground Potential ..... -0.5V to 4.6V  
 DC Voltage Applied to Outputs  
 in High-Z State<sup>[3]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

DC Input Voltage<sup>[3]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V  
 Output Current into Outputs (LOW) ..... 20 mA  
 Static Discharge Voltage ..... >2001V  
 (per MIL-STD-883, Method 3015)  
 Latch-up Current ..... >200 mA

**Operating Range**

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Industrial | -40°C to +85°C      | 2.7V to 3.6V    |

**Product Portfolio**

| Product         | V <sub>CC</sub> Range (V) |                                       |                        | Speed (ns) | Power Dissipation (Industrial)                       |                     |                                |      |
|-----------------|---------------------------|---------------------------------------|------------------------|------------|--|---------------------|--------------------------------|------|
|                 | V <sub>CC</sub> (min.)    | V <sub>CC</sub> (typ.) <sup>[4]</sup> | V <sub>CC</sub> (max.) |            | Operating, I <sub>CC</sub> (mA) f = f <sub>max</sub> |                     | Standby, I <sub>SB2</sub> (μA) |      |
|                 |                           |                                       |                        |            | Max.   | Typ. <sup>[4]</sup> | Typ. <sup>[4]</sup>            | Max. |
| CY62127BV MoBL® | 2.7                       | 3.0                                   | 3.6                    | 55         | 20   | 0.5                 | 15                             |      |
|                 |                           |                                       |                        | 70         | 15   |                     |                                |      |

**Notes:**

2. NC pins are not connected to the die.
3. V<sub>IL(min.)</sub> = -2.0V for pulse durations less than 20 ns.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.

**Electrical Characteristics** Over the Operating Range

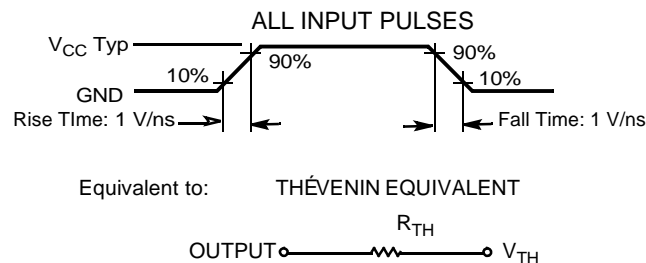
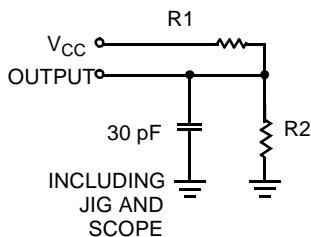
| Parameter        | Description                                  | Test Conditions   | CY62127BV MoBL®-55 |                     |                        | CY62127BV MoBL®-70 |                     |                        | Unit |
|------------------|--|---|--------------------|---------------------|------------------------|--------------------|---------------------|------------------------|------|
|                  |  |   | Min.               | Typ. <sup>[4]</sup> | Max.                   | Min.               | Typ. <sup>[4]</sup> | Max.                   |      |
| V <sub>OH</sub>  | Output HIGH Voltage                          | I <sub>OH</sub> = -1.0 mA<br>V <sub>CC</sub> = 2.7V   | 2.2                |                     |                        | 2.2                |                     |                        | V    |
| V <sub>OL</sub>  | Output LOW Voltage                           | I <sub>OL</sub> = 2.1 mA<br>V <sub>CC</sub> = 2.7V  |                    |                     | 0.4                    |                    |                     | 0.4                    | V    |
| V <sub>IH</sub>  | Input HIGH Voltage                           |   | 2.0                |                     | V <sub>CC</sub> + 0.3V | 2.0                |                     | V <sub>CC</sub> + 0.3V | V    |
| V <sub>IL</sub>  | Input LOW Voltage                            |   | -0.3               |                     | 0.4                    | -0.3               |                     | 0.4                    | V    |
| I <sub>IX</sub>  | Input Leakage Current                        | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>  | -1                 |                     | +1                     | -1                 |                     | +1                     | μA   |
| I <sub>OZ</sub>  | Output Leakage Current                       | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled  | -1                 |                     | +1                     | -1                 |                     | +1                     | μA   |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current     | f = f <sub>MAX</sub> = 1/t <sub>RC</sub><br>V <sub>CC</sub> = 3.6V<br>I <sub>OUT</sub> = 0 mA<br>CMOS Levels  |                    |                     | 20                     |                    |                     | 15                     | mA   |
| I <sub>SB1</sub> | Automatic CE Power-Down Current— TTL Inputs  | Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$<br>V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> |                    |                     | 2                      |                    |                     | 2                      | mA   |
| I <sub>SB2</sub> | Automatic CE Power-Down Current— CMOS Inputs | Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ ,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V,<br>f = 0        |                    | 0.5                 | 15                     |                    | 0.5                 | 15                     | μA   |

**Capacitance<sup>[5]</sup>**

| Parameter        | Description        | Test Conditions   | Max. | Unit |
|------------------|--------------------|---|------|------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 3.3V | 9    | pF   |
| C <sub>OUT</sub> | Output Capacitance |   | 9    | pF   |

**Thermal Resistance**

| Description   | Test Conditions   | Symbol          | BGA | Unit |
|---|---|-----------------|-----|------|
| Thermal Resistance (Junction to Ambient) <sup>[5]</sup> | Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board | θ <sub>JA</sub> | 55  | °C/W |
| Thermal Resistance (Junction to Case) <sup>[5]</sup>    |   | θ <sub>JC</sub> | 16  | °C/W |

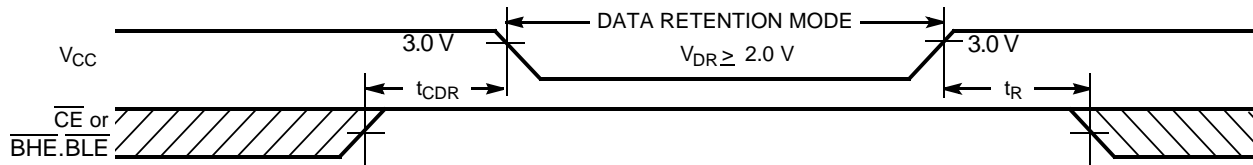
**AC Test Loads and Waveforms**

**Note:**

5. Tested initially and after any design or process changes that may affect these parameters.

| Parameters      | 3.0V  | Unit   |
|-----------------|-------|--------|
| R1              | 1.076 | K Ohms |
| R2              | 1.262 | K Ohms |
| R <sub>TH</sub> | 0.581 | K Ohms |
| V <sub>TH</sub> | 1.620 | Volts  |

**Data Retention Characteristics** (Over the Operating Range)

| Parameter                       | Description                          | Conditions  | Min.            | Typ. <sup>[4]</sup> | Max. | Unit |
|---------------------------------|--------------------------------------|---|-----------------|---------------------|------|------|
| V <sub>DR</sub>                 | V <sub>CC</sub> for Data Retention   |   | 2.0             |                     | 3.6  | V    |
| I <sub>CCDR</sub>               | Data Retention Current               | V <sub>CC</sub> = V <sub>DR</sub> = 2.0V, CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V |                 | 0.5                 | 15   | μA   |
| t <sub>CDR</sub> <sup>[5]</sup> | Chip Deselect to Data Retention Time |   | 0               |                     |      | ns   |
| t <sub>R</sub> <sup>[6]</sup>   | Operation Recovery Time              |   | t <sub>RC</sub> |                     |      | ns   |

**Data Retention Waveform<sup>[7]</sup>**

**Switching Characteristics** Over the Operating Range <sup>[8]</sup>

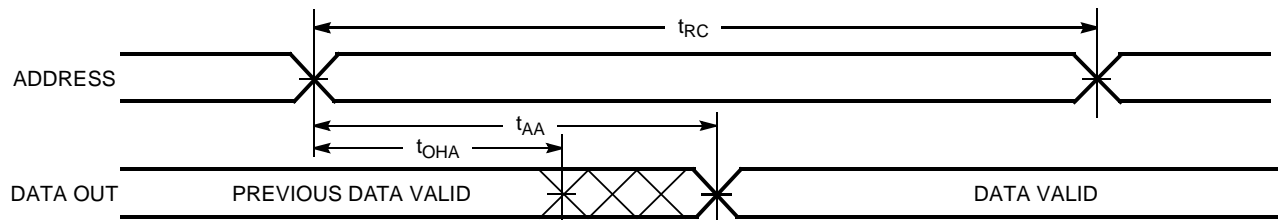
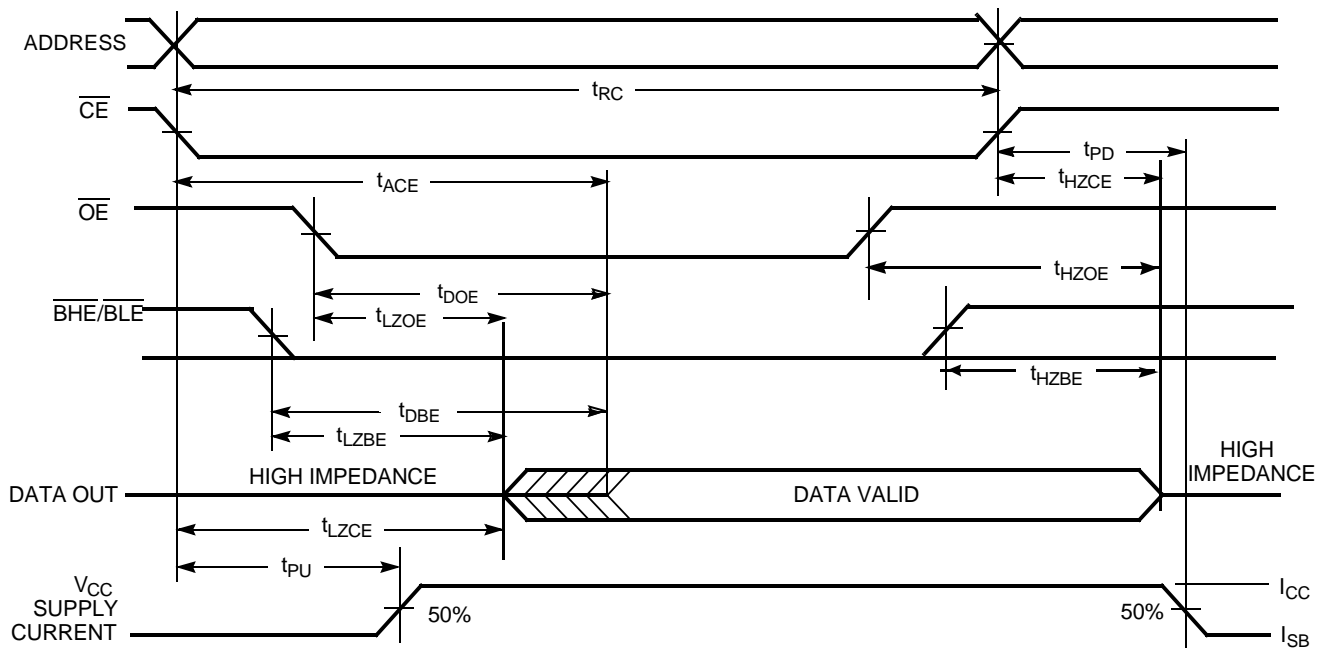
| Parameter                         | Description                                 | 55 ns |      | 70 ns |      | Unit |
|-----------------------------------|---|-------|------|-------|------|------|
|                                   |   | Min.  | Max. | Min.  | Max. |      |
| <b>Read Cycle</b>                 |   |       |      |       |      |      |
| t <sub>RC</sub>                   | Read Cycle Time                             | 55    |      | 70    |      | ns   |
| t <sub>AA</sub>                   | Address to Data Valid                       |       | 55   |       | 70   | ns   |
| t <sub>OHA</sub>                  | Data Hold from Address Change               | 10    |      | 10    |      | ns   |
| t <sub>ACE</sub>                  | CE LOW to Data Valid                        |       | 55   |       | 70   | ns   |
| t <sub>DOE</sub>                  | OE LOW to Data Valid                        |       | 25   |       | 35   | ns   |
| t <sub>LZOE</sub>                 | OE LOW to Low Z <sup>[9]</sup>              | 5     |      | 5     |      | ns   |
| t <sub>HZOE</sub>                 | OE HIGH to High Z <sup>[9, 11]</sup>        |       | 20   |       | 25   | ns   |
| t <sub>LZCE</sub>                 | CE LOW to Low Z <sup>[9]</sup>              | 10    |      | 10    |      | ns   |
| t <sub>HZCE</sub>                 | CE HIGH to High Z <sup>[9, 11]</sup>        |       | 20   |       | 25   | ns   |
| t <sub>PU</sub>                   | CE LOW to Power-Up                          | 0     |      | 0     |      | ns   |
| t <sub>PD</sub>                   | CE HIGH to Power-Down                       |       | 55   |       | 70   | ns   |
| t <sub>DBE</sub>                  | BHE / BLE LOW to Data Valid                 |       | 55   |       | 70   | ns   |
| t <sub>LZBE</sub> <sup>[10]</sup> | BHE / BLE LOW to Low Z <sup>[9]</sup>       | 5     |      | 5     |      | ns   |
| t <sub>HZBE</sub>                 | BHE / BLE HIGH to High Z <sup>[9, 11]</sup> |       | 20   |       | 25   | ns   |
| <b>Write Cycle<sup>[12]</sup></b> |   |       |      |       |      |      |
| t <sub>WC</sub>                   | Write Cycle Time                            | 55    |      | 70    |      | ns   |
| t <sub>SCE</sub>                  | CE LOW to Write End                         | 45    |      | 60    |      | ns   |

**Notes:**

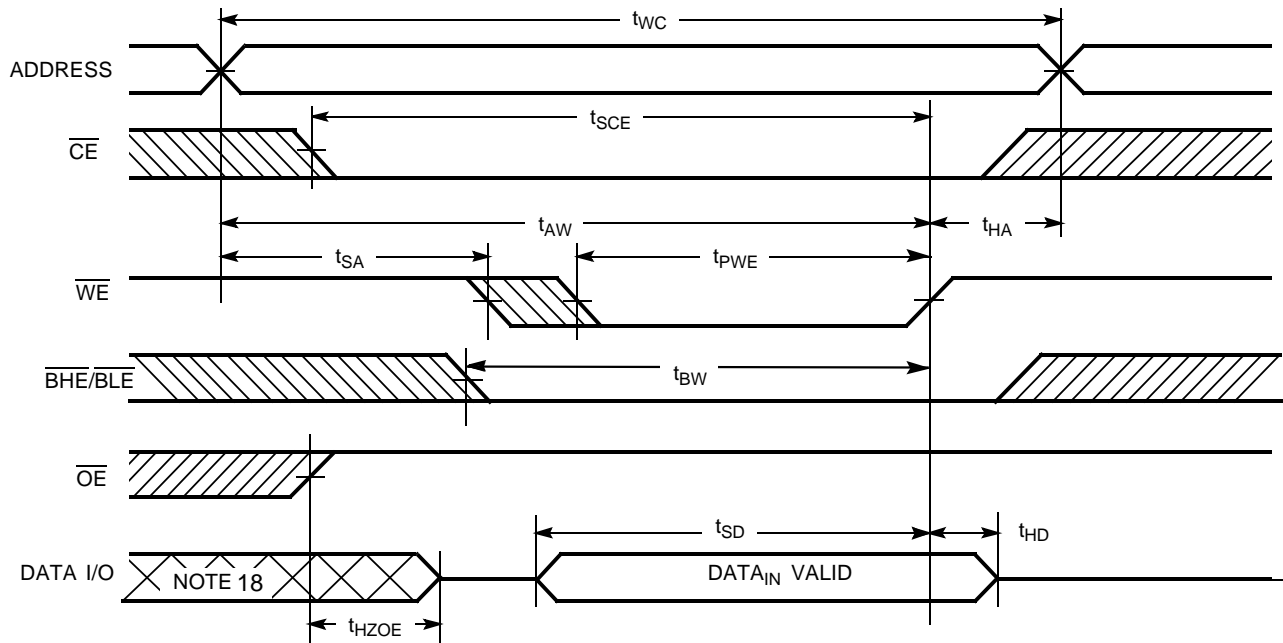
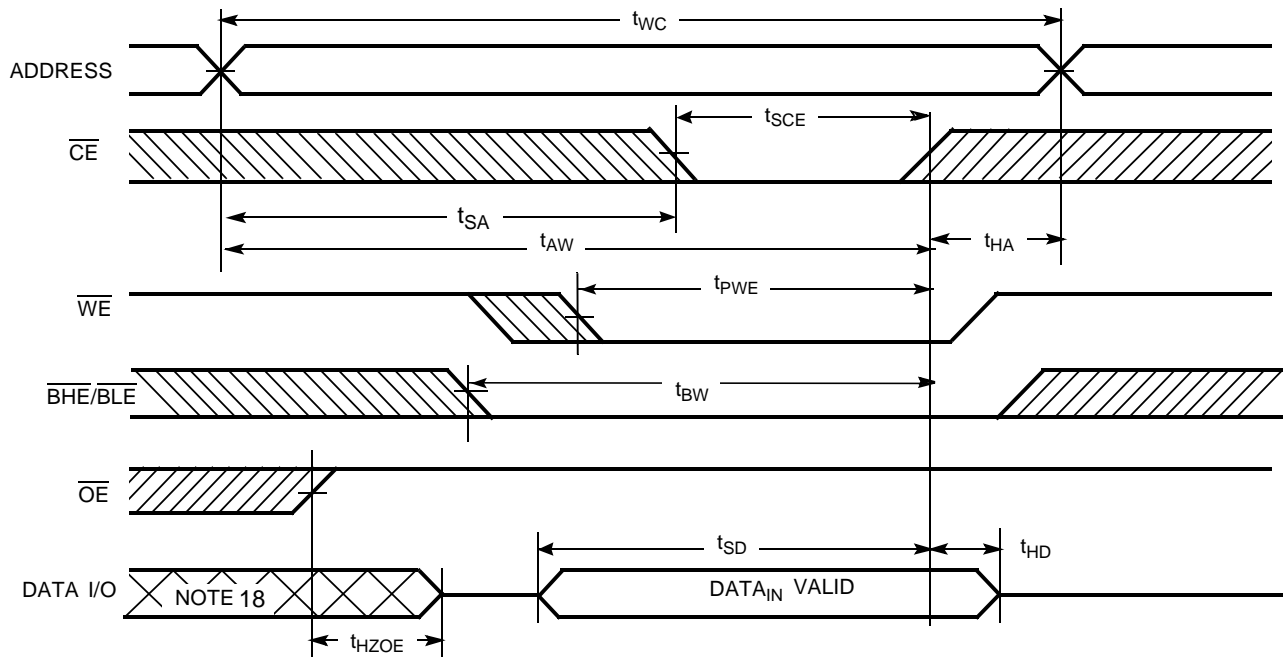
- Full Device AC operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min.)</sub> > 100 μs or stable at V<sub>CC(min.)</sub> > 100 μs.
- BHE, BLE is the AND of both BHE and BLE. Chip can be deselected by either disabling the chip enable signals or by disabling both BHE and BLE.
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of V<sub>CC(typ.)</sub>/2, input pulse levels of 0 to V<sub>CC(typ.)</sub>, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZBE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- If both byte enables are toggled together this value is 10 ns.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high impedance state.
- The internal write time of the memory is defined by the overlap of WE, CE = V<sub>IL</sub>, BHE and/or BLE = V<sub>IL</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

**Switching Characteristics** Over the Operating Range (continued)<sup>[8]</sup>

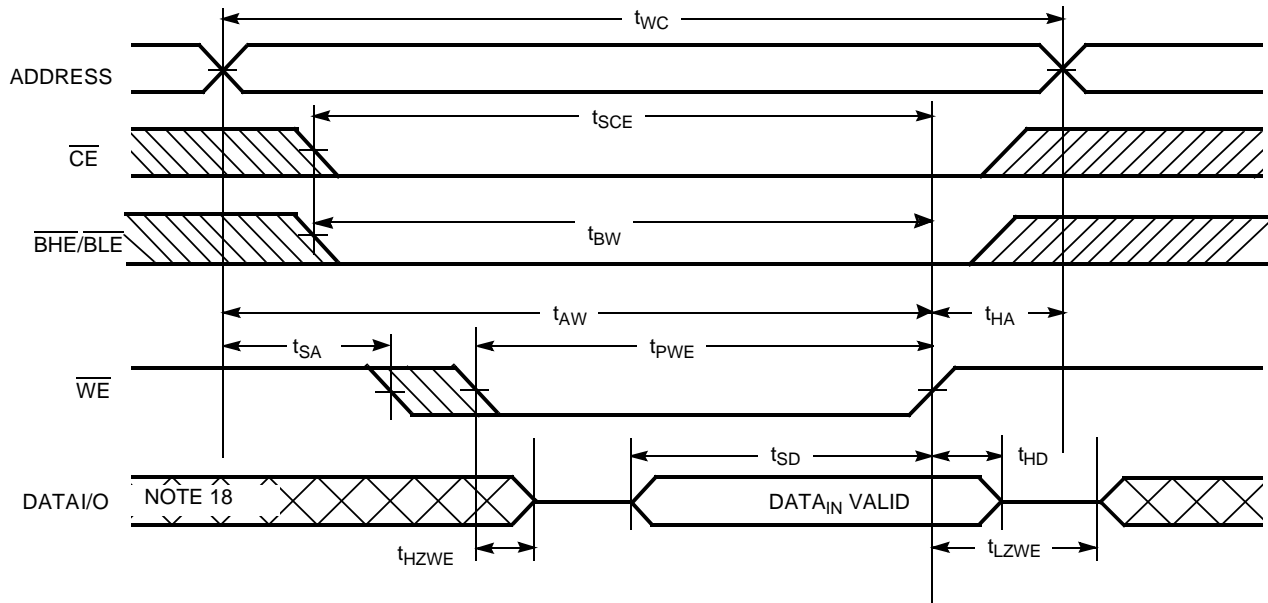
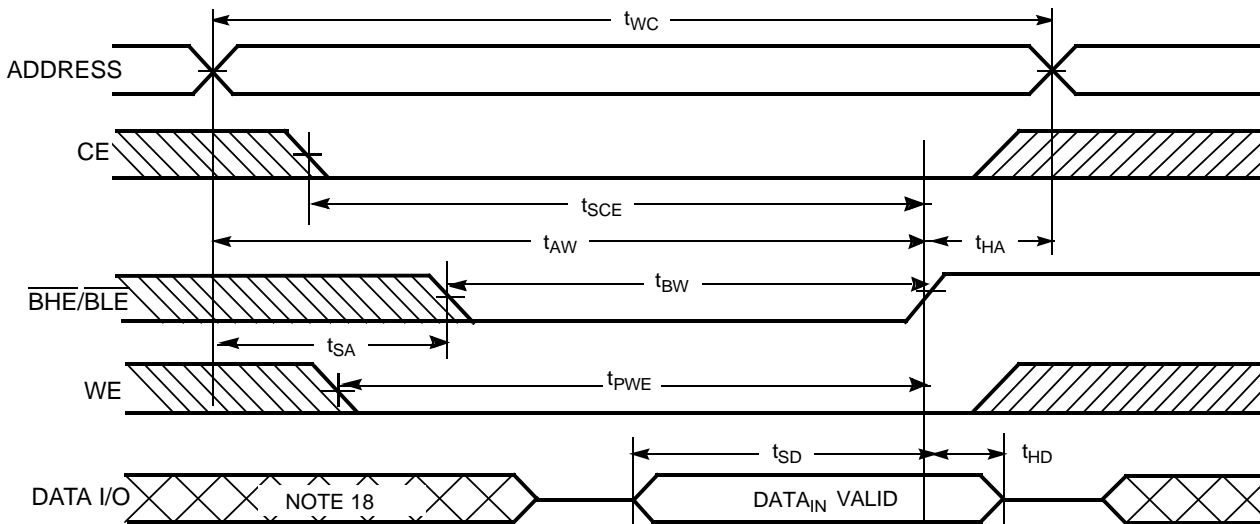
| Parameter  | Description                         | 55 ns |      | 70 ns |      | Unit |
|------------|-------------------------------------|-------|------|-------|------|------|
|            |                                     | Min.  | Max. | Min.  | Max. |      |
| $t_{AW}$   | Address Set-Up to Write End         | 45    |      | 60    |      | ns   |
| $t_{HA}$   | Address Hold from Write End         | 0     |      | 0     |      | ns   |
| $t_{SA}$   | Address Set-Up to Write Start       | 0     |      | 0     |      | ns   |
| $t_{PWE}$  | WE Pulse Width                      | 40    |      | 50    |      | ns   |
| $t_{BW}$   | BHE / BLE Pulse Width               | 45    |      | 60    |      | ns   |
| $t_{SD}$   | Data Set-Up to Write End            | 25    |      | 30    |      | ns   |
| $t_{HD}$   | Data Hold from Write End            | 0     |      | 0     |      | ns   |
| $t_{HZWE}$ | WE LOW to High Z <sup>[9, 11]</sup> |       | 25   |       | 25   | ns   |
| $t_{LZWE}$ | WE HIGH to Low Z <sup>[9]</sup>     | 5     |      | 5     |      | ns   |

**Switching Waveforms**
**Read Cycle No. 1 (Address Transition Controlled)<sup>[13, 14]</sup>**

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[14, 15]</sup>**

**Notes:**

13. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  =  $V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  =  $V_{IL}$ .
14.  $\overline{WE}$  is HIGH for read cycle.
15. Address valid prior to or coincident with  $\overline{CE}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled)** <sup>[12, 16, 17]</sup>

**Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)** <sup>[12, 16, 17]</sup>

**Notes:**

16. Data I/O is high-impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .
17. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in a high-impedance state.
18. During this period, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[17]</sup>**

**Write Cycle No. 4 ( $\overline{BHE/BLE}$  Controlled,  $\overline{OE}$  LOW)<sup>[17]</sup>**

**Truth Table**

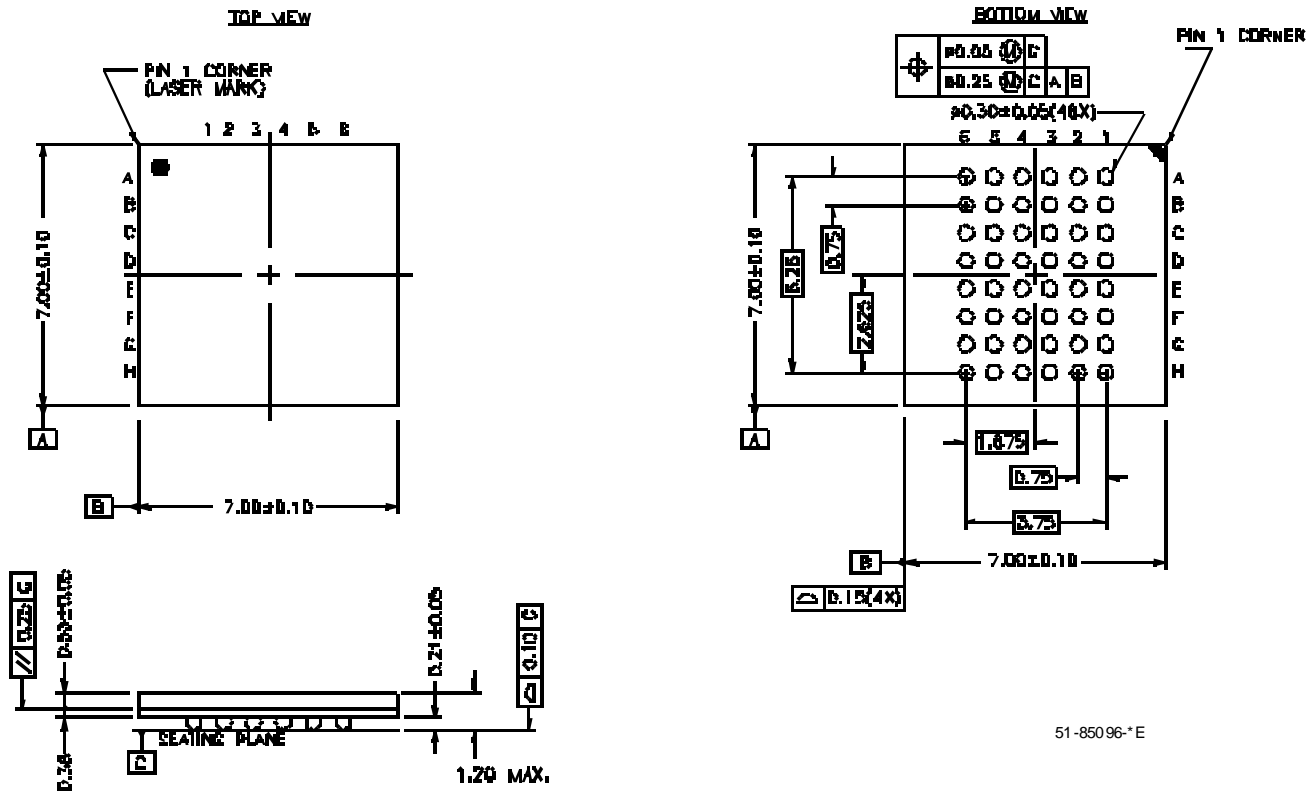
| CE | WE | OE | BHE | BLE | Inputs/Outputs   | Mode                | Power                |
|----|----|----|-----|-----|--|---------------------|----------------------|
| H  | X  | X  | X   | X   | High Z   | Deselect/Power-Down | Standby ( $I_{SB}$ ) |
| X  | X  | X  | H   | H   | High Z   | Deselect/Power-Down | Standby ( $I_{SB}$ ) |
| L  | H  | L  | L   | L   | Data Out (I/O <sub>0</sub> -I/O <sub>15</sub> )  | Read                | Active ( $I_{CC}$ )  |
| L  | H  | L  | H   | L   | Data Out (I/O <sub>0</sub> -I/O <sub>7</sub> );<br>I/O <sub>8</sub> -I/O <sub>15</sub> in High Z | Read                | Active ( $I_{CC}$ )  |
| L  | H  | L  | L   | H   | Data Out (I/O <sub>8</sub> -I/O <sub>15</sub> );<br>I/O <sub>0</sub> -I/O <sub>7</sub> in High Z | Read                | Active ( $I_{CC}$ )  |
| L  | H  | H  | L   | L   | High Z   | Output Disabled     | Active ( $I_{CC}$ )  |
| L  | H  | H  | H   | L   | High Z   | Output Disabled     | Active ( $I_{CC}$ )  |

**Truth Table** (continued)

| CE | WE | OE | BHE | BLE | Inputs/Outputs                                 | Mode                  | Power                     |
|----|----|----|-----|-----|--|-----------------------|---------------------------|
| L  | H  | H  | L   | H   | High Z   | Output Disabled       | Active (I <sub>CC</sub> ) |
| L  | L  | X  | L   | L   | Data In (I/O <sub>0</sub> -I/O <sub>15</sub> ) | Write                 | Active (I <sub>CC</sub> ) |
| L  | L  | X  | H   | L   | Data In (I/O <sub>0</sub> -I/O <sub>7</sub> )  | Write Lower Byte Only | Active (I <sub>CC</sub> ) |
| L  | L  | X  | L   | H   | Data In (I/O <sub>8</sub> -I/O <sub>15</sub> ) | Write Upper Byte Only | Active (I <sub>CC</sub> ) |

**Ordering Information**

| Speed (ns) | Ordering Code     | Package Name | Package Type                                  | Operating Range |
|------------|-------------------|--------------|---|-----------------|
| 55         | CY62127BVLL-55ZI  | Z44          | 44-lead TSOP II                               | Industrial      |
| 70         | CY62127BVLL-70ZI  |              |   |                 |
|            | CY62127BVLL-70BAI | BA48A        | 48-ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm) |                 |
|            | CY62127BVLL-70BVI | BV48A        | 48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)   |                 |

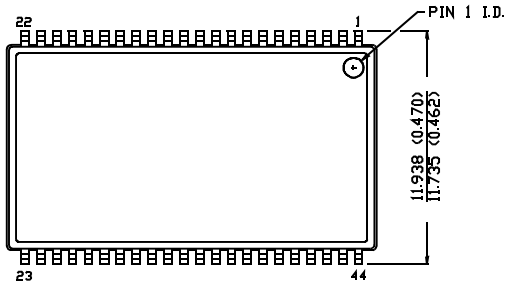
**Package Diagrams**
**48-Ball (7.00 mm x 7.00 mm x 1.2 mm) FBGA BA48A**




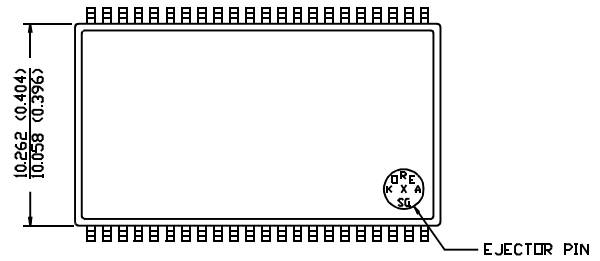
Package Diagrams (continued)

44-pin TSOP II Z44

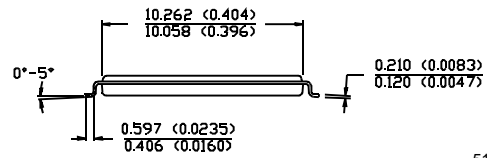
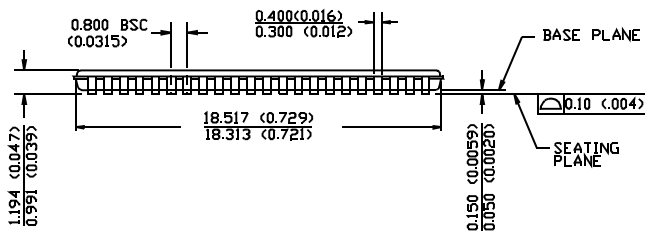
DIMENSION IN MM (INCH)  
MAX  
MIN



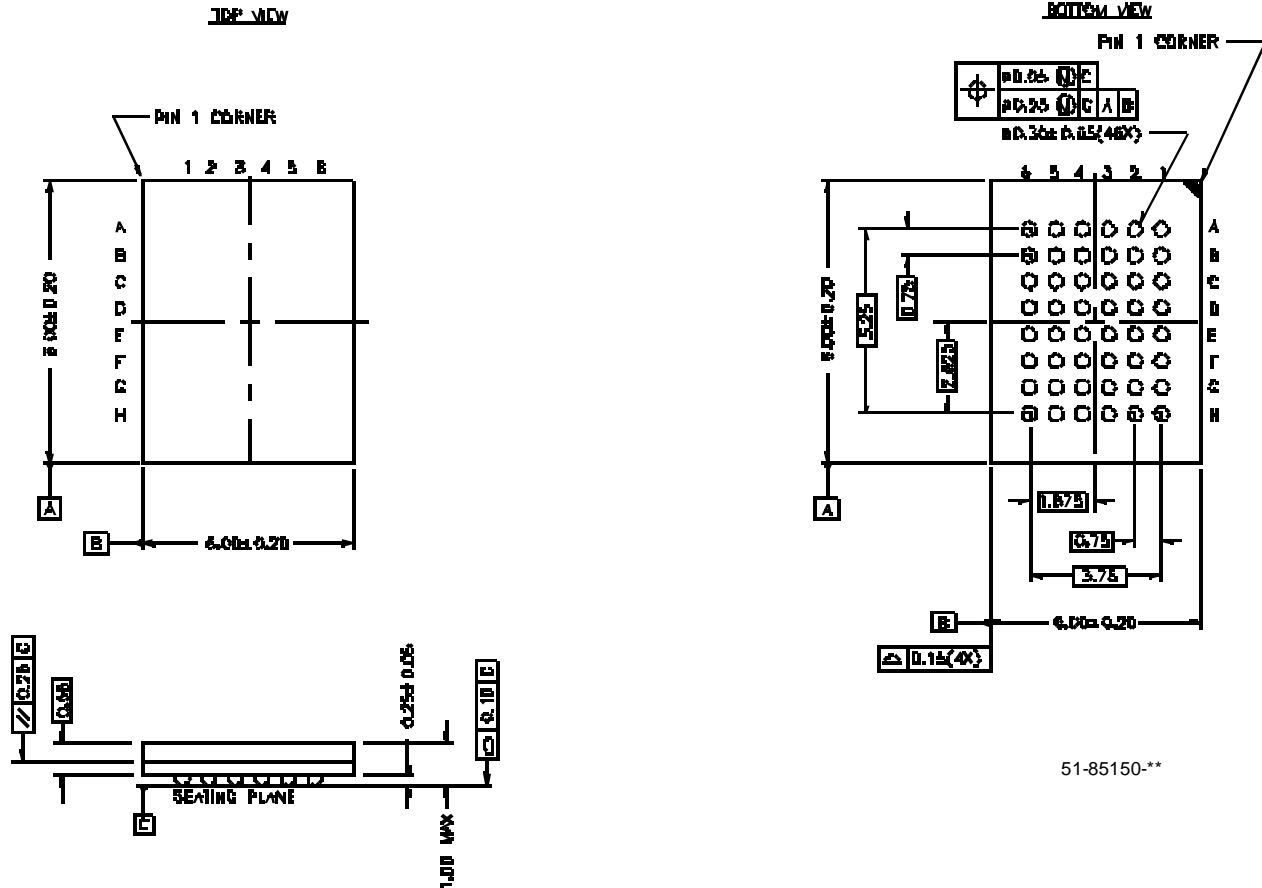
TOP VIEW



BOTTOM VIEW



51-85087-A

**Package Diagrams (continued)**
**48-Lead VFBGA (6 x 8 x 1 mm) BV48A**


51-85150-\*\*

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| Document Title: CY62127BV MoBL <sup>®</sup> 1M (64K x 16) Static RAM |         |            |                 |  |
|--|---------|------------|-----------------|--|
| Document Number: 38-05155  |         |            |                 |  |
| REV.   | ECN NO. | Issue Date | Orig. of Change | Description of Change                                |
| **   | 109899  | 10/02/01   | SZV             | Change from Spec number: 38-01018 to 38-05155        |
| *A   | 113307  | 03/01/02   | MGN             | Format standardization & update ordering information |
| *B   | 116362  | 09/04/02   | GBI             | Add footnote 1 and BV Package.                       |