4 MEG x 16 FPM DRAM

DRAM

MT4LC4M16F5

For the latest data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- Single +3.3V ±0.3V power supply
- Industry-standard x16 pinout, timing, functions, and packages
- 12 row, 10 column addresses
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are LVTTL-compatible
- FAST PAGE MODE (FPM) access
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) REFRESH distributed across 64ms

OPTIONS — MARKING

- Plastic Package
  50-pin TSOP (400 mil) — TG
- Timing
  50ns access — -5
  60ns access — -6
- Refresh Rate
  Standard Refresh — None

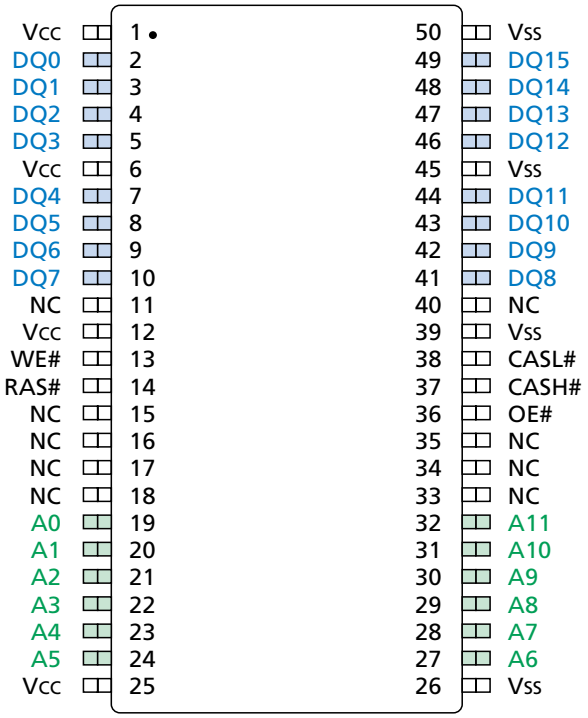
Part Number Example
MT4LC4M16F5TG-5

KEY TIMING PARAMETERS

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC
-5	90ns	50ns	30ns	25ns	13ns
-6	110ns	60ns	35ns	30ns	15ns

PIN ASSIGNMENT (Top View)

50-Pin TSOP



NOTE: 1. The # symbol indicates signal is active LOW.

GENERAL DESCRIPTION

The 4 Meg x 16 DRAM is a high-speed CMOS, dynamic random-access memory device containing 67,108,864 bits organized in a x16 configuration. The MT4LC4M16F5 is functionally organized as 4,194,304 locations containing 16 bits each. The 4,194,304 memory locations are arranged in 4,096 rows by 1,024 columns. During READ or WRITE cycles, each location is uniquely addressed via the address bits: 12 row-address bits (A0-A11) and 10 column-address bits (A0-A9). In addition, both byte and word accesses are supported via the two CAS# pins (CASL# and CASH#). The CAS# functionality and timing related to address and control functions (e.g., latching column addresses or selecting CBR REFRESH) are such that the internal CAS# signal is determined by the first external CAS# signal (CASL# or CASH#) to transition LOW and the last to transition back HIGH. The CAS# functionality and timing related to driving or latching data are such that each CAS# signal independently controls the associated eight DQ pins.

The row address is latched by the RAS# signal, then the column address by CAS#. The device provides FAST-PAGE-MODE operation, allowing for fast successive data operations (READ, WRITE, or READ-MODIFY-WRITE) within a given row.

The MT4LC4M16F5 must be refreshed periodically in order to retain stored data.

FAST PAGE MODE ACCESS

Each location in the DRAM is uniquely addressable, as mentioned in the General Description. Use of both CAS# signals results in a word access via the 16 I/O pins (DQ0-DQ15). Use of only one of the two results in a BYTE access cycle. CASL# transitioning LOW selects an access cycle for the lower byte (DQ0-DQ7), and CASH# transitioning LOW selects an access cycle for the upper byte (DQ8-DQ15). General byte and word access timing is shown in Figures 1 and 2.

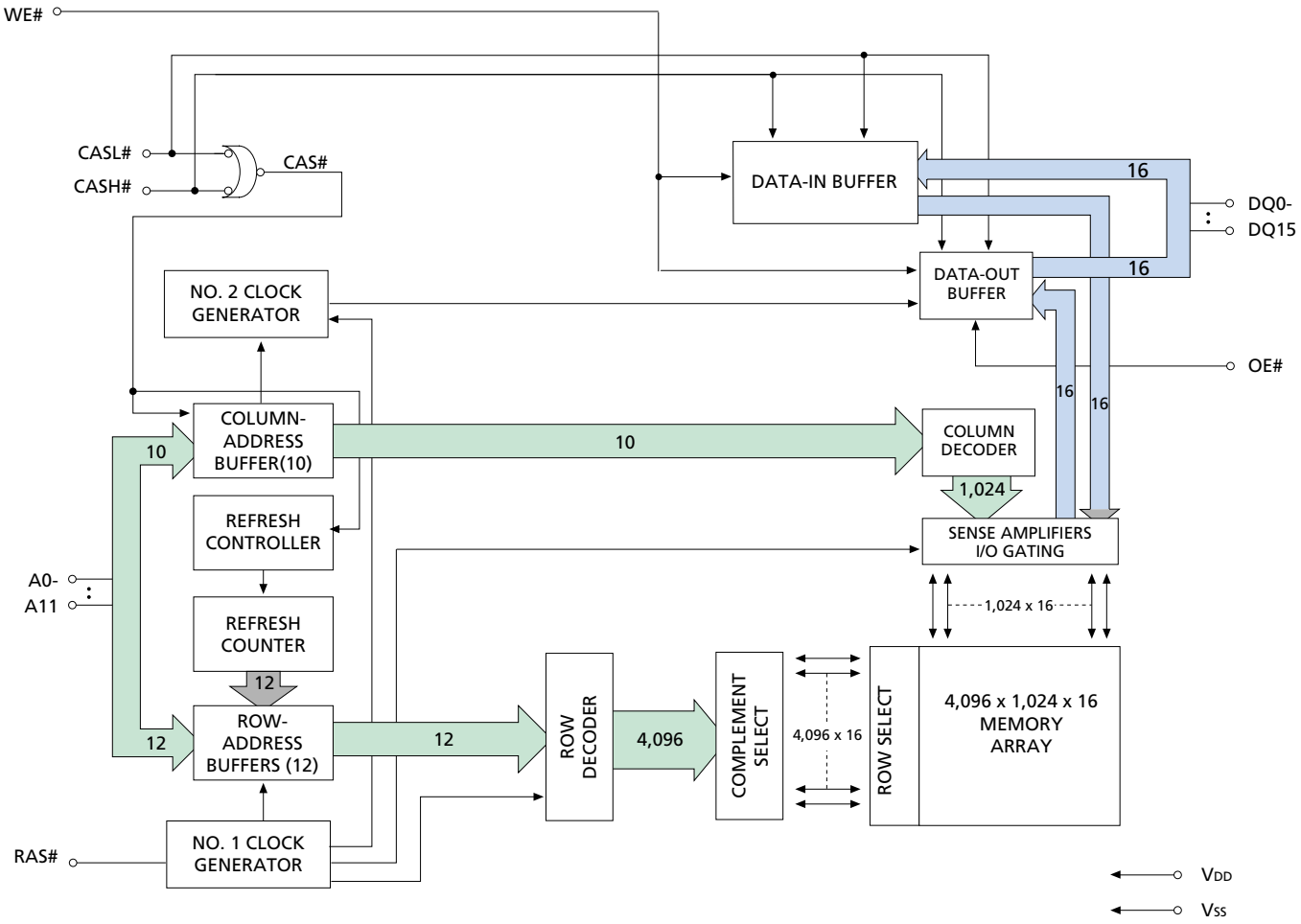
Additionally, both bytes must always be of the same mode of operation if both bytes are active. A CAS# precharge must be satisfied prior to changing modes of operation between the upper and lower bytes. For example, an EARLY WRITE on one byte and a LATE WRITE on the other byte are not allowed during the same cycle. However, an EARLY WRITE on one byte and a LATE WRITE on the other byte, after a CAS# precharge has been satisfied, are permissible.

The WE# signal must be activated to execute a WRITE operation; otherwise a READ operation will be performed. The OE# signal must be activated to enable the DQ output drivers for a read access and can be deactivated to disable output data if necessary.

FAST-PAGE-MODE operations are always initiated with a row address strobed in by the RAS# signal, followed by a column address strobed in by CAS#, just like for single location accesses. However, subsequent column locations within the row may then be accessed at the page mode cycle time. This is accomplished by cycling CAS# while holding RAS# LOW and entering new column addresses with each CAS# cycle. Returning RAS# HIGH terminates the FAST-PAGE-MODE operation.

FUNCTIONAL BLOCK DIAGRAM

MT4LC4M16F5 (12 row addresses)



DRAM REFRESH

The supply voltage must be maintained at the specified levels, and the refresh requirements must be met in order to retain stored data in the DRAM. The refresh requirements are met by refreshing all rows in the DRAM array at least once every 64ms. The recommended procedure is to execute 4,096 CBR REFRESH cycles, either uniformly spaced or grouped in bursts, every 64ms. The MT4LC4M16F5 internally refreshes one row for every CBR cycle, so executing 4,096 CBR cycles covers all rows. The CBR REFRESH will invoke the internal refresh counter for automatic RAS# addressing. Alternatively, RAS#-ONLY REFRESH capability is inherently provided. However, with this method some compatibility issues may become apparent. JEDEC strongly recommends the use of CBR REFRESH for this device.

STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the RAS# HIGH time.

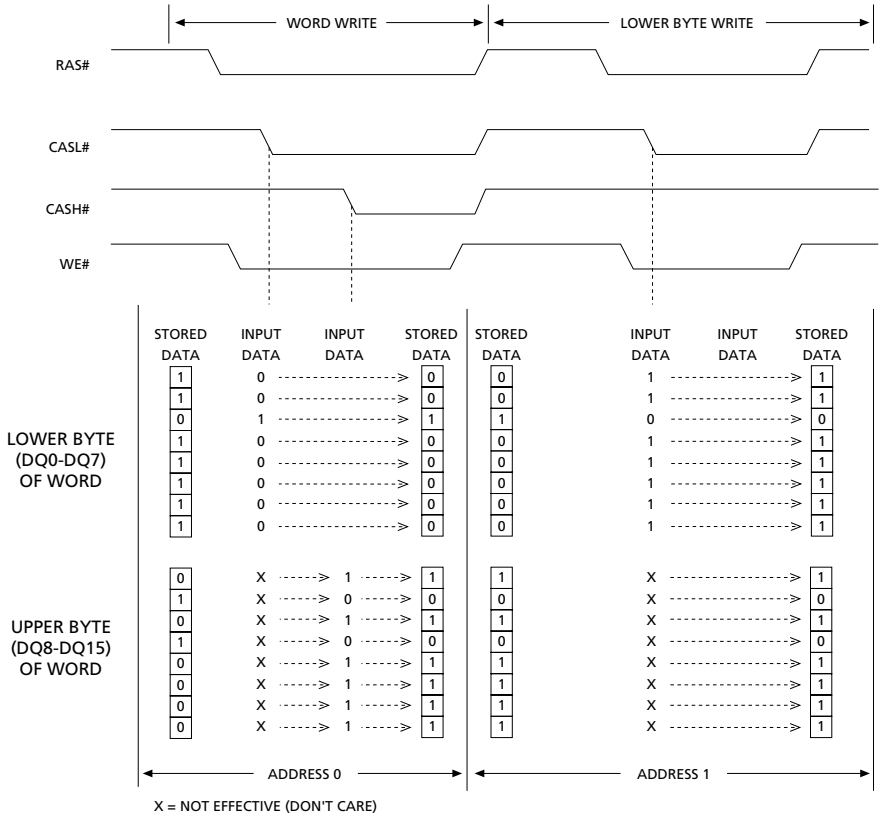


Figure 1
WORD and BYTE WRITE Example

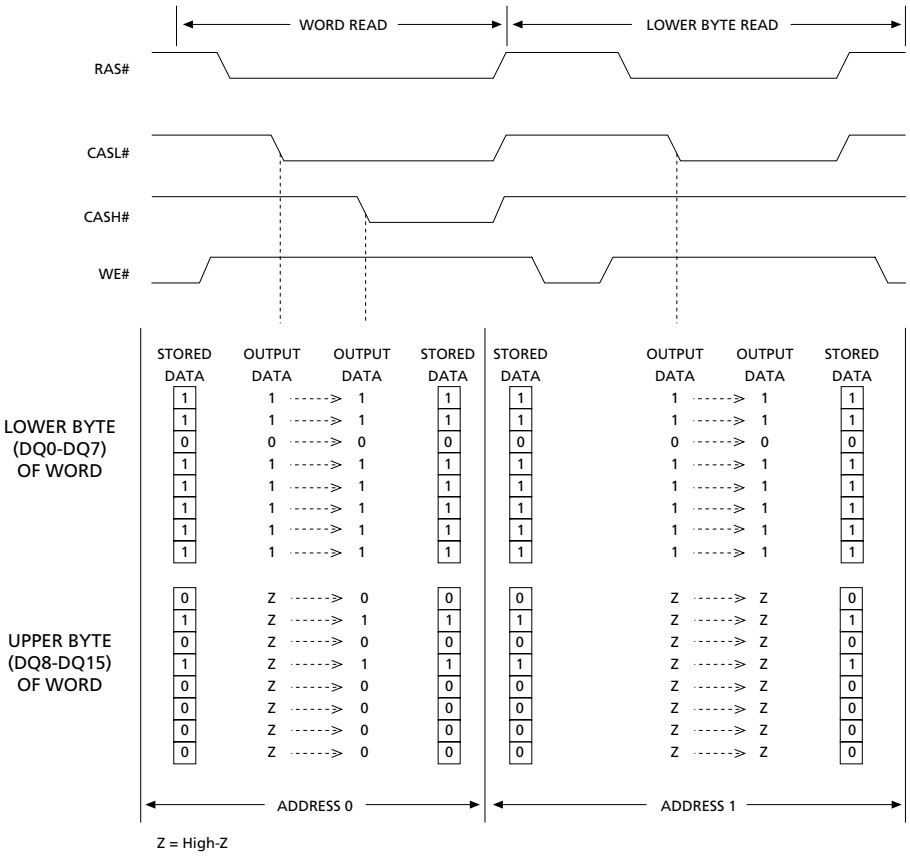


Figure 2
WORD and BYTE READ Example

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Relative to V_{SS} ..... -1V to +4.6V
Voltage on NC, Inputs or I/O Pins
Relative to V_{SS} ..... -1V to +4.6V
Operating Temperature, T_A (ambient) ... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 5, 6) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{CC}	3	3.6	V	
INPUT HIGH VOLTAGE: Valid Logic 1; All inputs, I/Os and any NC	V_{IH}	2	V_{CC} + 0.3	V	37
INPUT LOW VOLTAGE: Valid Logic 0; All inputs, I/Os and any NC	V_{IL}	-0.3	0.8	V	37
INPUT LEAKAGE CURRENT: Any input at V_{IN} (0V ≤ V_{IN} ≤ V_{CC} + 0.3V); All other pins not under test = 0V	I_I	-2	2	µA	
OUTPUT HIGH VOLTAGE: I_{OUT} = -2mA	V_{OH}	2.4	–	V	
OUTPUT LOW VOLTAGE: I_{OUT} = 2mA	V_{OL}	–	0.4	V	
OUTPUT LEAKAGE CURRENT: Any output at V_{OUT} (0V ≤ V_{OUT} ≤ V_{CC} + 0.3V); DQ is disabled and in High-Z state	I_{OZ}	-5	5	µA	

I_{DD} OPERATING CONDITIONS AND MAXIMUM LIMITS

(Notes: 1, 2, 3, 5, 6) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SPEED	MAX	UNITS	NOTES
STANDBY CURRENT: TTL (RAS# = CAS# = V_{IH})	I_{DD1}	ALL	1	mA	
STANDBY CURRENT: CMOS (RAS# = CAS# ≥ V_{CC} - 0.2V; DQs may be left open; Other inputs: V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V)	I_{DD2}	ALL	500	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: ^tRC = ^tRC [MIN])	I_{DD3}	-5 -6	150 165	mA	25
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^tPC = ^tPC [MIN])	I_{DD4}	-5 -6	105 95	mA	25
REFRESH CURRENT: RAS# ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: ^tRC = ^tRC [MIN])	I_{DD5}	-5 -6	150 165	mA	22
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^tRC = ^tRC [MIN])	I_{DD6}	-5 -6	150 165	mA	4, 7

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS
Input Capacitance: Address pins	C_{I1}	5	pF
Input Capacitance: RAS#, CAS#, WE#, OE#	C_{I2}	7	pF
Input/Output Capacitance: DQ	C_{IO}	7	pF

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column address	^tAA		25		30	ns	
Column-address hold time (referenced to RAS#)	^tAR	40		45		ns	
Column-address setup time	^tASC	0		0		ns	26
Row-address setup time	^tASR	0		0		ns	
Column address to WE# delay time	^tAWD	48		55		ns	18
Access time from CAS#	^tCAC		13		15	ns	28
Column-address hold time	^tCAH	8		10		ns	26
CAS# pulse width	^tCAS	13	10,000	15	10,000	ns	32, 34
CAS# hold time (CBR Refresh)	^tCHR	15		15		ns	4, 27
Last CAS# going LOW to first CAS# to return HIGH	^tCLCH	5		5		ns	29
CAS# to output in Low-Z	^tCLZ	3		3		ns	26, 28
CAS# precharge time (FAST PAGE MODE)	^tCP	8		10		ns	13, 32
Access time from CAS# precharge	^tCPA		30		35	ns	27
CAS# to RAS# precharge time	^tCRP	5		5		ns	27
CAS# hold time	^tCSH	50		60		ns	27
CAS# setup time (CBR Refresh)	^tCSR	5		5		ns	4, 26
CAS# to WE# delay time	^tCWD	36		40		ns	18, 26
WRITE command to CAS# lead time	^tCWL	13		15		ns	28
Data-in hold time	^tDH	8		10		ns	19, 28
Data-in setup time	^tDS	0		0		ns	19, 28
Output disable	^tOD	3	13	3	15	ns	23, 24, 36
Output enable time	^tOE		13		15	ns	20
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^tOEH	13		15		ns	24
Output buffer turn-off delay	^tOFF	3	13	3	15	ns	17, 23, 28
OE# setup prior to RAS# during HIDDEN REFRESH cycle	^tORD	0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	30		35		ns	30
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	76		85		ns	30
Access time from RAS#	^tRAC		50		60	ns	
RAS# to column-address delay time	^tRAD	13		15		ns	15
Row-address hold time	^tRAH	8		10		ns	

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
RAS# pulse width	^{t}RAS	50	10,000	60	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	^{t}RASP	50	125,000	60	125,000	ns	
Random READ or WRITE cycle time	^{t}RC	90		110		ns	
RAS# to CAS# delay time	^{t}RCD	18		20		ns	14, 26
READ command hold time (referenced to CAS#)	^{t}RCH	0		0		ns	16, 27
READ command setup time	^{t}RCS	0		0		ns	26
Refresh period	^{t}REF		64		64	ms	22
RAS# precharge time	^{t}RP	30		40		ns	
RAS# to CAS# precharge time	^{t}RPC	0		0		ns	
READ command hold time (referenced to RAS#)	^{t}RRH	0		0		ns	16
RAS# hold time	^{t}RSH	13		15		ns	35
READ-WRITE cycle time	^{t}RWC	131		155		ns	
RAS# to WE# delay time	^{t}RWD	73		85		ns	18
WRITE command to RAS# lead time	^{t}RWL	13		15		ns	
Transition time (rise or fall)	^{t}T	2	50	2	50	ns	
WRITE command hold time	^{t}WCH	8		10		ns	35
WRITE command hold time (referenced to RAS#)	^{t}WCR	40		45		ns	
WE# command setup time	^{t}WCS	0		0		ns	18, 26
WRITE command pulse width	^{t}WP	8		10		ns	
WE# hold time (CBR Refresh)	^{t}WRH	10		10		ns	
WE# setup time (CBR Refresh)	^{t}WRP	10		10		ns	

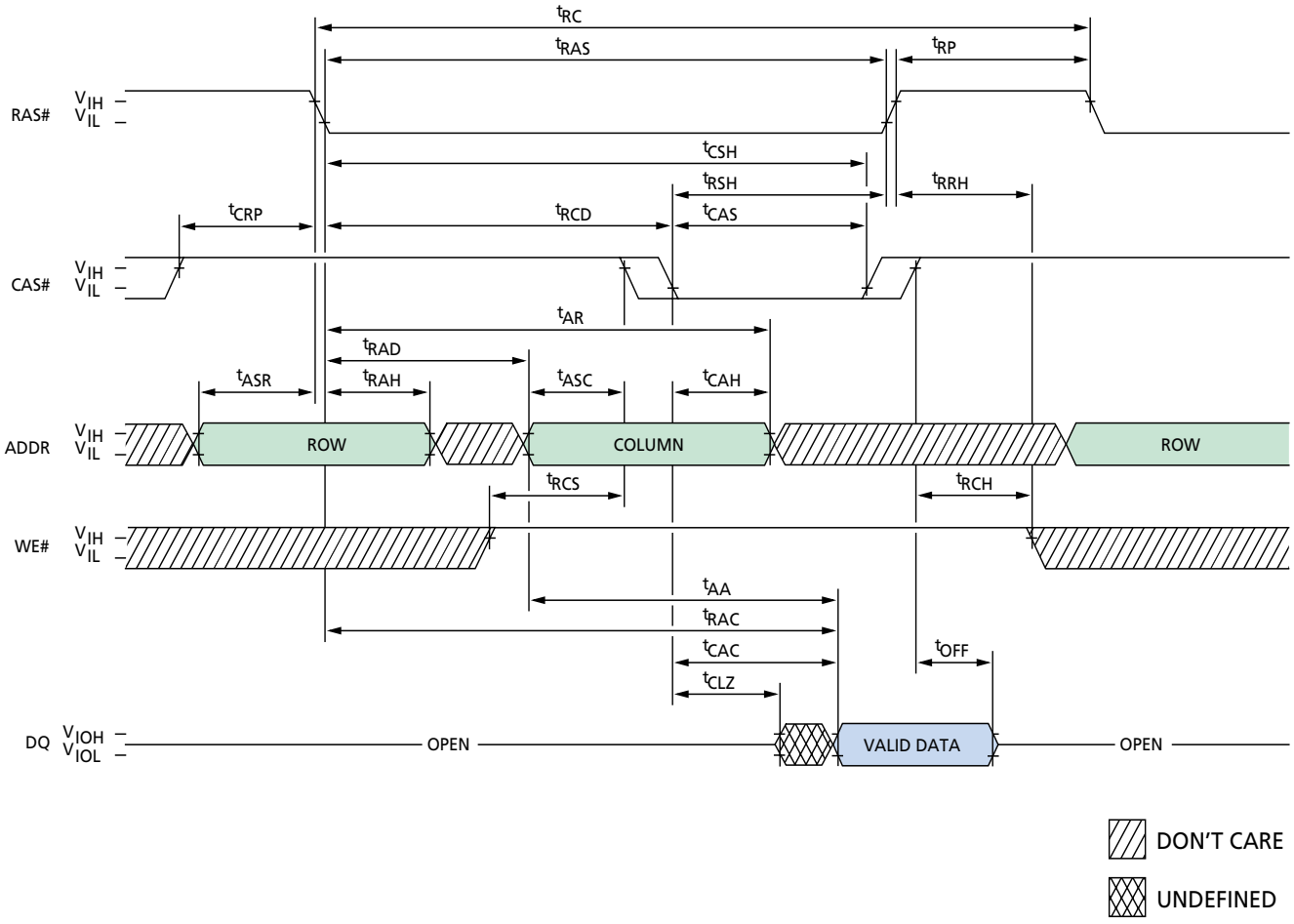
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V; f = 1 MHz.
3. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 5ns.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH}, data output is High-Z.
11. If CAS# = V_{IL}, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates, 100pF and V_{OL} = 0.8V and V_{OH} = 2V.
13. If CAS# is LOW at the falling edge of RAS#, output data will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ^{t}CP.
14. The ^{t}RCD (MAX) limit is no longer specified. ^{t}RCD (MAX) was specified as a reference point only. If ^{t}RCD was greater than the specified ^{t}RCD (MAX) limit, then access time was controlled exclusively by ^{t}CAC (^{t}RAC [MIN] no longer applied). With or without the ^{t}RCD limit, ^{t}AA and ^{t}CAC must always be met.
15. The ^{t}RAD (MAX) limit is no longer specified. ^{t}RAD (MAX) was specified as a reference point only. If ^{t}RAD was greater than the specified ^{t}RAD (MAX) limit, then access time was controlled exclusively by ^{t}AA (^{t}RAC and ^{t}CAC no longer applied). With or without the ^{t}RAD (MAX) limit, ^{t}AA, ^{t}RAC, and ^{t}CAC must always be met.
16. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
17. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
18. ^{t}WCS, ^{t}RWD, ^{t}AWD, and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. If ^{t}WCS > ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. ^{t}RWD, ^{t}AWD and ^{t}CWD define READ-MODIFY-WRITE cycles. Meeting these limits allows for reading and disabling output data and then applying input data. The values shown were calculated for reference allowing 10ns for the external latching of read data and application of write data. OE# held HIGH and WE# taken LOW after CAS# goes LOW result in a LATE WRITE (OE#-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD, and ^{t}AWD are not applicable in a LATE WRITE cycle.
19. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
20. If OE# is tied permanently LOW, LATE WRITE, or READ-MODIFY-WRITE operations are not possible.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
22. RAS#-ONLY REFRESH requires that all 4,096 rows be refreshed at least once every 64ms. CBR REFRESH requires that at least 4,096 cycles be completed every 64ms.
23. The DQs go High-Z during READ cycles once ^{t}OD or ^{t}OFF occur. If CAS# goes HIGH before OE#, the DQs will go High-Z regardless of the state of OE#. If CAS# stays LOW while OE# is brought HIGH, the DQs will go High-Z. If OE# is brought back LOW (CAS# still LOW), the DQs will provide the previously read data.
24. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If OE# is taken back LOW while CAS# remains LOW, the DQs will remain open.
25. Column address changed once each cycle.
26. The first CASx# edge to transition LOW.
27. The last CASx# edge to transition HIGH.
28. Output parameter (DQx) is referenced to corresponding CAS# input; DQ0-DQ7 by CASL# and DQ8-DQ15 by CASH#.
29. Last falling CASx# edge to first rising CASx# edge.

NOTES (continued)

30. Last rising CASx# edge to next cycle's last rising CASx# edge.
31. Last rising CASx# edge to first falling CASx# edge.
32. First DQs controlled by the first CASx# to go LOW.
33. Last DQs controlled by the last CASx# to go HIGH.
34. Each CASx# must meet minimum pulse width.
35. Last CASx# to go LOW.
36. All DQs controlled, regardless CASL# and CASH#.
37. V_{IH} overshoot: V_{IH} (MAX) = V_{CC} + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate.

READ CYCLE

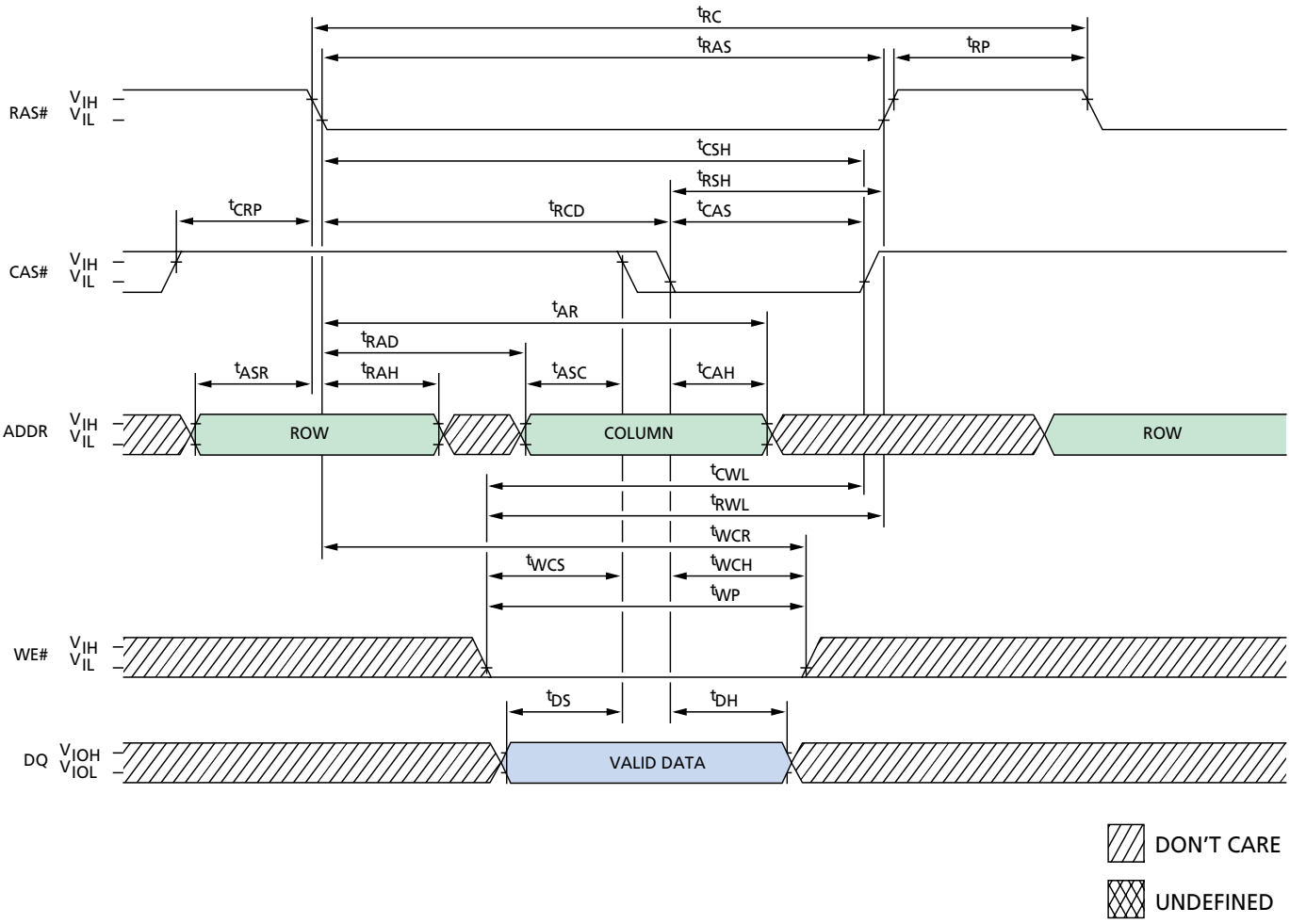


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	40		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	13	10,000	15	10,000	ns
tCLCH	5		5		ns
tCLZ	3		3		ns
tCRP	5		5		ns
tCSH	50		60		ns
tOD	3	13	3	15	ns
tOE		13		15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOFF	3	13	3	15	ns
tRAC		50		60	ns
tRAD	13		15		ns
tRAH	8		10		ns
tRAS	50	10,000	60	10,000	ns
tRC	90		110		ns
tRCD	18		20		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

EARLY WRITE CYCLE



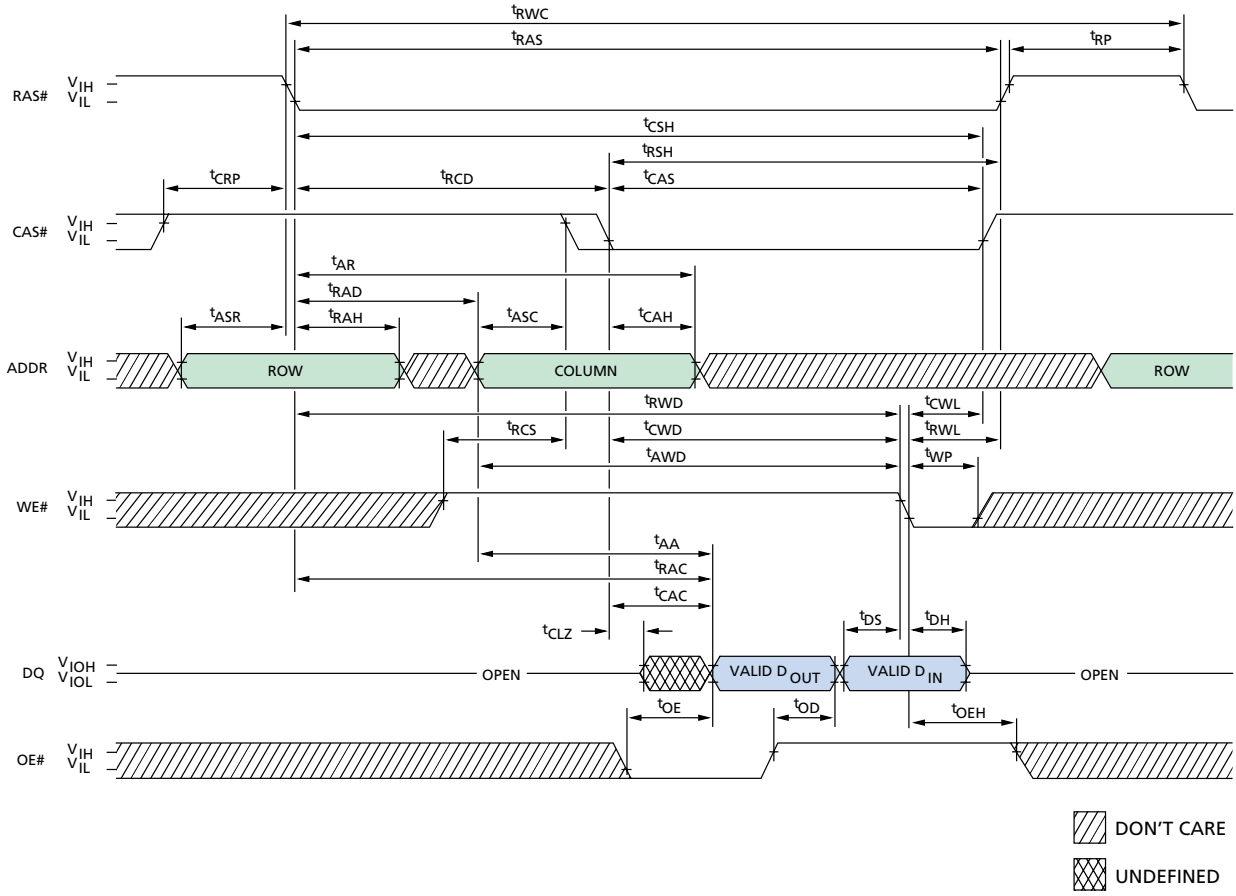
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAR	40		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS	13	10,000	15	10,000	ns
tCLCH	5		5		ns
tCRP	5		5		ns
tCSH	50		60		ns
tCWL	13		15		ns
tDH	8		10		ns
tDS	0		0		ns
tRAD	13		15		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRAH	8		10		ns
tRAS	50	10,000	60	10,000	ns
tRC	90		110		ns
tRCD	18		20		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR	40		45		ns
tWCS	0		0		ns
tWP	8		10		ns

READ-WRITE CYCLE

(LATE WRITE and READ-MODIFY-WRITE cycles)

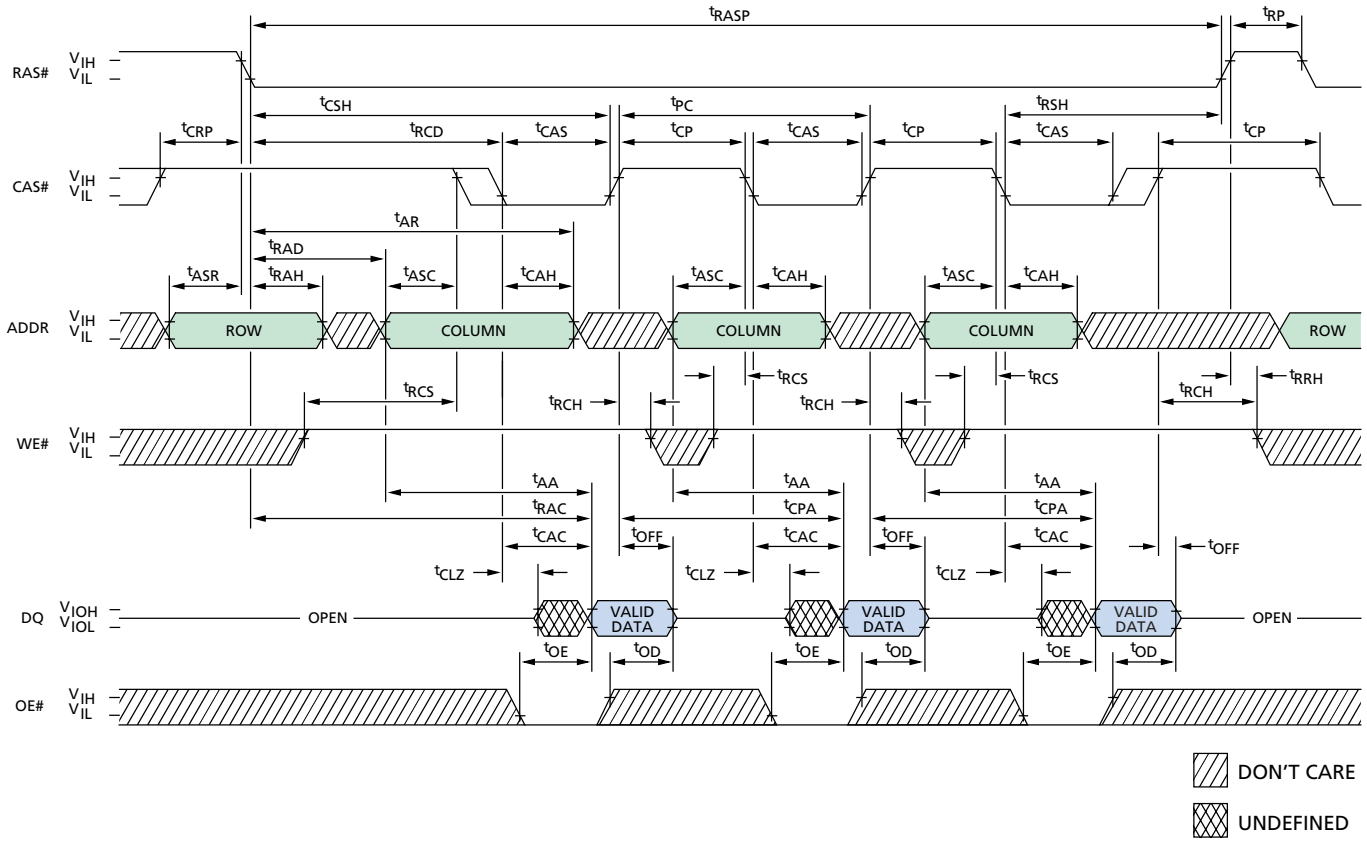


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	40		45		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	48		55		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	13	10,000	15	10,000	ns
tCLCH	5		5		ns
tCLZ	3		3		ns
tCRP	5		5		ns
tCSH	50		60		ns
tCWD	36		40		ns
tCWL	13		15		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOD	3	13	3	15	ns
tOE		13		15	ns
tOEH	13		15		ns
tRAC		50		60	ns
tRAD	13		15		ns
tRAH	8		10		ns
tRAS	50	10,000	60	10,000	ns
tRCD	18		20		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWC	131		155		ns
tRWD	73		85		ns
tRWL	13		15		ns
tWP	8		10		ns

FAST-PAGE-MODE READ CYCLE

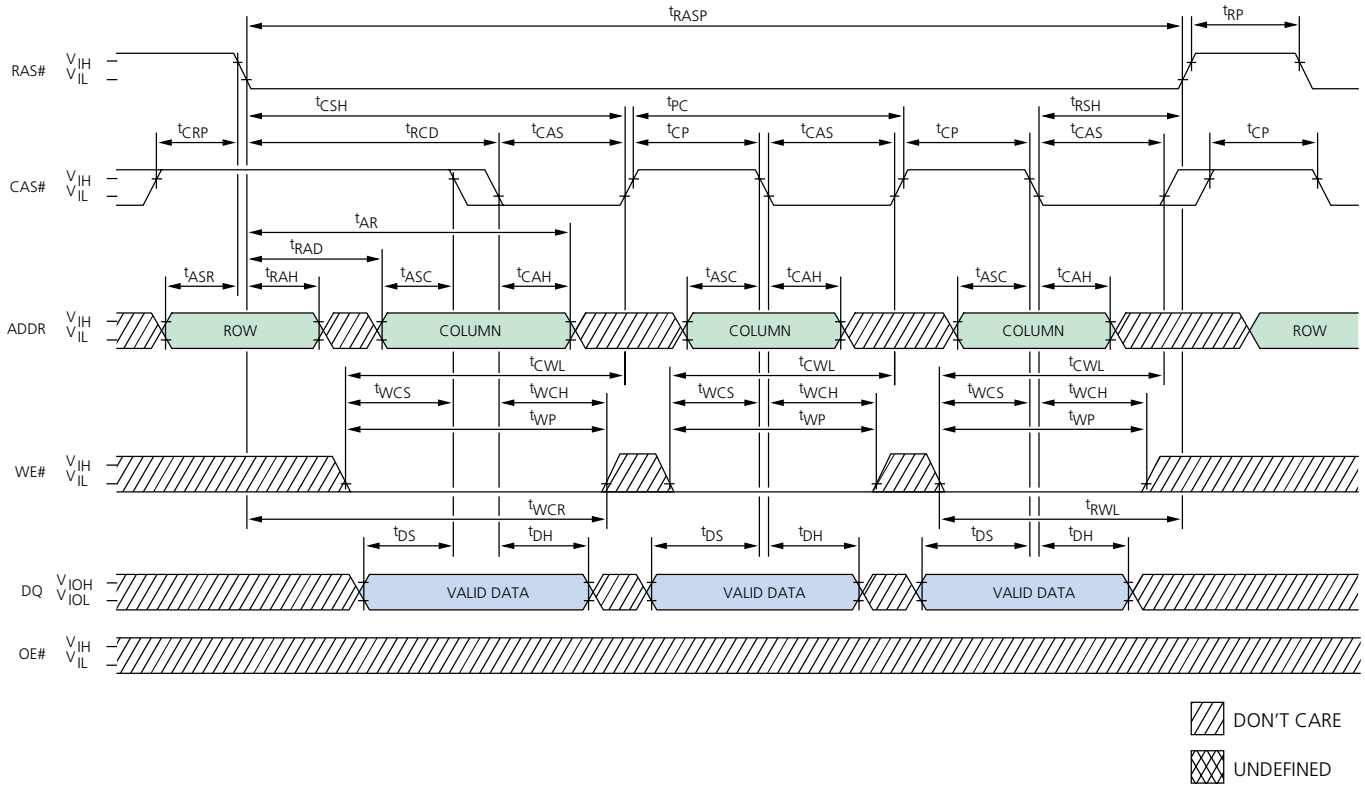


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	40		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	13	10,000	15	10,000	ns
tCLCH	5		5		ns
tCLZ	3		3		ns
tCP	8		10		ns
tCPA		30		35	ns
tCRP	5		5		ns
tCSH	50		60		ns
tOD	3	13	3	15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE		13		15	ns
tOFF	3	13	3	15	ns
tPC	30		35		ns
tRAC		50		60	ns
tRAD	13		15		ns
tRAH	8		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	18		20		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

FAST-PAGE-MODE EARLY WRITE CYCLE



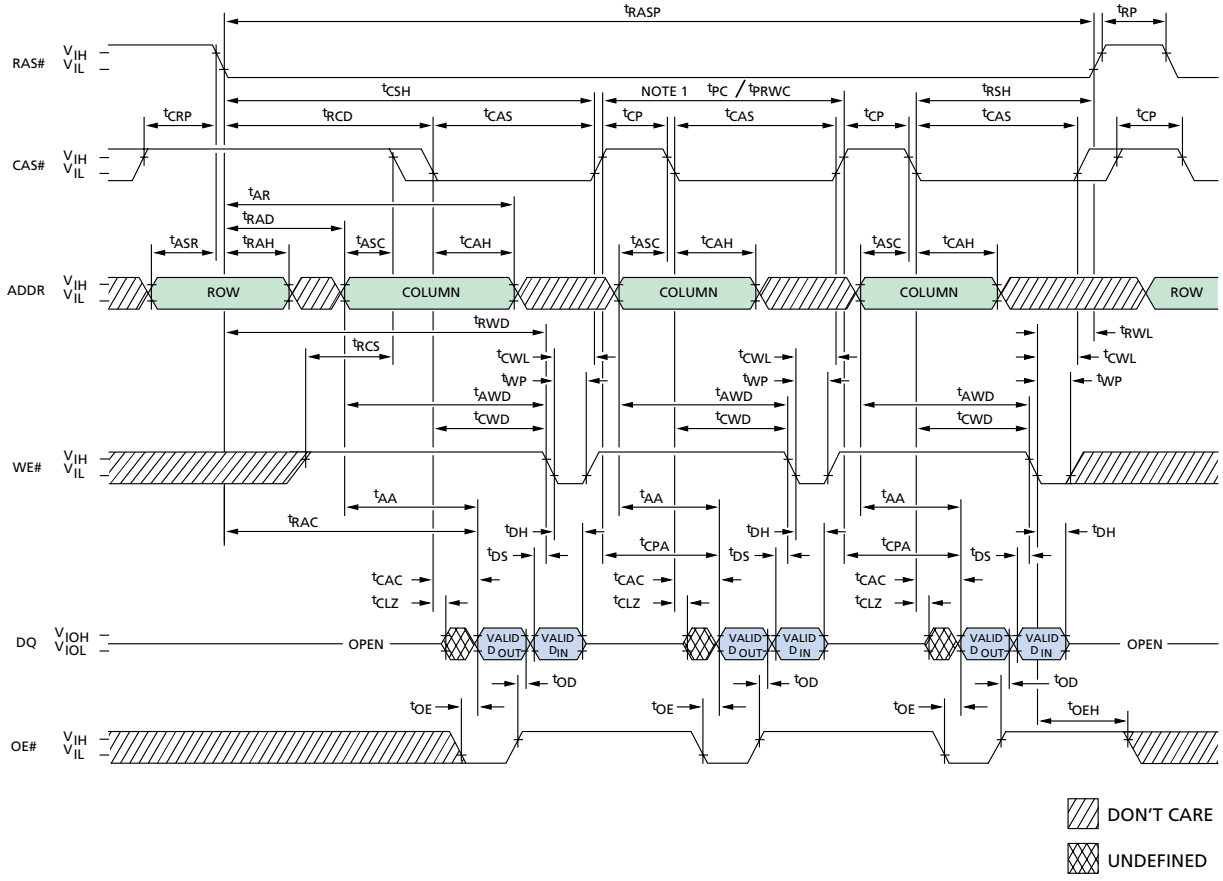
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAR	40		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS	13	10,000	15	10,000	ns
tCLCH	5		5		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSH	50		60		ns
tCWL	13		15		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tPC	30		35		ns
tRAD	13		15		ns
tRAH	8		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	18		20		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR	40		45		ns
tWCS	0		0		ns
tWP	8		10		ns

FAST-PAGE-MODE READ-WRITE CYCLE

(LATE WRITE and READ-MODIFY-WRITE cycles)



TIMING PARAMETERS

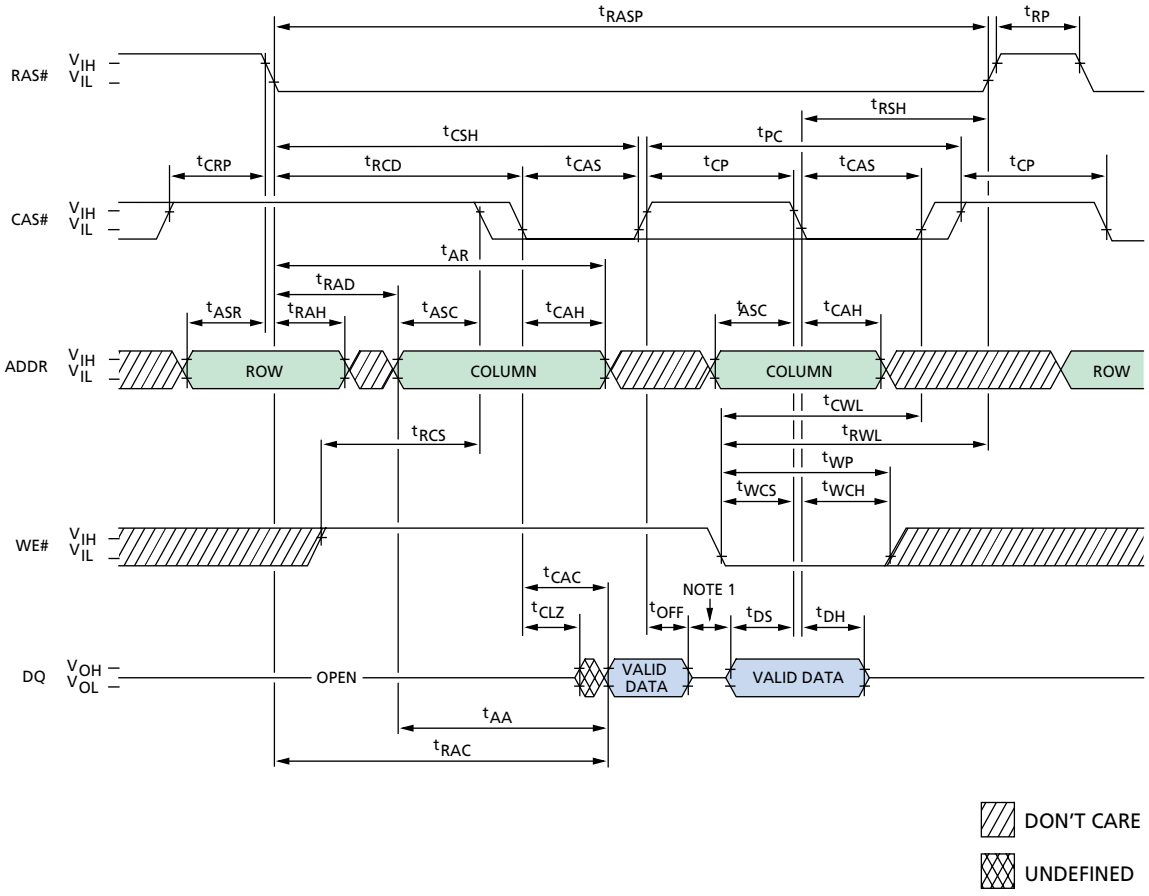
SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	40		45		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	48		55		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	13	10,000	15	10,000	ns
tCLCH	5		5		ns
tCLZ	3		3		ns
tCP	8		10		ns
tCPA		30		35	ns
tCRP	5		5		ns
tCSH	50		60		ns
tCWD	36		40		ns
tCWL	13		15		ns
tDH	8		10		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tDS	0		0		ns
tOD	3	13	3	15	ns
tOE		13		15	ns
tOEH	13		15		ns
tPC	30		35		ns
tPRWC	76		85		ns
tRAC		50		60	ns
tRAD	13		15		ns
tRAH	8		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	18		20		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWD	73		85		ns
tRWL	13		15		ns
tWP	8		10		ns

NOTE: 1. tPC is for LATE WRITE only.

FAST-PAGE-MODE READ EARLY WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



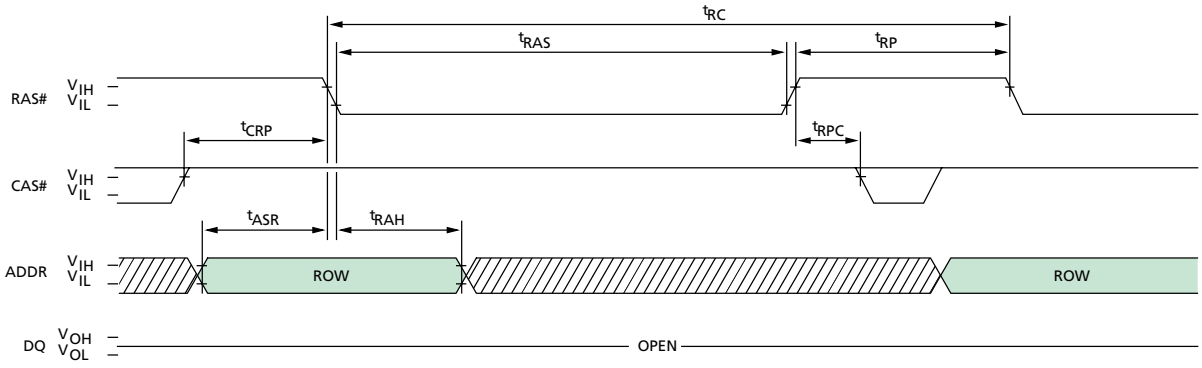
TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tAA		25		30	ns
tAR	40		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	13	10,000	15	10,000	ns
tCLZ	3		3		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSH	50		60		ns
tCWL	13		15		ns
tDH	8		10		ns
tDS	0		0		ns

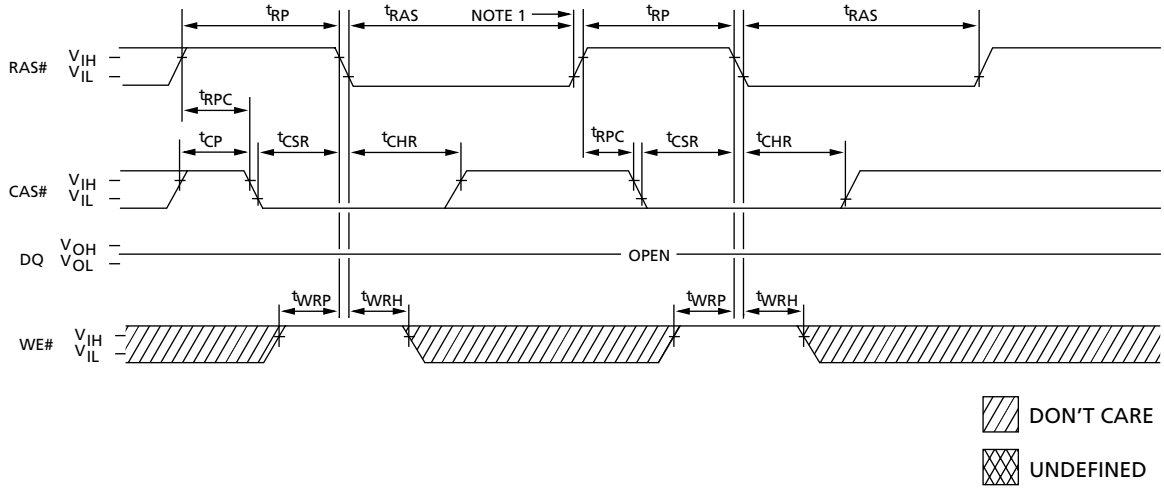
SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tOFF	3	13	3	15	ns
tPC	30		35		ns
tRAC		50		60	ns
tRAD	13		15		ns
tRAH	8		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	18		20		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCS	0		0		ns
tWP	8		10		ns

NOTE: 1. Do not drive input data prior to output data going High-Z.

RAS#-ONLY REFRESH CYCLE
(OE# and WE# = DON'T CARE)



CBR REFRESH CYCLE
(Addresses and OE# = DON'T CARE)



TIMING PARAMETERS

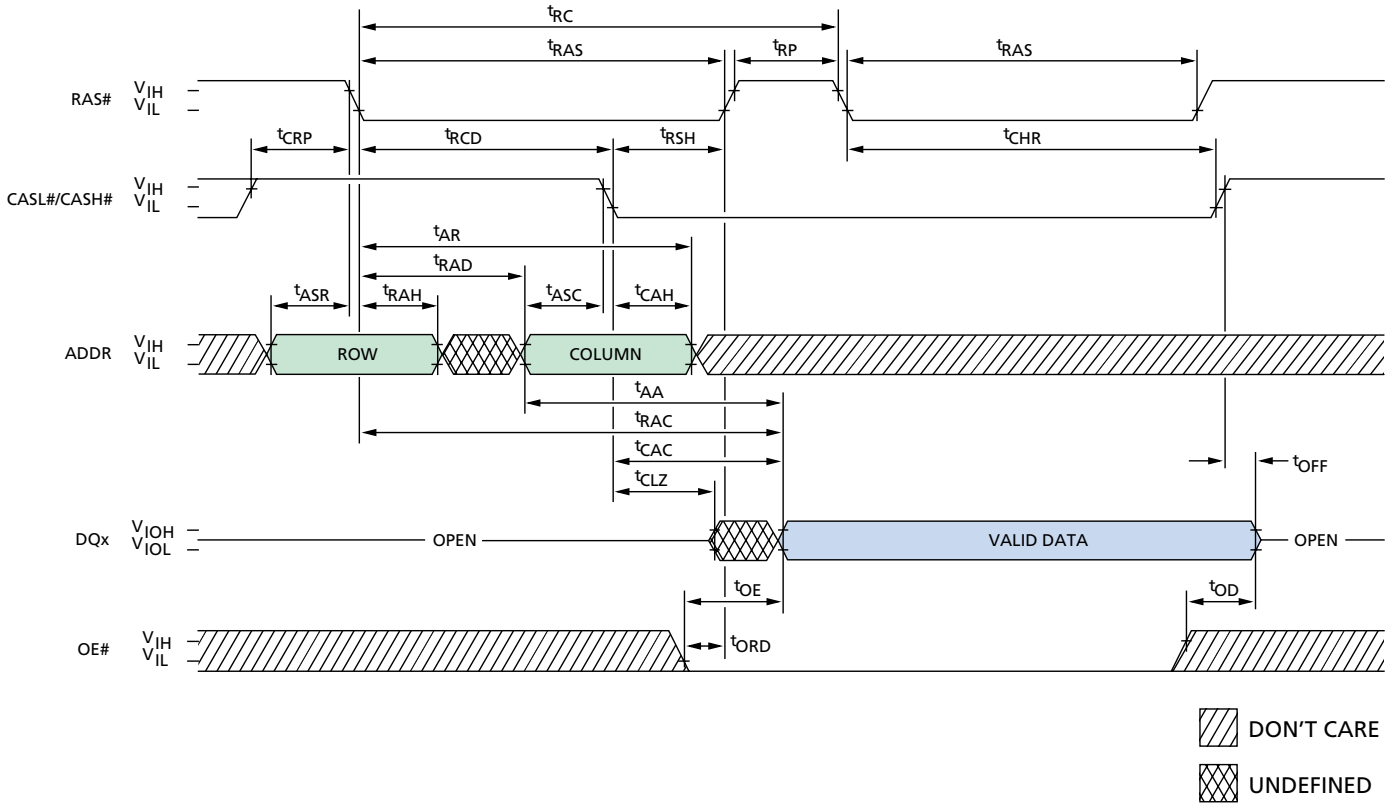
SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tASR	0		0		ns
tCHR	15		15		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSR	5		5		ns
tRAH	8		10		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRAS	50	10,000	60	10,000	ns
tRC	90		110		ns
tRP	30		40		ns
tRPC	0		0		ns
tWRH	10		10		ns
tWRP	10		10		ns

NOTE: 1. End of first CBR REFRESH cycle.

HIDDEN REFRESH CYCLE [1]

(WE# = HIGH; OE# = LOW)



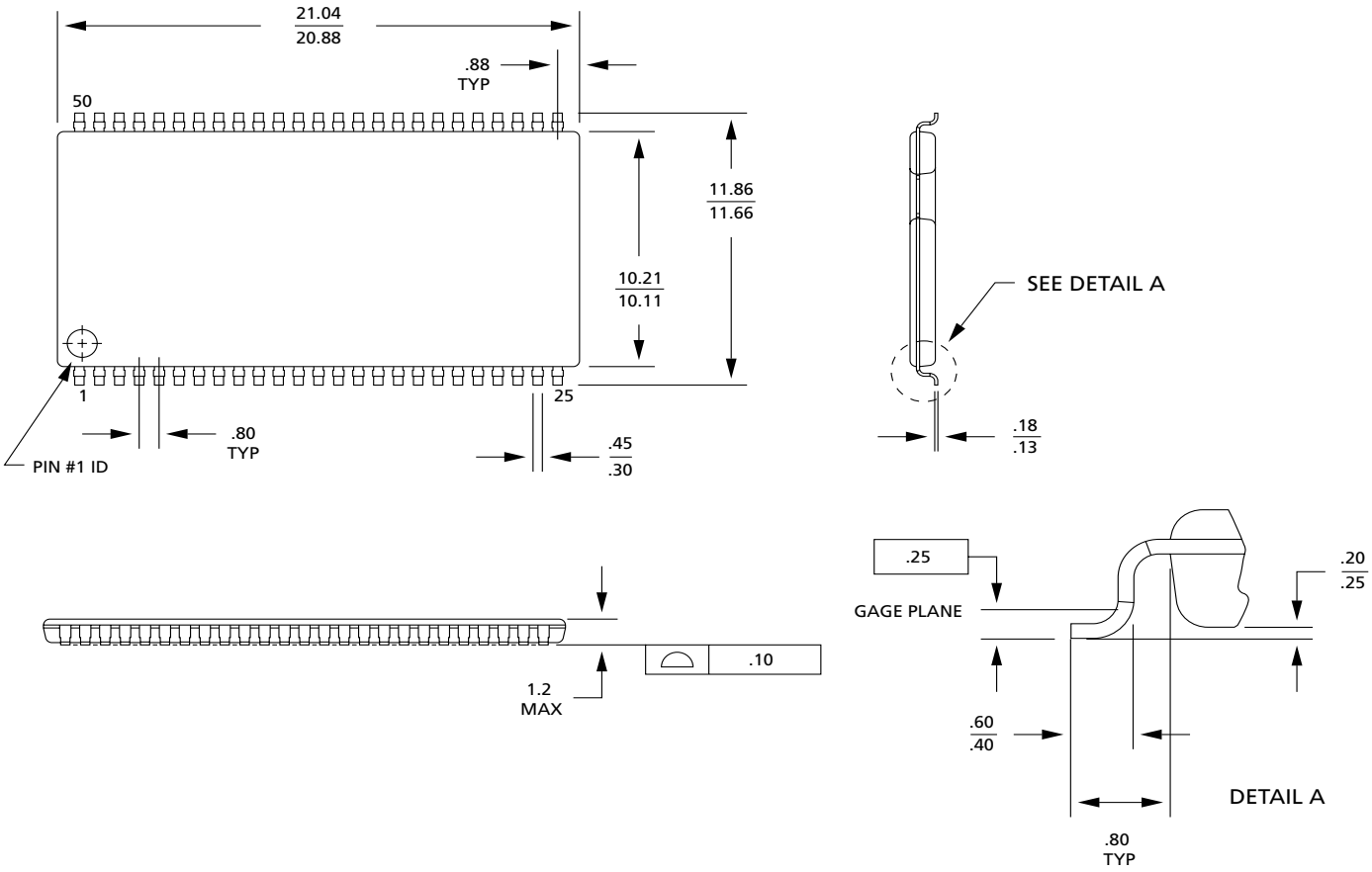
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	40		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCHR	15		15		ns
tCLZ	3		3		ns
tCRP	5		5		ns
tOD	3	13	3	15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE		13		15	ns
tOFF	3	13	3	15	ns
tORD	0		0		ns
tRAC		50		60	ns
tRAD	13		15		ns
tRAH	8		10		ns
tRAS	50	10,000	60	10,000	ns
tRCD	18		20		ns
tRP	30		40		ns
tRSH	13		15		ns

NOTE: 1. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# is LOW and OE# is HIGH.

50-PIN PLASTIC TSOP (400 mil)



NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .25mm per side.

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