PRELIMINARY

3 VOLT FlashFile™ MEMORY

28F004S3, 28F008S3, 28F016S3 (x8)

- **SmartVoltage Technology**
  - **2.7 V (Read-Only) or 3.3 V V_{CC} and 3.3 V or 12 V V_{PP}**
- **High-Performance**
  - **120 ns Read Access Time**
- **Enhanced Data Protection Features**
  - **Absolute Protection with V_{PP} = GND**
  - **Flexible Block Locking**
  - **Block Write Lockout during Power Transitions**
- **Enhanced Automated Suspend Options**
  - **Program Suspend to Read**
  - **Block Erase Suspend to Program**
  - **Block Erase Suspend to Read**
- **Industry-Standard Packaging**
  - **40-Lead TSOP, 44-Lead PSOP**
- **High-Density 64-Kbyte Symmetrical Erase Block Architecture**
  - **4 Mbit: Eight Blocks**
  - **8 Mbit: Sixteen Blocks**
  - **16 Mbit: Thirty-Two Blocks**
- **Extended Cycling Capability**
  - **100,000 Block Erase Cycles**
- **Low Power Management**
  - **Deep Power-Down Mode**
  - **Automatic Power Savings Mode Decreases I_{CC} in Static Mode**
- **Automated Program and Block Erase**
  - **Command User Interface**
  - **Status Register**
- **SRAM-Compatible Write Interface**
- **ETOX™ V Nonvolatile Flash Technology**

The Intel® 3 Volt FlashFile™ memory family renders a variety of density offerings in the same package. The 4-, 8-, and 16-Mbit 3 Volt FlashFile memories provide high-density, low-cost, nonvolatile, read/write storage solutions for a wide range of applications. Their symmetrically-blocked architecture, flexible voltage, and extended cycling provide highly flexible components suitable for resident flash arrays, SIMMs, and memory cards. Enhanced suspend capabilities provide an ideal solution for code or data storage applications. For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the 4-, 8-, and 16-Mbit FlashFile memories offer three levels of protection: absolute protection with V_{PP} at GND, selective hardware block locking, or flexible software block locking. These alternatives give designers ultimate control of their code security needs.

This family of products is manufactured on Intel® 0.4 µm ETOX™ V process technology. They come in industry-standard packages: the 40-lead TSOP, ideal for board-constrained applications, and the rugged 44-lead PSOP. Based on the 28F008SA architecture, the 3 Volt FlashFile memory family enables quick and easy upgrades for designs that demand state-of-the-art technology.

NOTE: This document formerly known as *Byte-Wide Smart 3 FlashFile™ Memory Family 4, 8, and 16 Mbit*.

December 1998

Order Number: 290598-005

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PRELIMINARY

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REVISION HISTORY

Number	Description
-001	Original version
-002	Table 3 revised to reflect change in abbreviations from “W” for write to “P” for program. Ordering information graphic (Appendix A) corrected: from PB = Ext. Temp. 44-Lead PSOP to **TB** = Ext. Temp. 44-Lead PSOP Updated Ordering Information and table Correction to table, Section 6.2.3. Under I_{LO} Test Conditions, previously read $V_{IN} = V_{CC}$ or GND, corrected to $V_{OUT} = V_{CC}$ or GND Section 6.2.7, modified Program and Block Erase Suspend Latency Times
-003	Updated disclaimer
-004	Added 2.7 V V_{PP} specifications Added µBGA* CSP pinouts and corrected error in PSOP pinout Added Design Consideration for V_{PP} Program and Erase Voltages on future sub-0.4µ devices
-005	Added maximum Block Erase time for 2.7 V operation Name of document changed from *Byte-Wide Smart 3 FlashFile™ Memory Family 4, 8, and 16 Mbit*

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1.0 INTRODUCTION

This datasheet contains 4-, 8-, and 16-Mbit 3 Volt FlashFile memory specifications. Section 1.0 provides a flash memory overview. Sections 2.0, 3.0, 4.0, and 5.0 describe the memory organization and functionality. Section 6.0 covers electrical specifications for commercial and extended temperature product offerings. Ordering information is provided in Section 7.0. Finally, the 3 Volt FlashFile memory family documentation also includes application notes and design tools which are referenced in Section 8.0.

1.1 New Features

The 3 Volt FlashFile memory family maintains backwards-compatibility with Intel® 28F008SA-L. Key enhancements include:

- SmartVoltage Technology
- Enhanced Suspend Capabilities
- In-System Block Locking

They share a compatible status register, software commands, and pinouts. These similarities enable a clean upgrade from the 28F008SA-L to 3 Volt FlashFile products. When upgrading, it is important to note the following differences:

- Because of new feature and density options, the devices have different device identifier codes. This allows for software optimization.
- V_{PPLK} has been lowered from 6.5 V to 1.5 V to support low V_{PP} voltages during block erase, program, and lock-bit configuration operations. Designs that switch V_{PP} off during read operations should transition V_{PP} to GND.
- To take advantage of SmartVoltage technology, allow V_{PP} connection to 3.3 V.

For more details see application note *AP-625, 28F008SC Compatibility with 28F008SA* (order number 292180).

1.2 Product Overview

The 3 Volt FlashFile memory family provides density upgrades with pinout compatibility for the 4- , 8-, and 16-Mbit densities. The 28F004S3, 28F008S3, and 28F016S3 are high-performance memories arranged as 512 Kbyte, 1 Mbyte, and 2 Mbyte of eight bits. This data is grouped in eight, sixteen, and thirty-two 64-Kbyte blocks which are individually erasable, lockable, and unlockable in-system. Figure 5 illustrates the memory organization.

SmartVoltage technology enables fast factory programming and low power designs. Specifically designed for 3 V systems, 3 Volt FlashFile components support read operations at 2.7 V and 3.3 V V_{CC} and block erase and program operations at 2.7 V, 3.3 V and 12 V V_{PP}. The 12 V V_{PP} option renders the fastest program performance which will increase your factory throughput. With the 2.7 V or 3.3 V V_{PP} option, V_{CC} and V_{PP} can be tied together for a simple, low-power 2.7 V or 3 V design. In addition to the voltage flexibility, the dedicated V_{PP} pin gives complete data protection when $V_{PP} \leq V_{PPLK}$.

Internal V_{PP} detection circuitry automatically configures the device for optimized block erase and program operations.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, program, and lock-bit configuration operations.

A block erase operation erases one of the device's 64-Kbyte blocks typically within 1.1 second (12 V V_{PP}), independent of other blocks. Each block can be independently erased 100,000 times (1.6 million block erases per device). A block erase suspend operation allows system software to suspend block erase to read data from or program data to any other block.

Data is programmed in byte increments typically within 7.6 µs (12 V V_{PP}). A program suspend operation permits system software to read data or execute code from any other flash memory array location.

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To protect programmed data, each block can be locked. This block locking mechanism uses a combination of bits, block lock-bits and a master lock-bit, to lock and unlock individual blocks. The block lock-bits gate block erase and program operations, while the master lock-bit gates block lock-bit configuration operations. Lock-bit configuration operations (Set Block Lock-Bit, Set Master Lock-Bit, and Clear Block Lock-Bits commands) set and clear lock-bits.

The status register and RY/BY# output indicate whether or not the device is busy executing or ready for a new command. Polling the status register, system software retrieves WSM feedback. The RY/BY# output gives an additional indicator of WSM activity by providing a hardware status signal. Like the status register, RY/BY#-low indicates that the WSM is performing a block erase, program, or lock-bit configuration operation. RY/BY#-high indicates that the WSM is ready for a new command, block erase is suspended, program is suspended, or the device is in deep power-down mode.

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical I_{CCR} current is 3 mA.

When CE# and RP# pins are at V_{CC}, the component enters a CMOS standby mode. Driving RP# to GND enables a deep power-down mode which significantly reduces power consumption, provides write protection, resets the device, and clears the status register. A reset time (t_{PHQV}) is required from RP# switching high until outputs are valid. Likewise, the device has a wake time (t_{PHEL}) from RP#-high until writes to the CUI are recognized.

1.3 Pinout and Pin Description

The family of devices is available in 40-lead TSOP (Thin Small Outline Package, 1.2 mm thick), 44-lead PSOP (Plastic Small Outline Package) and 40-bump µBGA* CSP (28F008S3 and 28F016S3 only). Pinouts are shown in Figures 2, 3 and 4.

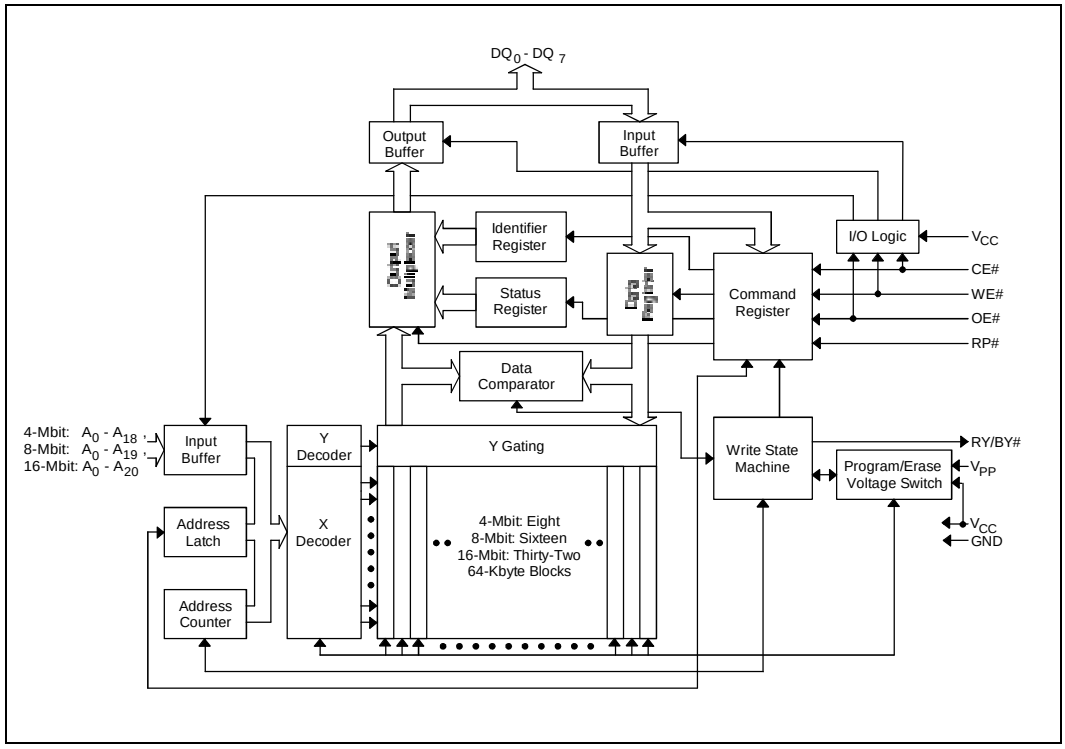

Figure 1. Block Diagram

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Table 1. Pin Descriptions

Sym	Type	Name and Function
A_0–A_{20}	INPUT	**ADDRESS INPUTS:** Inputs for addresses during read and write operations. Addresses are internally latched during a write cycle. 4 Mbit → A_0–A_{18} 8 Mbit → A_0–A_{19} 16 Mbit → A_0–A_{20}
DQ_0–DQ_7	INPUT/ OUTPUT	**DATA INPUT/OUTPUTS:** Inputs data and commands during CUI write cycles; outputs data during memory array, status register, and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle.
CE#	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders, and sense amplifiers. CE#-high deselects the device and reduces power consumption to standby levels.
RP#	INPUT	**RESET/DEEP POWER-DOWN:** When driven low, RP# inhibits write operations which provides data protection during power transitions, puts the device in deep power-down mode, and resets internal automation. RP#-high enables normal operation. Exit from deep power-down sets the device to read array mode. RP# at V_{HH} enables setting of the master lock-bit and enables configuration of block lock-bits when the master lock-bit is set. RP# = V_{HH} overrides block lock-bits, thereby enabling block erase and program operations to locked memory blocks. Block erase, program, or lock-bit configuration with V_{IH} < RP# < V_{HH} produce spurious results and should not be attempted.
OE#	INPUT	**OUTPUT ENABLE:** Gates the device's outputs during a read cycle.
WE#	INPUT	**WRITE ENABLE:** Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the WE# pulse.
RY/BY#	OUTPUT	**READY/BUSY#:** Indicates the status of the internal WSM. When low, the WSM is performing an internal operation (block erase, program, or lock-bit). RY/BY#-high indicates that the WSM is ready for new commands, block erase or program is suspended, or the device is in deep power-down mode. RY/BY# is always active.
V_{PP}	SUPPLY	**BLOCK ERASE, PROGRAM, LOCK-BIT CONFIGURATION POWER SUPPLY:** For erasing array blocks, programming data, or configuring lock-bits. 3 Volt Flash → 2.7 V, 3.3 V and 12 V V_{PP} With $V_{PP} \le V_{PPLK}$, memory contents cannot be altered. Block erase, program, and lock-bit configuration with an invalid V_{PP} (see *DC Characteristics*) produce spurious results and should not be attempted.
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY:** Internal detection automatically configures the device for optimized read performance. Do not float any power pins. 3 Volt Flash → 2.7 V and 3.3 V V_{CC} With $V_{CC} \le V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltages (see *DC Characteristics*) produce spurious results and should not be attempted. Block erase, program, and lock-bit configuration operations with V_{CC} < 2.7 V are not supported.
GND	SUPPLY	**GROUND:** Do not float any ground pins.
NC		**NO CONNECT:** Lead is not internally connected; it may be driven or floated.

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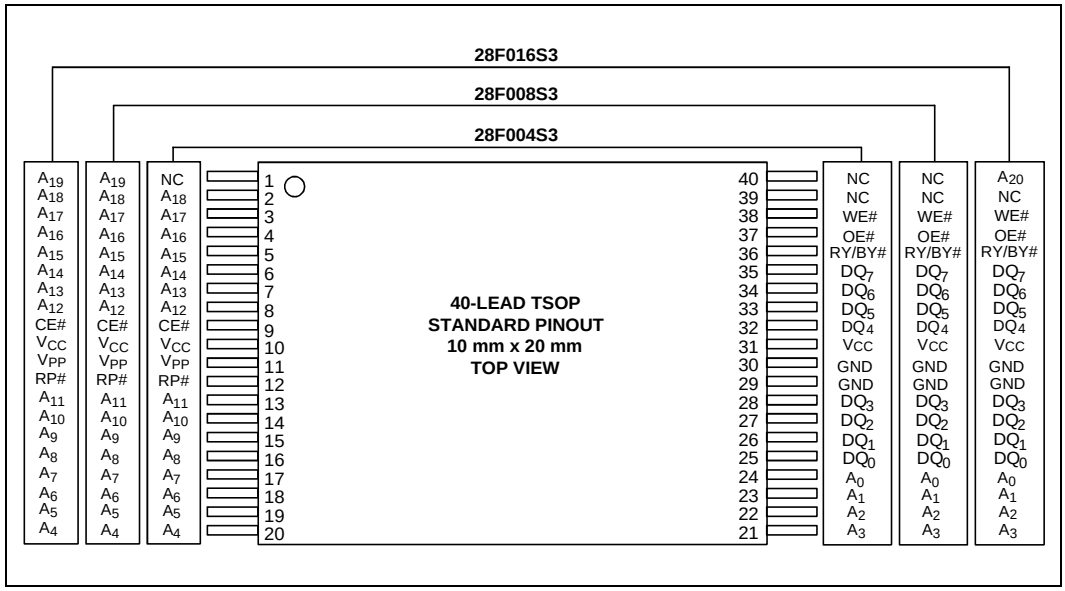

Figure 2. TSOP 40-Lead Pinout

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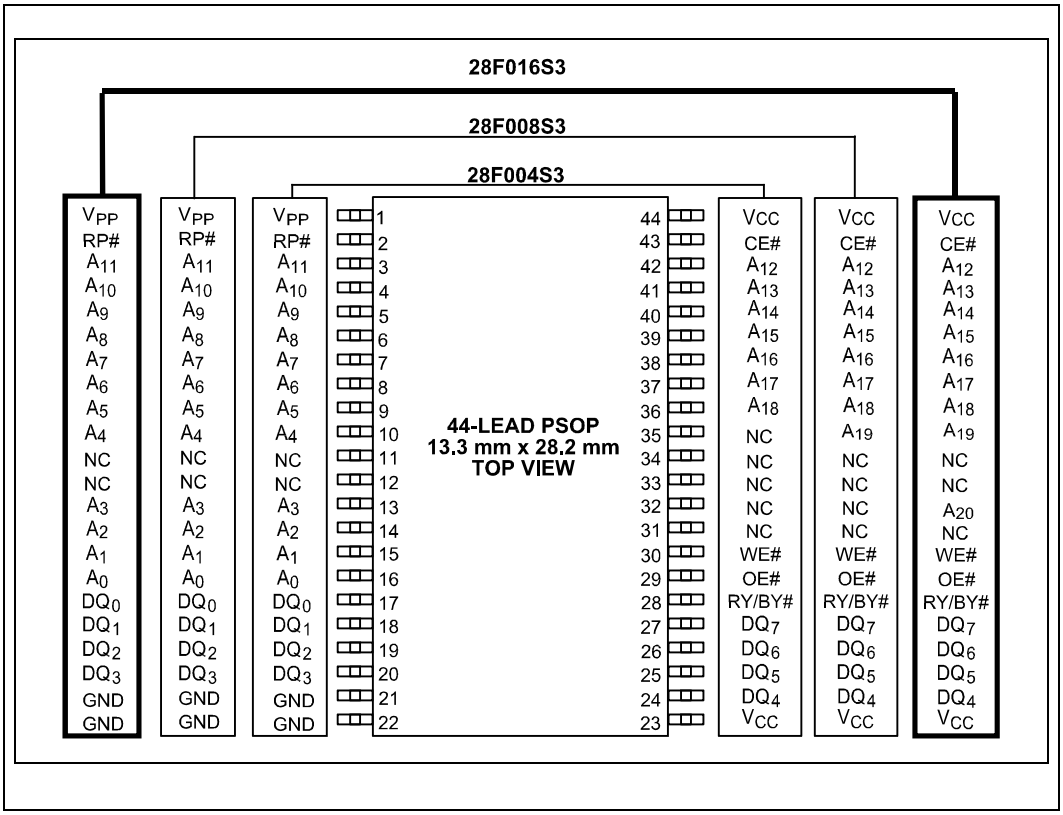

Figure 3. PSOP 44-Lead Pinout

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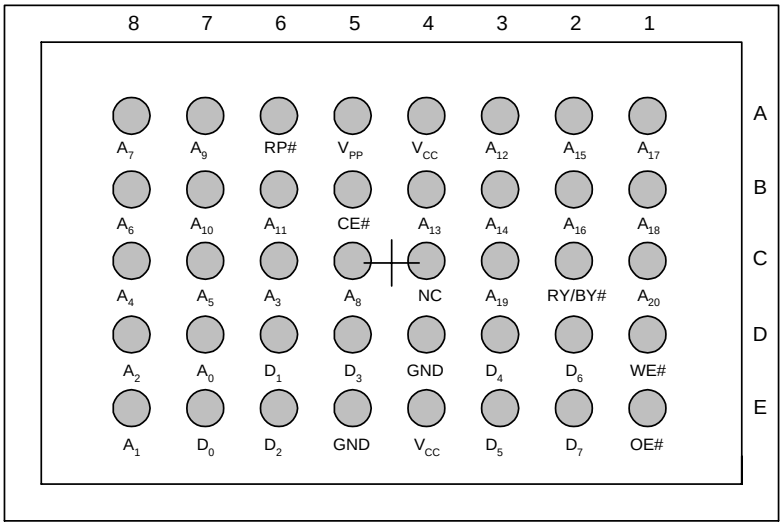
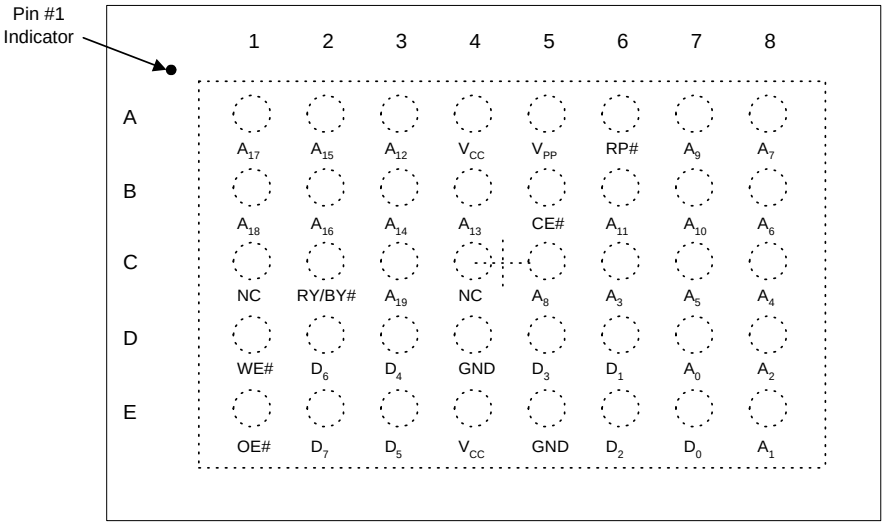


Bottom View - Bump Side Up



Top View - Bump Side Down

This is the view of the package as surface mounted on the board.
Note that the signals are mirror images of bottom view.

NOTES:

1. Figures are not drawn to scale.
2. Address A_{20} is not included in the 28F008S3.
3. More information on µBGA* packages is available by contacting your Intel/Distribution sales office.

Figure 4. µBGA* CSP 40-Bump Pinout (28F008S3 and 28F016S3)

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2.0 PRINCIPLES OF OPERATION

The 3 Volt FlashFile memories include an on-chip WSM to manage block erase, program, and lock-bit configuration functions. It allows for: 100% TTL-level control inputs, fixed power supplies during block erasure, program, and lock-bit configuration, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from deep power-down mode (see *Bus Operations*), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby, and output disable operations.

Status register and identifier codes can be accessed through the CUI independent of the V_{PP} voltage. High voltage on V_{PP} enables successful block erasure, program, and lock-bit configuration. All functions associated with altering memory contents—block erase, program, lock-bit configuration, status, and identifier codes—are accessed via the CUI and verified through the status register.

Commands are written using standard micro-processor write timings. The CUI contents serve as input to the WSM that controls block erase, program, and lock-bit configuration operations. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification, and margining of data. Addresses and data are internally latched during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes, or outputs status register data.

Interface software that initiates and polls progress of block erase, program, and lock-bit configuration can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read data from or program data to any other block. Program suspend allows system software to suspend a program to read data from any other flash memory array location.

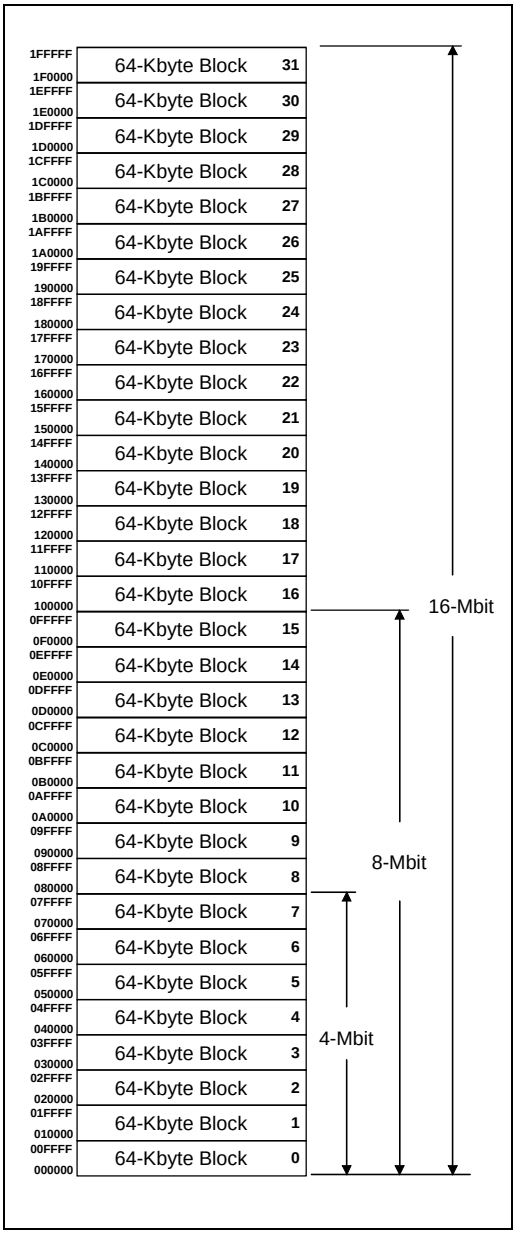

Figure 5. Memory Map

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2.1 Data Protection

Depending on the application, the system designer may choose to make the V_{PP} power supply switchable (available only when memory block erase, program, or lock-bit configuration operations are required) or hardwired to $V_{PPH1/2}$. The device accommodates either design practice and encourages optimization of the processor-memory interface.

When $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. When high voltage is applied to V_{PP}, the two-step block erase, program, or lock-bit configuration command sequences provides protection from unwanted operations. All write functions are disabled when V_{CC} voltage is below the write lockout voltage V_{LKO} or when RP# is at V_{IL}. The device's block locking capability provides additional protection from inadvertent code or data alteration by gating erase and program operations.

3.0 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

3.1 Read

Block information, identifier codes, or status register can be read independent of the V_{PP} voltage. RP# can be at either V_{IH} or V_{HH}.

The first task is to write the appropriate read-mode command (Read Array, Read Identifier Codes, or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to read array mode. Four control pins dictate the data flow in and out of the component: CE#, OE#, WE#, and RP#. CE# and OE# must be driven active to obtain data at the outputs. CE# is the device selection control, and when active enables the selected memory device. OE# is the data output (DQ_0–DQ_7) control and when active drives the selected memory data onto the I/O bus. WE# must be at V_{IH} and RP# must be at V_{IH} or V_{HH}. Figure 15 illustrates a read cycle.

3.2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins DQ_0–DQ_7 are placed in a high-impedance state.

3.3 Standby

CE# at a logic-high level (V_{IH}) places the device in standby mode which substantially reduces device power consumption. DQ_0–DQ_7 outputs are placed in a high-impedance state independent of OE#. If deselected during block erase, program, or lock-bit configuration, the device continues functioning and consuming active power until the operation completes.

3.4 Deep Power-Down

RP# at V_{IL} initiates the deep power-down mode.

In read mode, RP#-low deselects the memory, places output drivers in a high-impedance state, and turns off all internal circuits. RP# must be held low for time t_{PLPH}. Time t_{PHQV} is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI resets to read array mode, and the status register is set to 80H.

During block erase, program, or lock-bit configuration, RP#-low will abort the operation. RY/BY# remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written. Time t_{PHWL} is required after RP# goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, program, or lock-bit configuration modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. Intel's flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

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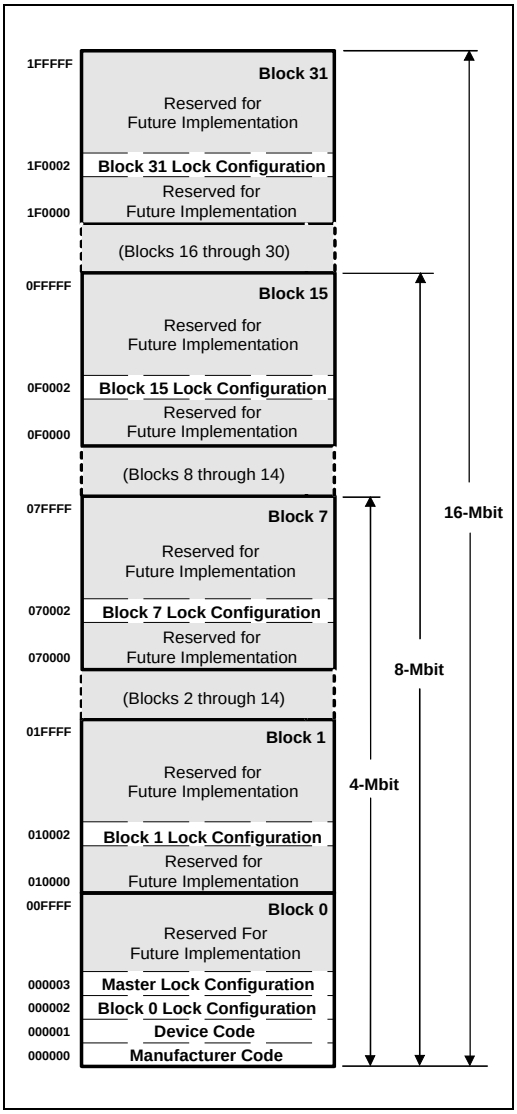

Figure 6. Device Identifier Code Memory Map

3.5 Read Identifier Codes Operation

The read identifier codes operation outputs the manufacturer code, device code, block lock configuration codes for each block, and master lock configuration code (see Figure 6). Using the manufacturer and device codes, the system software can automatically match the device with its proper algorithms. The block lock and master lock configuration codes identify locked and unlocked blocks and master lock-bit setting.

3.6 Write

The CUI does not occupy an addressable memory location. It is written when WE# and CE# are active and OE# = V_{IH}. The address and data needed to execute a command are latched on the rising edge of WE# or CE# (whichever goes high first). Standard microprocessor write timings are used. Figure 18 illustrates a write operation.

4.0 COMMAND DEFINITIONS

When the V_{PP} voltage ≤ V_{PPLK}, read operations from the status register, identifier codes, or blocks are enabled. Placing $V_{PPH1/2}$ on V_{PP} enables successful block erase, program, and lock-bit configuration operations.

Device operations are selected by writing specific commands into the CUI. Table 3 defines these commands.

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Table 2. Bus Operations

Mode	Notes	RP#	CE#	OE#	WE#	Address	V_{PP}	DQ_{0-7}	RY/BY#
Read	1,2,3	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	X
Output Disable	3	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	X
Standby	3	V_{IH} or V_{HH}	V_{IH}	X	X	X	X	High Z	X
Deep Power-Down	4	V_{IL}	X	X	X	X	X	High Z	V_{OH}
Read Identifier Codes		V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	See Figure 5	X	Note 5	V_{OH}
Write	3,6,7	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}	X

NOTES:

1. Refer to *DC Characteristics*. When $V_{PP} \le V_{PPLK}$, memory contents can be read, but not altered.
2. X can be V_{IL} or V_{IH} for control and address input pins and V_{PPLK} or $V_{PPH1/2}$ for V_{PP}. See *DC Characteristics* for V_{PPLK} and $V_{PPH1/2}$ voltages.
3. RY/BY# is V_{OL} when the WSM is executing internal block erase, program, or lock-bit configuration algorithms. It is V_{OH} when the WSM is not busy, in block erase suspend, program suspend, or deep power-down mode.
4. RP# at GND ± 0.2 V ensures the lowest deep power-down current.
5. See Section 4.2 for read identifier code data.
6. Command writes involving block erase, program, or lock-bit configuration are reliably executed when $V_{PP} = V_{PPH1/2}$ and $V_{CC} = V_{CC2}$ (see Section 6.2 for operating conditions).
7. Refer to Table 3 for valid D_{IN} during a write operation.

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Table 3. Command Definitions[9]

Command	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
			Oper[1]	Addr[2]	Data[3]	Oper[1]	Addr[2]	Data[3]
Read Array/Reset	1		Write	X	FFH			
Read Identifier Codes	≥ 2	4	Write	X	90H	Read	IA	ID
Read Status Register	2		Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Program	2	5,6	Write	PA	40H or 10H	Write	PA	PD
Block Erase and Program Suspend	1	5	Write	X	B0H			
Block Erase and Program Resume	1	5	Write	X	D0H			
Set Block Lock-Bit	2	7	Write	BA	60H	Write	BA	01H
Set Master Lock-Bit	2	7	Write	X	60H	Write	X	F1H
Clear Block Lock-Bits	2	8	Write	X	60H	Write	X	D0H

NOTES:

1. Bus operations are defined in Table 2.
2. X = Any valid address within the device.
   IA = Identifier Code Address: see Figure 6.
   BA = Address within the block being erased or locked.
   PA = Address of memory location to be programmed.
3. SRD = Data read from status register. See Table 6 for a description of the status register bits.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).
   ID = Data read from identifier codes.
4. Following the Read Identifier Codes command, read operations access manufacturer, device, block lock, and master lock codes. See Section 4.2 for read identifier code data.
5. If the block is locked, RP# must be at V_{HH} to enable block erase or program operations. Attempts to issue a block erase or program to a locked block while RP# is V_{IH} will fail.
6. Either 40H or 10H are recognized by the WSM as the program setup.
7. If the master lock-bit is set, RP# must be at V_{HH} to set a block lock-bit. RP# must be at V_{HH} to set the master lock-bit. If the master lock-bit is not set, a block lock-bit can be set while RP# is V_{IH}.
8. If the master lock-bit is set, RP# must be at V_{HH} to clear block lock-bits. The clear block lock-bits operation simultaneously clears all block lock-bits. If the master lock-bit is not set, the Clear Block Lock-Bits command can be done while RP# is V_{IH}.
9. Commands other than those shown above are reserved by Intel for future device implementations and should not be used.

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4.1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase, program, or lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend or Program Suspend command. The Read Array command functions independently of the V_{PP} voltage and RP# can be V_{IH} or V_{HH}.

4.2 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 6 retrieve the manufacturer, device, block lock configuration and master lock configuration codes (see Table 4 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V_{PP} voltage and RP# can be V_{IH} or V_{HH}. Following the Read Identifier Codes command, the subsequent information can be read.

Table 4. Identifier Codes

Code		Address	Data
Manufacturer Code		000000	89
Device Code	4-Mbit	000001	A7
	8-Mbit	000001	A6
	16-Mbit	000001	AA
Block Lock Configuration		XX0002(1)	
• Block Is Unlocked			DQ_0 = 0
• Block Is Locked			DQ_0 = 1
• Reserved for Future Use			DQ_{1-7}
Master Lock Configuration		000003	
• Device Is Unlocked			DQ_0 = 0
• Device Is Locked			DQ_0 = 1
• Reserved for Future Use			DQ_{1-7}

NOTE:

1. X selects the specific block lock configuration code to be read. See Figure 5 for the device identifier code memory map.

4.3 Read Status Register Command

The status register may be read to determine when a block erase, program, or lock-bit configuration is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of OE# or CE#, whichever occurs first. OE# or CE# must toggle to V_{IH} to update the status register latch. The Read Status Register command functions independently of the V_{PP} voltage. RP# can be V_{IH} or V_{HH}.

4.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3, and SR.1 are set to “1”s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 6). By allowing system software to reset these bits, several operations (such as cumulatively erasing or locking multiple blocks or writing several bytes in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied V_{PP} voltage. RP# can be V_{IH} or V_{HH}. This command is not functional during block erase or program suspend modes.

4.5 Block Erase Command

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is written first, followed by a block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 7). The CPU can detect block erase completion by analyzing the RY/BY# pin or status register bit SR.7.

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When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1." Also, reliable block erasure can only occur when $V_{CC} = V_{CC2}$ and $V_{PP} = V_{PPH1/2}$. In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while $V_{PP} \leq V_{PPLK}$, SR.3 and SR.5 will be set to "1." Successful block erase requires that the corresponding block lock-bit be cleared or, if set, that RP# = V_{HH}. If block erase is attempted when the corresponding block lock-bit is set and RP# = V_{IH}, the block erase will fail, and SR.1 and SR.5 will be set to "1." Block erase operations with $V_{IH} < RP\# < V_{HH}$ produce spurious results and should not be attempted.

4.6 Program Command

Program is executed by a two-cycle command sequence. Program setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the program and verify algorithms internally. After the program sequence is written, the device automatically outputs status register data when read (see Figure 8). The CPU can detect the completion of the program event by analyzing the RY/BY# pin or status register bit SR.7.

When program is complete, status register bit SR.4 should be checked. If program error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully program to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable program only occurs when $V_{CC} = V_{CC2}$ and $V_{PP} = V_{PPH1/2}$. In the absence of this high voltage, memory contents are protected against program operations. If a program operation is attempted while $V_{PP} \leq V_{PPLK}$, the operation will fail, and status register bits SR.3 and SR.5 will be set to "1."

A successful program operation also requires that the corresponding block lock-bit be cleared or, if set, that RP# = V_{HH}. If a program operation is attempted when the corresponding block lock-bit is set and RP# = V_{IH}, the operation will fail, and SR.1 and SR.4 will be set to "1." Program operations with $V_{IH} < RP\# < V_{HH}$ produce spurious results and should not be attempted.

4.7 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or program data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to "1"). RY/BY# will also transition to V_{OH}. Specification t_{WHRH2} defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A Program command sequence can also be issued during erase suspend to program data in other blocks. Using the Program Suspend command (see Section 4.8), a program operation can also be suspended. During a program operation with block erase suspended, status register bit SR.7 will return to "0" and the RY/BY# output will transition to V_{OL}. However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and RY/BY# will return to V_{OL}. After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 9). V_{PP} must remain at $V_{PPH1/2}$ (the same V_{PP} level used for block erase) while block erase is suspended. RP# must also remain at V_{IH} or V_{HH} (the same RP# level used for block erase). Block erase cannot resume until program operations initiated during block erase suspend have completed.

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4.8 Program Suspend Command

The Program Suspend command allows program interruption to read data in other flash memory locations. Once the program process starts, writing the Program Suspend command requests that the WSM suspend the program sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Program Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the program operation has been suspended (both will be set to "1"). RY/BY# will also transition to V_{OH}. Specification t_{WHRH1} defines the program suspend latency.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while program is suspended are Read Status Register and Program Resume. After Program Resume command is written to the flash memory, the WSM will continue the program process. Status register bits SR.2 and SR.7 will automatically clear and RY/BY# will return to V_{OL}. After the Program Resume command is written, the device automatically outputs status register data when read (see Figure 10). V_{PP} must remain at $V_{PPH1/2}$ (the same V_{PP} level used for program) while in program suspend mode. RP# must also remain at V_{IH} or V_{HH} (the same RP# level used for program).

4.9 Set Block and Master Lock-Bit Commands

A flexible block locking and unlocking scheme is enabled via a combination of block lock-bits and a master lock-bit. The block lock-bits gate program and erase operations while the master lock-bit gates block-lock bit modification. With the master lock-bit not set, individual block lock-bits can be set using the Set Block Lock-Bit command. The Set Master Lock-Bit command, in conjunction with RP# = V_{HH}, sets the master lock-bit. After the master lock-bit is set, subsequent setting of block lock-bits requires both the Set Block Lock-Bit command and V_{HH} on the RP# pin. See Table 5 for a summary of hardware and software write protection options.

Set block lock-bit and master lock-bit are initiated using two-cycle command sequence. The set block or master lock-bit setup along with appropriate block or device address is written followed by either the set block lock-bit confirm (and an address within the block to be locked) or the set master lock-bit confirm (and any device address). The WSM then controls the set lock-bit algorithm. After the sequence is written, the device automatically outputs status register data when read (see Figure 11). The CPU can detect the completion of the set lock-bit event by analyzing the RY/BY# pin output or status register bit SR.7.

When the set lock-bit operation is complete, status register bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.

This two-step sequence of setup followed by execution ensures that lock-bits are not accidentally set. An invalid Set Block or Master Lock-Bit command will result in status register bits SR.4 and SR.5 being set to "1." Also, reliable operations occur only when V_{CC} = V_{CC2} and V_{PP} = $V_{PPH1/2}$. In the absence of this high voltage, lock-bit contents are protected against alteration.

A successful set block lock-bit operation requires that the master lock-bit be cleared or, if the master lock-bit is set, that RP# = V_{HH}. If it is attempted with the master lock-bit set and RP# = V_{IH}, the operation will fail, and SR.1 and SR.4 will be set to "1." A successful set master lock-bit operation requires that RP# = V_{HH}. If it is attempted with RP# = V_{IH}, the operation will fail, and SR.1 and SR.4 will be set to "1." Set block and master lock-bit operations with V_{IH} < RP# < V_{HH} produce spurious results and should not be attempted.

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4.10 Clear Block Lock-Bits Command

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. With the master lock-bit not set, block lock-bits can be cleared using only the Clear Block Lock-Bits command. If the master lock-bit is set, clearing block lock-bits requires both the Clear Block Lock-Bits command and V_{HH} on the RP# pin. See Table 5 for a summary of hardware and software write protection options.

Clear block lock-bits operation is initiated using a two-cycle command sequence. A clear block lock-bits setup is written first. Then, the device automatically outputs status register data when read (see Figure 12). The CPU can detect completion of the clear block lock-bits event by analyzing the RY/BY# pin output or status register bit SR.7.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock-bit error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in status register bits SR.4 and SR.5 being set to "1." Also, a reliable clear block lock-bits operation can only occur when $V_{CC} = V_{CC2}$ and $V_{PP} = V_{PPH1/2}$. If a clear block lock-bits operation is attempted while $V_{PP} \leq V_{PPLK}$, SR.3 and SR.5 will be set to "1." In the absence of this high voltage, the block lock-bits content are protected against alteration. A successful clear block lock-bits operation requires that the master lock-bit is not set or, if the master lock-bit is set, that RP# = V_{HH}. If it is attempted with the master lock-bit set and RP# = V_{IH}, SR.1 and SR.5 will be set to "1" and the operation will fail. A clear block lock-bits operation with $V_{IH} < RP\# < V_{HH}$ produce spurious results and should not be attempted.

If a clear block lock-bits operation is aborted due to V_{PP} or V_{CC} transitioning out of valid range or RP# active transition, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values. Once the master lock-bit is set, it cannot be cleared.

Table 5. Write Protection Alternatives

Operation	Master Lock-Bit	Block Lock-Bit	RP#	Effect
Block Erase or Byte Write	X	0	V_{IH} or V_{HH}	Block Erase and Program Enabled
		1	V_{IH}	Block is Locked. Block Erase and Program Disabled
			V_{HH}	Block Lock-Bit Override. Block Erase and Program Enabled
Set Block Lock-Bit	0	X	V_{IH} or V_{HH}	Set Block Lock-Bit Enabled
	1	X	V_{IH}	Master Lock-Bit is Set. Set Block Lock-Bit Disabled
			V_{HH}	Master Lock-Bit Override. Set Block Lock-Bit Enabled
Set Master Lock-Bit	X	X	V_{IH}	Set Master Lock-Bit Disabled
			V_{HH}	Set Master Lock-Bit Enabled
Clear Block Lock-Bits	0	X	V_{IH} or V_{HH}	Clear Block Lock-Bits Enabled
	1	X	V_{IH}	Master Lock-Bit is Set. Clear Block Lock-Bits Disabled
			V_{HH}	Master Lock-Bit Override. Clear Block Lock-Bits Enabled

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Table 6. Status Register Definition

WSMS	ESS	ECLBS	PSLBS	VPPS	PSS	DPS	R
7	6	5	4	3	2	1	0

	NOTES:
SR.7 = WRITE STATE MACHINE STATUS 1 = Ready 0 = Busy	Check RY/BY# or SR.7 to determine block erase, program, or lock-bit configuration completion. SR.6–0 are invalid while SR.7 = "0."
SR.6 = ERASE SUSPEND STATUS 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	
SR.5 = ERASE AND CLEAR LOCK-BITS STATUS 1 = Error in Block Erasure or Clear Lock-Bits 0 = Successful Block Erase or Clear Lock-Bits	If both SR.5 and SR.4 are "1"s after a block erase or lock-bit configuration attempt, an improper command sequence was entered.
SR.4 = PROGRAM AND SET LOCK-BIT STATUS 1 = Error in Program or Set Master/Block Lock-Bit 0 = Successful Program or Set Master/Block Lock-Bit	
SR.3 = V_{PP} STATUS 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK	SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after a block erase, program, or lock-bit configuration operation. SR.3 is not guaranteed to reports accurate feedback only when $V_{PP} \neq V_{PPH1/2}$.
SR.2 = PROGRAM SUSPEND STATUS 1 = Program Suspended 0 = Program in Progress/Completed	
SR.1 = DEVICE PROTECT STATUS 1 = Master Lock-Bit, Block Lock-Bit and/or RP# Lock Detected, Operation Abort 0 = Unlock	SR.1 does not provide a continuous indication of master and block lock-bit values. The WSM interrogates the master lock-bit, block lock-bit, and RP# only after a block erase, program, or lock-bit configuration operation. It informs the system, depending on the attempted operation, if the block lock-bit is set, master lock-bit is set, and/or RP# ≠ V_{HH}.
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS	SR.0 is reserved for future use and should be masked out when polling the status register.

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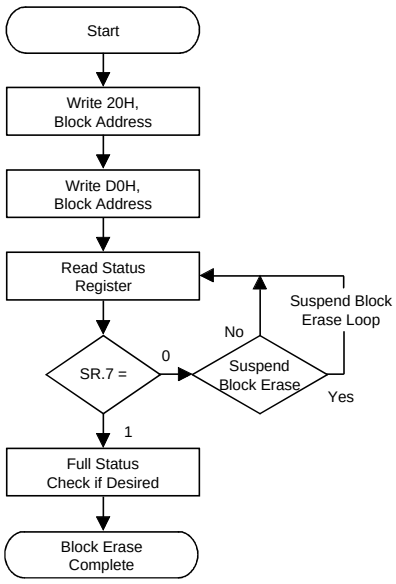
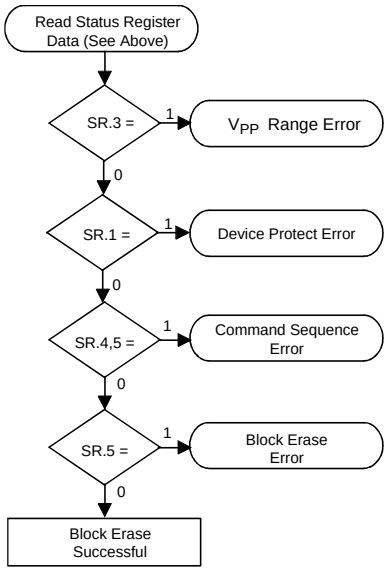


Bus Operation	Command	Comments
Write	Erase Setup	Data = 20H Addr = Within Block to Be Erased
Write	Erase Confirm	Data = D0H Addr = Within Block to Be Erased
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent block erasures. Full status check can be done after each block erase, or after a sequence of block erasures. Write FFH after the last operation to place device in read array mode.		

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect RP# = V_{IH}, Block Lock-Bit Is Set Only required for systems implementing lock-bit configuration
Standby		Check SR.4,5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple blocks are erased before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 7. Automated Block Erase Flowchart

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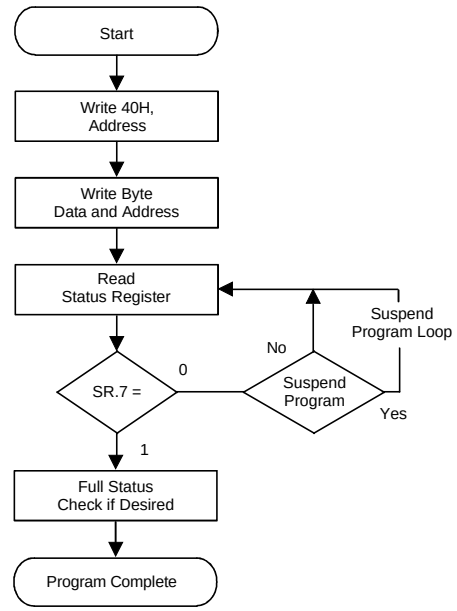
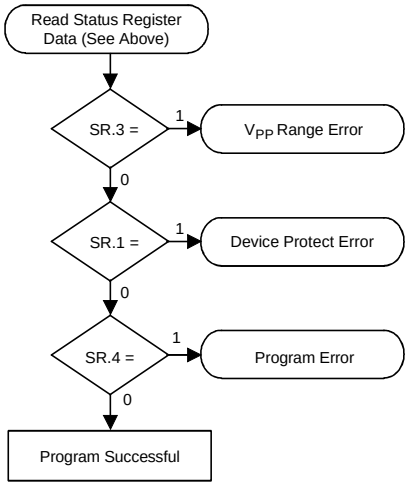


Bus Operation	Command	Comments
Write	Setup Program	Data = 40H Addr = Location to Be Programmed
Write	Program	Data = Data to Be Programmed Addr = Location to Be Programmed
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent byte writes. SR full status check can be done after each program, or after a sequence of program operations. Write FFH after the last program operation to reset device to read array mode.		

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect RP# = V_{IH}, Block Lock-Bit Is Set Only required for systems implementing lock-bit configuration
Standby		Check SR.4 1 = Program Error
SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 8. Automated Program Flowchart

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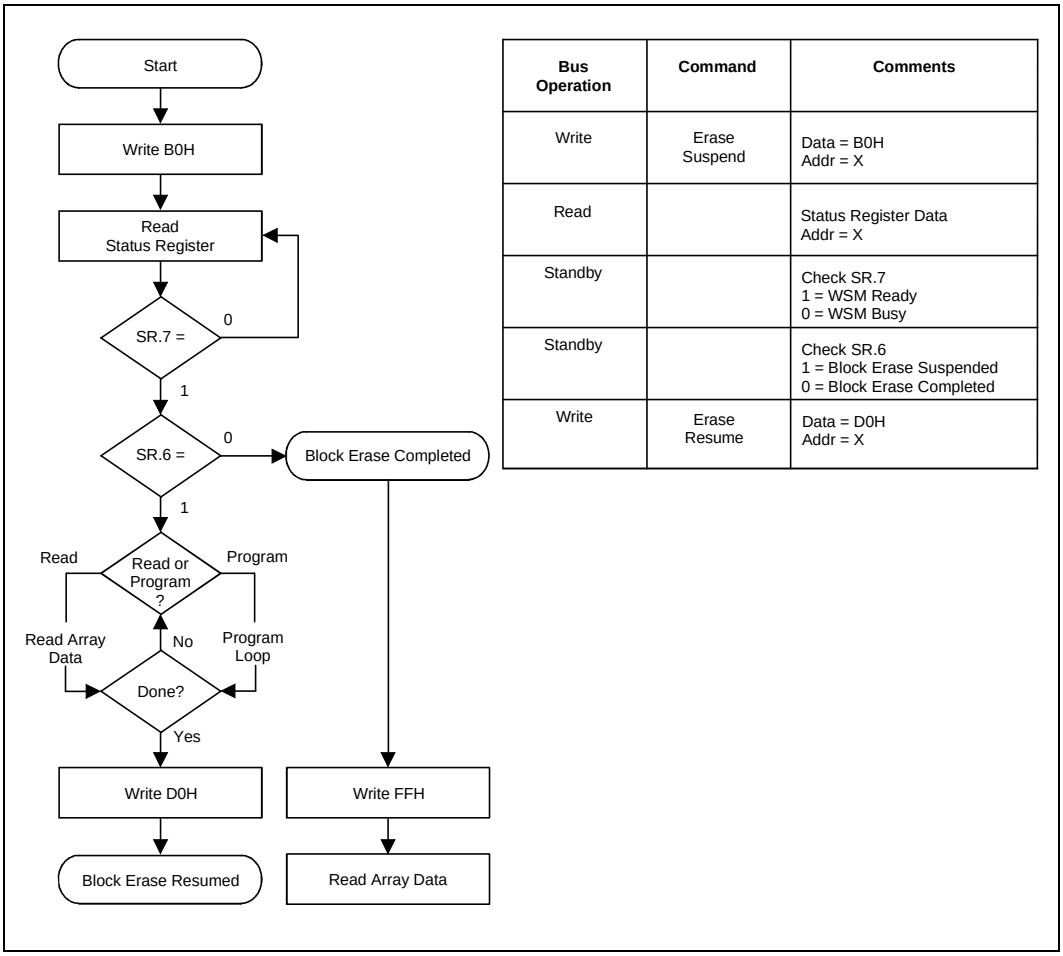

Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Block Erase Suspended 0 = Block Erase Completed
Write	Erase Resume	Data = D0H Addr = X

Figure 9. Block Erase Suspend/Resume Flowchart

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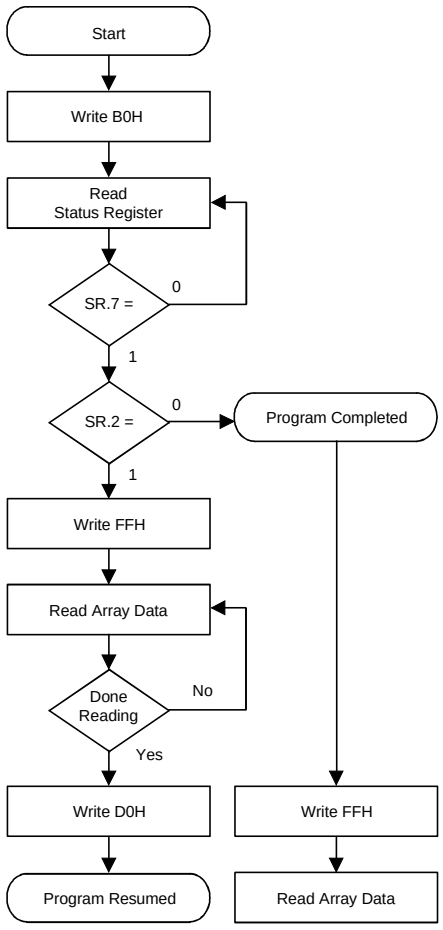

Bus Operation	Command	Comments
Write	Program Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.2 1 =Program Suspended 0 = Program Completed
Write	Read Array	Data = FFH Addr = X
Read		Read array locations other than that being data written.
Write	Program Resume	Data = D0H Addr = X

Figure 10. Program Suspend/Resume Flowchart

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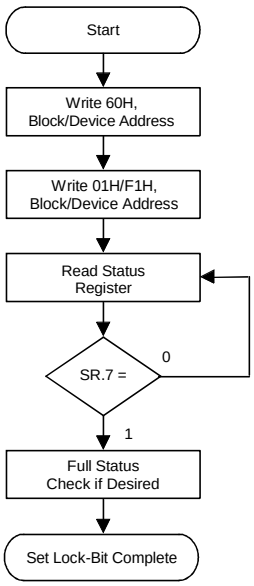
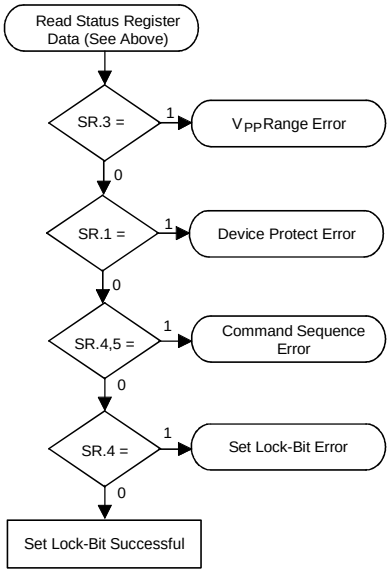


Bus Operation	Command	Comments
Write	Set Block/Master Lock-Bit Setup	Data = 60H Addr = Block Address (Block), Device Address (Master)
Write	Set Block or Master Lock-Bit Confirm	Data = 01H (Block), F1H (Master) Addr = Block Address (Block), Device Address (Master)
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent lock-bit set operations. Full status check can be done after each lock-bit set operation or after a sequence of lock-bit set operations. Write FFH after the last lock-bit set operation to place device in read array mode.		

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect RP# = V_{IH}, (Set Master Lock-Bit Operation) RP# = V_{HH}, Master Lock-Bit Is Set (Set Block Lock-Bit Operation)
Standby		Check SR.4,5 Both 1 = Command Sequence Error
Standby		Check SR.4 1 = Set Lock-Bit Reset Error
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple lock-bits are set before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 11. Set Block and Master Lock-Bit Flowchart

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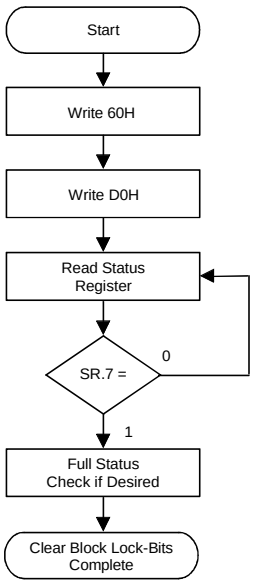
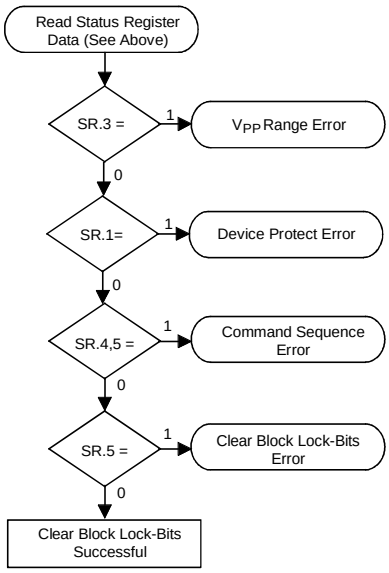


Bus Operation	Command	Comments
Write	Clear Block Lock-Bits Setup	Data = 60H Addr = X
Write	Clear Block Lock-Bits Confirm	Data = D0H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write FFH after the Clear Block Lock-Bits operation to place device to read array mode.		

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect RP# = V_{IH}, Master Lock-Bit Is Set
Standby		Check SR.4,5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Clear Block Lock-Bits Error
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 12. Clear Block Lock-Bits Flowchart

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5.0 DESIGN CONSIDERATIONS

5.1 Three-Line Output Control

Intel provides three control inputs to accommodate multiple memory connections: CE#, OE#, and RP#. Three-line control provides for:

a. Lowest possible memory power dissipation.

b. Data bus contention avoidance.

To use these control inputs efficiently, an address decoder should enable CE# while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs while de-selected memory devices are in standby mode. RP# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

5.2 RY/BY# Hardware Detection

RY/BY# is a full CMOS output that provides a hardware method of detecting block erase program and lock-bit configuration completion. This output can be directly connected to an interrupt input of the system CPU. RY/BY# transitions low when the WSM is busy and returns to V_{OH} when it is finished executing the internal algorithm. During suspend and deep power-down modes, RY/BY# remains at V_{OH}.

5.3 Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues: standby current levels, active current levels and transient peaks produced by falling and rising edges of CE# and OE#. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between its V_{CC} and GND and between its V_{PP} and GND. These high-frequency, low-inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7 µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

5.4 V_{PP} Trace on Printed Circuit Boards

Updating flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{PP} power supply trace. The V_{PP} pin supplies the memory cell current for byte writing and block erasing. Use similar trace widths and layout considerations given to the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

5.5 V_{CC}, V_{PP}, RP# Transitions

Block erase, program and lock-bit configuration are not guaranteed if V_{PP} or V_{CC} fall outside of a valid voltage range (V_{CC2} and $V_{PPH1/2}$) or RP# ≠ V_{IH} or V_{HH}. If V_{PP} error is detected, status register bit SR.3 is set to "1" along with SR.4 or SR.5, depending on the attempted operation. If RP# transitions to V_{IL} during block erase, program, or lock-bit configuration, RY/BY# will remain low until the reset operation is complete. Then, the operation will abort and the device will enter deep power-down. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored.

5.6 Power-Up/Down Protection

The device is designed to offer protection against accidental block erasure, byte writing, or lock-bit configuration during power transitions. Upon power-up, the device is indifferent as to which power supply (V_{PP} or V_{CC}) powers-up first. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against spurious writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both WE# and CE# must be low for a command write, driving either input signal to V_{IH} will inhibit writes. The CUI's two-step command sequence architecture provides an added level of protection against data alteration.

In-system block lock and unlock renders additional protection during power-up by prohibiting block erase and program operations. The device is disabled while RP# = V_{IL} regardless of its control inputs state.

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5.7 V_{PP} Program and Erase Voltages on Sub-0.4µ S3 Memory Family

The Intel 3 Volt FlashFile™ memory family provides in-system program/erase at 2.7 V and 3.3 V V_{PP} as well as faster factory program/erase at 12 V V_{PP}.

Future sub-0.4 µ lithography 3 Volt FlashFile memory products will also include a backward-compatible 12 V programming feature. This mode, however, is not intended for extended use. A 12 V program/erase V_{PP} can be applied for 1000 cycles maximum per block or 80 hours maximum per device. To ensure compatibility with future sub-0.4 µ 3 Volt FlashFile memory products, present designs should not permanently connect V_{PP} to 12 V. This will avoid device over-stressing that may cause permanent damage.

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6.0 ELECTRICAL SPECIFICATIONS

NOTICE: This datasheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

6.1 Absolute Maximum Ratings*

Temperature under Bias ..... –10 °C to +80 °C

Storage Temperature ..... –65 °C to +125 °C

Voltage On Any Pin (except V_{PP}, and RP#) ..... –2.0 V to +7.0 V(2)

V_{PP} Voltage ..... –2.0 V to +14.0 V(1,2)

RP# Voltage ..... –2.0 V to +14.0 V(1,2,4)

Output Short Circuit Current ..... 100 mA(3)

** WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may effect device reliability.*

NOTES:

1. All specified voltages are with respect to GND. Minimum DC voltage is –0.5 V on input/output pins and –0.2 V on V_{CC}, RP#, and V_{PP} pins. During transitions, this level may undershoot to –2.0 V for periods <20 ns. Maximum DC voltage on input/output pins and V_{CC} is V_{CC} +0.5 V which, during transitions, may overshoot to V_{CC} +2.0 V for periods <20 ns.
2. Maximum DC voltage on V_{PP} and RP# may overshoot to +14.0 V for periods <20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.
4. RP# voltage is normally at V_{IL} or V_{IH}. Connection to supply of V_{HH} is allowed for a maximum cumulative period of 80 hours.

6.2 Commercial Temperature Operating Conditions

Commercial Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Notes	Min	Max	Unit	Test Condition
T_A	Operating Temperature		0	+70	°C	Ambient Temperature
V_{CC1}	V_{CC} Supply Voltage (2.7 V–3.6 V)	1	2.7	3.6	V	
V_{CC2}	V_{CC} Supply Voltage (3.3 V ± 0.3 V)		3.0	3.6	V	

NOTE:

1. Block erase, program, and lock-bit configuration with V_{CC} < 2.7 V should not be attempted.

6.3 Capacitance(1)

T_A = +25 °C, f = 1 MHz

Symbol	Parameter	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	6	8	pF	V_{IN} = 0.0 V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0.0 V

NOTE:

1. Sampled, not 100% tested.

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6.4 DC Characteristics—Commercial Temperature

Sym	Parameter	Notes	2.7 V V_{CC}		3.3 V V_{CC}		Unit	Test Conditions
			Typ	Max	Typ	Max		
I_{LI}	Input Load Current	1		± 0.5		± 0.5	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1		± 0.5		± 0.5	µA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	1,3,6	20	100	20	100	µA	CMOS Inputs $V_{CC} = V_{CC}$ Max CE# = RP# = V_{CC} ± 0.2 V
			0.1	2	0.2	2	mA	TTL Inputs $V_{CC} = V_{CC}$ Max CE# = RP# = V_{IH}
I_{CCD}	V_{CC} Deep Power-Down Current	1		10		10	µA	RP# = GND ± 0.2 V I_{OUT} (RY/BY#) = 0 mA
I_{CCR}	V_{CC} Read Current	1,5,6	6	15	7	15	mA	CMOS Inputs $V_{CC} = V_{CC}$ Max, CE# = GND f = 5 MHz, I_{OUT} = 0 mA
			7	18	8	18	mA	TTL Inputs $V_{CC} = V_{CC}$ Max, CE# = GND f = 5 MHz, I_{OUT} = 0 mA
I_{CCW}	V_{CC} Program/ Set Lock-Bit Current	1,7	—	—		17	mA	V_{PP} = 3.3 V ± 0.3 V
			—	—		12	mA	V_{PP} = 12.0 V ± 5%
I_{CCE}	V_{CC} Block Erase/Clear Block Lock-Bits Current	1,7	—	—		17	mA	V_{PP} = 3.3 V ± 0.3 V
			—	—		12	mA	V_{PP} = 12.0 V ± 5%
I_{CCWS} I_{CCES}	V_{CC} Program/Block Erase Suspend Current	1,2	—	—		6	mA	CE# = V_{IH}
I_{PPS}	V_{PP} Standby Current	1	± 2	± 15	± 2	± 15	µA	$V_{PP} \leq V_{CC}$
I_{PPR}	V_{PP} Read Current	1	10	200	10	200	µA	$V_{PP} > V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1	0.1	5	0.1	5	µA	RP# = GND ± 0.2 V
I_{PPW}	V_{PP} Program/Set Lock-Bit Current	1,7	—	—		40	mA	V_{PP} = 3.3 V ± 0.3 V
			—	—		15	mA	V_{PP} = 12.0 V ± 5%
I_{PPE}	V_{PP} Block Erase/Clear Block Lock-Bits Current	1,7	—	—		20	mA	V_{PP} = 3.3 V ± 0.3 V
			—	—		15	mA	V_{PP} = 12.0 V ± 5%
I_{PPWS} I_{PPES}	V_{PP} Block Erase/Program Suspend Current	1	—	—	10	200	µA	$V_{PP} = V_{PPH1/2}$

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6.4 DC Characteristics— Commercial Temperature (Continued)

Sym	Parameter	Notes	2.7 V V_{CC}		3.3 V V_{CC}		Unit	Test Conditions
			Min	Max	Min	Max		
V_{IL}	Input Low Voltage	7	–0.5	0.8	–0.5	0.8	V	
V_{IH}	Input High Voltage	7	2.0	V_{CC} + 0.5	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage	3,7		0.4		0.4	V	$V_{CC} = V_{CC}$ Min I_{OL} = 2 mA
V_{OH1}	Output High Voltage (TTL)	3,7	2.4		2.4		V	$V_{CC} = V_{CC}$ Min I_{OH} = –2.5 mA
V_{OH2}	Output High Voltage (CMOS)	3,7	0.85 V_{CC}		0.85 V_{CC}		V	$V_{CC} = V_{CC}$ Min I_{OH} = –2.5 mA
			V_{CC} –0.4		V_{CC} –0.4		V	$V_{CC} = V_{CC}$ Min I_{OH} = –100 µA
V_{PPLK}	V_{PP} Lockout Voltage	4,7		1.5		1.5	V	
V_{PPH1}	V_{PP} Voltage		2.7	3.6	2.7	3.6	V	
V_{PPH2}	V_{PP} Voltage		—	—	11.4	12.6	V	
V_{LKO}	V_{CC} Lockout Voltage		2.0		2.0		V	
V_{HH}	RP# Unlock Voltage	8,9	—	—	11.4	12.6	V	Set Master Lock-Bit Override Lock-Bit

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC} voltage and T_A = +25 °C. These currents are valid for all product versions (packages and speeds).
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or written while in erase suspend mode, the device's current is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}.
3. Includes RY/BY#.
4. Block erases, program, and lock-bit configurations are inhibited when $V_{PP} \le V_{PPLK}$, and not guaranteed in the range between V_{PPLK} (max) and V_{PPH1} (min), between V_{PPH1} (max) and V_{PPH2} (min), and above V_{PPH2} (max).
5. Automatic Power Savings (APS) reduces typical I_{CCR} to 3 mA at 3.3 V V_{CC} in static operation.
6. CMOS inputs are either V_{CC} ± 0.2 V or GND ± 0.2 V. TTL inputs are either V_{IL} or V_{IH}.
7. Sampled, not 100% tested.
8. Master lock-bit set operations are inhibited when RP# = V_{IH}. Block lock-bit configuration operations are inhibited when the master lock-bit is set and RP# = V_{IH}. Block erases and program are inhibited when the corresponding block-lock bit is set and RP# = V_{IH}. Block erase, program, and lock-bit configuration operations are not guaranteed and should not be attempted with V_{IH} < RP# < V_{HH}.
9. RP# connection to a V_{HH} supply is allowed for a maximum cumulative period of 80 hours.

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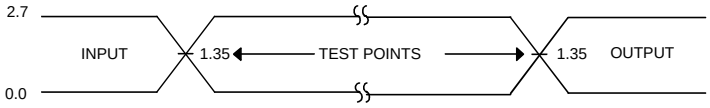
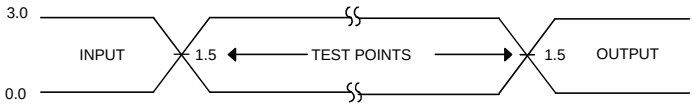


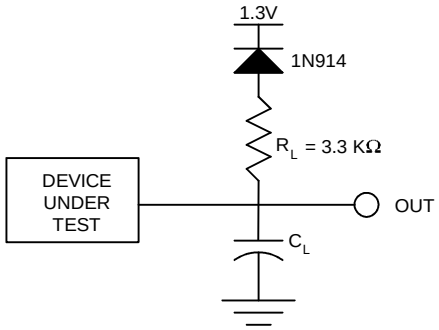
AC test inputs are driven at 2.7 V for a Logic "1" and 0.0 V for a Logic "0." Input timing begins, and output timing ends, at 1.35 V. Input rise and fall times (10% to 90%) <10 ns.

Figure 13. Transient Input/Output Reference Waveform for V_{CC} = 2.7 V–3.6 V



AC test inputs are driven at 3.0 V for a Logic "1" and 0.0 V for a Logic "0." Input timing begins, and output timing ends, at 1.5 V. Input rise and fall times (10% to 90%) <10 ns.

Figure 14. Transient Input/Output Reference Waveform for V_{CC} = 3.3 V ± 0.3 V



NOTE:
C_L includes Jig Capacitance

Figure 15. Transient Equivalent Testing Load Circuit

Test Configuration Capacitance Loading Value

Test Configuration	C_L (pF)
V_{CC} = 3.3 V ± 0.3 V, 2.7 V–3.6 V	50

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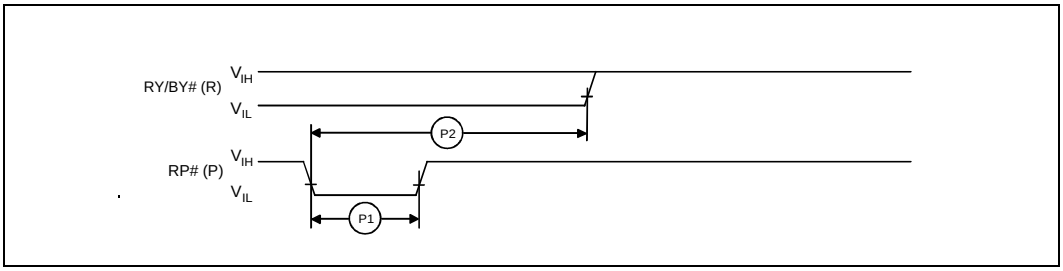

Figure 16. AC Waveform for Reset Operation

Table 7. Reset Specifications(1)—Commercial Temperature

#	Sym	Parameter	Notes	2.7 V V_{CC}		3.3 V V_{CC}		Unit
				Min	Max	Min	Max	
P1	t_{PLPH}	RP# Pulse Low Time (If RP# is tied to V_{CC}, this specification is not applicable)		100		100		ns
P2	t_{PLRH}	RP# Low to Reset during Block Erase, Program, or Lock-Bit Configuration	2,3		—		20	µs

NOTES:

1. These specifications are valid for all product versions (packages and speeds).
2. If RP# is asserted when the WSM is not busy (RY/BY# = "1"), the reset will complete within 100 ns.
3. A reset time, t_{PHQV}, is required from the latter of RY/BY# or RP# going high until outputs are valid.

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6.5 AC Characteristics—Read-Only Operations[1, 4]–Commercial Temperature

T_A = 0 °C to +70 °C

Versions[4]				3.3V ± 0.3V V_{CC}		–120		–150		—		Unit
				2.7V–3.6V V_{CC}		—		–150		–170		
#	Sym	Parameter	Notes	Min	Max	Min	Max	Min	Max			
R1	t_{AVAV}	Read Cycle Time		120		150		170				ns
R2	t_{AVQV}	Address to Output Delay			120		150		170			ns
R3	t_{ELQV}	CE# to Output Delay	2		120		150		170			ns
R4	t_{GLQV}	OE# to Output Delay	2		50		55		55			ns
R5	t_{PHQV}	RP# High to Output Delay			600		600		600			ns
R6	t_{ELQX}	CE# to Output in Low Z	3	0		0		0				ns
R7	t_{GLQX}	OE# to Output in Low Z	3	0		0		0				ns
R8	t_{EHQZ}	CE# High to Output in High Z	3		55		55		55			ns
R9	t_{GHQZ}	OE# High to Output in High Z	3		20		20		25			ns
R10	t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		0		0				ns

NOTES:

1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. OE# may be delayed up to t_{ELQV}–t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
3. Sampled, not 100% tested.
4. See *Ordering Information* for device speeds (valid operational combinations).

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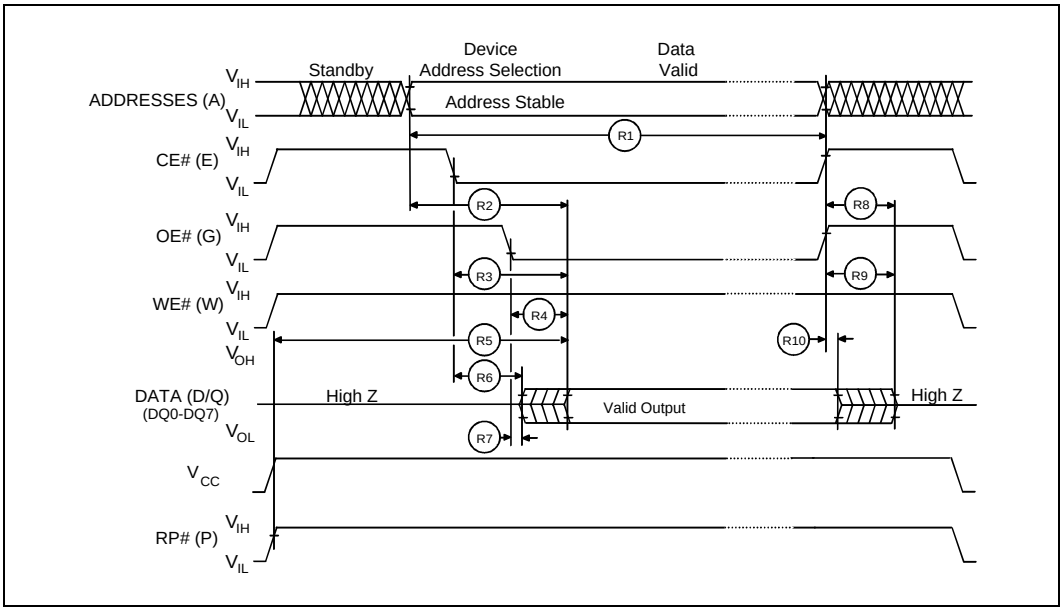

Figure 17. AC Waveform for Read Operations

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6.6 AC Characteristics—Write Operations[1, 2]—Commercial Temperature

T_A = 0 °C to +70 °C

Versions[4]			3.3V ± 0.3V, 2.7V–3.6V V_{CC}	Valid for All Speeds		Unit
#	Sym	Parameter	Notes	Min	Max	
W1	t_{PHWL} (t_{PHEL})	RP# High Recovery to WE# (CE#) Going Low	3	1		µs
W2	t_{ELWL} (t_{WLEL})	CE# (WE#) Setup to WE# (CE#) Going Low	7	0		ns
W3	t_{WP}	Write Pulse Width	7	70		ns
W4	t_{DVWH} (t_{DVEH})	Data Setup to WE# (CE#) Going High	4	50		ns
W5	t_{AVWH} (t_{AVEH})	Address Setup to WE# (CE#) Going High	4	50		ns
W6	t_{WHEH} (t_{EHWH})	CE# (WE#) Hold from WE# (CE#) High		0		ns
W7	t_{WHDX} (t_{EHDX})	Data Hold from WE# (CE#) High		5		ns
W8	t_{WHAX} (t_{EHAX})	Address Hold from WE# (CE#) High		5		ns
W9	t_{WPH}	Write Pulse Width High	9	25		ns
W10	t_{PHHWH} (t_{PHHEH})	RP# V_{HH} Setup to WE# (CE#) Going High	3,8	100		ns
W11	t_{VPWH} (t_{VPEH})	V_{PP} Setup to WE# (CE#) Going High	3,8	100		ns
W12	t_{WHRL} (t_{EHRL})	WE# (CE#) High to RY/BY# Going Low	8		90	ns
W13	t_{WHGL} (t_{EHGL})	Write Recovery before Read		0		ns
W14	t_{QVPH}	RP# V_{HH} Hold from Valid SRD, RY/BY# High	3,5,8	0		ns
W15	t_{QVVL}	V_{PP} Hold from Valid SRD, RY/BY# High	3,5,8	0		ns

NOTES:

1. Read timing characteristics during block erase, program, and lock-bit configuration operations are the same as during read-only operations. Refer to *AC Characteristics—Read-Only Operations*.
2. A write operation can be initiated and terminated with either CE# or WE#.
3. Sampled, not 100% tested.
4. Refer to Table 3 for valid A_{IN} and D_{IN} for block erase, program, or lock-bit configuration.
5. V_{PP} should be held at $V_{PPH1/2}$ (and if necessary RP# should be held at V_{HH}) until determination of block erase, program, or lock-bit configuration success (SR.1/3/4/5 = 0).
6. See Ordering Information for device speeds (valid operational combinations).
7. Write pulse width (t_{WP}) is defined from CE# or WE# going low (whichever goes low last) to CE# or WE# going high (whichever goes high first). Hence, $t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$. If CE# is driven low 10 ns before WE# going low, WE# pulse width requirement decreases to t_{WP} - 20 ns.
8. Block erase, program, and lock-bit configuration with $V_{CC} < 2.7$ V should not be attempted.
9. Write pulse width high (t_{WPH}) is defined from CE# or WE# going high (whichever goes high first) to CE# or WE# going low (whichever goes low last). Hence, $t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$.

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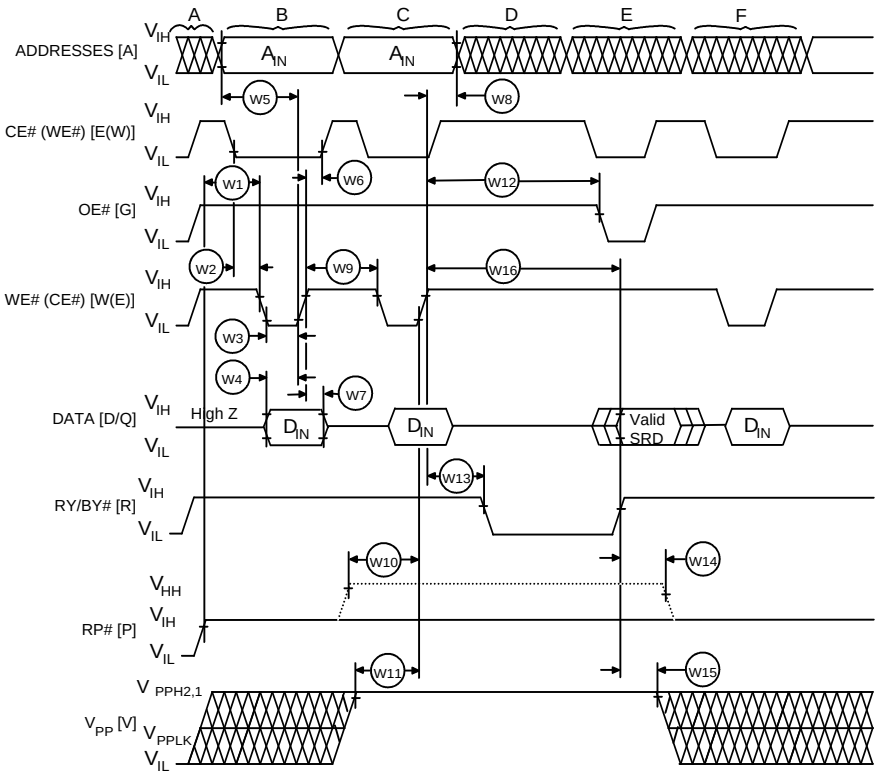

NOTES:

A. V_{CC} power-up and standby.
B. Write block erase or program setup.
C. Write block erase confirm or valid address and data..
D. Automated erase or program delay.
E. Read status register data.
F. Write Read Array command.

Figure 18. AC Waveform for Write Operations

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6.7 Block Erase, Program, and Lock-Bit Configuration Performance[3, 4, 5]— Commercial Temperature

V_{CC} = 3.3V ± 0.3V, T_A = 0 °C to +70 °C

#	Sym	Parameter	Notes	2.7 V V_{PP}		3.3 V V_{PP}		12 V V_{PP}		Unit
				Typ[1]	Max	Typ[1]	Max	Typ[1]	Max	
W16	t_{WHRH1} t_{EHRH1}	Byte Program Time	2	TBD	TBD	17	300	7.0	125	µs
		Block Program Time	2	TBD	TBD	1.1	4.0	0.5	1.5	sec
W16	t_{WHRH2} t_{EHRH2}	Block Erase Time	2	TBD	TBD	0.8	6.0	0.3	4.0	sec
W16	t_{WHRH3} t_{EHRH3}	Set Lock-Bit Time	2	TBD	TBD	21	TBD	11.6	TBD	µs
W16	t_{WHRH4} t_{EHRH4}	Clear Block Lock-Bits Time	2	TBD	TBD	1.8	TBD	1.1	TBD	sec
W16	t_{WHRH5} t_{EHRH5}	Program Suspend Latency Time		TBD	TBD	7.1	10	7.4	10.4	µs
W16	t_{WHRH6} t_{EHRH6}	Block Erase Suspend Latency Time		TBD	TBD	15.2	21.1	12.3	17.2	µs

NOTES:

1. Typical values measured at T_A = +25 °C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled, but not 100% tested.
5. Reference the *AC Waveform for Write Operations,* Figure 18.

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6.8 Extended Temperature Operating Conditions

Except for the specifications given in this section, all DC and AC characteristics are identical to those give in commercial temperature specifications. See the Section 6.2 for commercial temperature specifications.

Extended Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Notes	Min	Max	Unit	Test Condition
T_A	Operating Temperature		–40	+85	°C	Ambient Temperature

6.9 DC Characteristics—Extended Temperature

T_A = –40 °C to +85 °C

Sym	Parameter	Notes	2.7 V V_{CC}		3.3 V V_{CC}		Unit	Test Conditions
			Typ	Max	Typ	Max		
I_{CCD}	V_{CC} Deep Power-Down Current	1		20		20	µA	RP# = GND ± 0.2 V I_{OUT} (RY/BY#) = 0 mA

NOTE:

1. All currents are in RMS unless otherwise noted. These currents are valid for all product versions (packages and speeds). Contact Intel's Application Support Hotline or your local sales office for information about typical specifications.

6.10 AC Characteristics—Read-Only Operations[1, 3]—Extended Temperature

T_A = –40 °C to +85 °C

Versions[3]				3.3 V ± 0.3 V V_{CC}		–150		—		Unit
				2.7 V–3.6 V V_{CC}		—		–170		
#	Sym	Parameter	Notes	Min	Max	Min	Max			
R1	t_{AVAV}	Read Cycle Time		150		170		ns		
R2	t_{AVQV}	Address to Output Delay			150		170	ns		
R3	t_{ELQV}	CE# to Output Delay	2		150		170	ns		

NOTES:

1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. OE# may be delayed up to t_{ELQV}–t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
3. See *Ordering Information* for device speeds (valid operational combinations).

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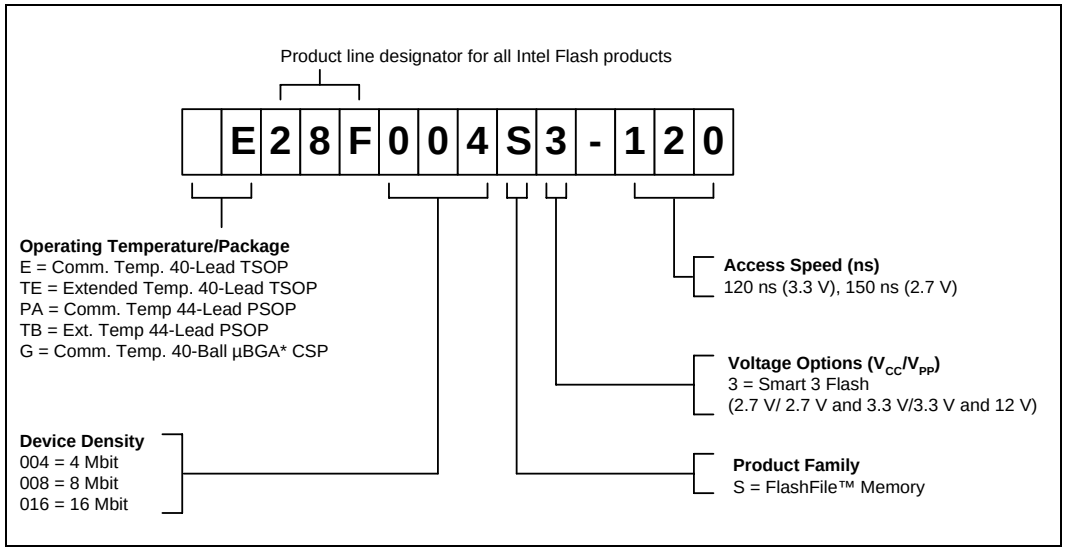
7.0 ORDERING INFORMATION



Order Code by Density[1]			Valid Operational Combinations	
4 Mbit	**8 Mbit**	**16 Mbit**	**2.7V–3.6V V_{CC} 50 pF load**	**3.3V ± 0.3V V_{CC} 50 pF load**
Commercial Temperature				
E28F004S3-120	E28F008S3-120	E28F016S3-120	–150	–120
E28F004S3-150	E28F008S3-150	E28F016S3-150	–170	–150
PA28F004S3-120	PA28F008S3-120	PA28F016S3-120	–150	–120
PA28F004S3-150	PA28F008S3-150	PA28F016S3-150	–170	–150
	G28F008S3-120	G28F016S3-120	–150	–120
	G28F008S3-150	G28F016S3-150	–170	–150
Extended Temperature				
TE28F004S3-150	TE28F008S3-150	TE28F016S3-150	–170	–150
TB28F004S3-150	TB28F008S3-150	TB28F016S3-150	–170	–150

NOTE:

1. Contact your local Intel or distribution sales office to order components with 2.7 V V_{PP} capability.

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8.0 ADDITIONAL INFORMATION

Order Number	Document/Tool
290597	*5 Volt FlashFile™ Memory; 28F004S5, 28F008S5, 28F016S5* datasheet
292182	*AP-627 Byte-Wide FlashFile™ Memory Family Software Drivers*
292123	*AP-374 Flash Memory Write Protection Techniques*
297799	*3 Volt FlashFile™ Memory; 28F004S3, 28F008S3, 28F016S3 Specification Update*
Note 3	*AP-625 28F008SC Compatibility with 28F008SA*
Note 3	*AP-364 28F008SA Automation and Algorithms*
Note 3	*AP-359 28F008SA Hardware Interfacing*
Note 3	*AB-64 4-, 8-, 16-Mbit Byte-Wide FlashFile™ Memory Family Overview*
Contact Intel/Distribution Sales Office	4-, 8-, and 16-Mbit Schematic Symbols
Contact Intel/Distribution Sales Office	4-, 8-, and 16-Mbit TimingDesigner* Files
Contact Intel/Distribution Sales Office	4-, 8-, and 16-Mbit VHDL and Verilog Models
Contact Intel/Distribution Sales Office	4-, 8-, and 16-Mbit iBIS Models

NOTES:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com for technical documentation and tools.
3. These documents can be located at the Intel World Wide Web support site, http://www.intel.com/support/flash/memory

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