3 Volt Fast Boot Block Flash Memory

28F800F3—Automotive

Preliminary Datasheet

Product Features

- High Performance
  - — Up to 50 MHz Effective Zero Wait-State Performance
  - — Synchronous Burst-Mode Reads
  - — Asynchronous Page-Mode Reads
- SmartVoltage Technology
  - — 3.0 V–3.6 V Read and Write Operations for Low Power Designs
  - — 12 V V_{PP} Fast Factory Programming
- Enhanced Data Protection
  - — Absolute Write Protection with V_{PP} = GND
  - — Block Locking
  - — Block Erase/Program Lockout during Power Transitions
- Manufactured on ETOX™ V Flash Technology
- Supports Code Plus Data Storage
  - — Optimized for Flash Data Integrator (FDI) and other Intel® Software
  - — Fast Program Suspend Capability
  - — Fast Erase Suspend Capability
- Flexible Blocking Architecture
  - — Eight 4-Kword Blocks for Data
  - — 32-Kword Main Blocks for Code
  - — Top or Bottom Boot Configurations
- Extended Cycling Capability
- Low Power Consumption
- Automated Program and Block Erase Algorithms
  - — Command User Interface for Automation
  - — Status Register for System Feedback
- Industry-Standard Packaging
  - — 56-Lead SSOP
  - — Intel® Easy BGA

The Intel® 3 Volt Fast Boot Block Flash memory offers the highest performance synchronous burst reads—making it an ideal memory solution for burst CPUs. The Intel 3 Volt Fast Boot Block Flash memory also supports asynchronous page mode operation for non-clocked memory subsystems. Combining high read performance with the intrinsic nonvolatility of flash memory eliminates the traditional redundant memory paradigm of shadowing code from a slower nonvolatile storage source to a faster execution memory device, (e.g., SRAM SDRAM), for improved system performance. By adding 3 Volt Fast Boot Block Flash memory to your system you could reduce the total memory requirement, which helps increase reliability and reduce overall system power consumption—all while reducing system cost.

This family of products is manufactured on Intel® 0.4 µm ETOX™ V process technology. They are available in a wide variety of industry-standard packaging technologies.

Notice: This document contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

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PRELIMINARY

Contents

Revision History

Date of Revision	Version	Description
10/01/99	-001	Original version
08/03/00	-002	Removed all references to 5 V and 1.65 V I/O capability. Removed -125 ns device and added 80ns device. Changed t_{CHQV} time from 19 ns to 17 ns. Changed t_{APA} time from 35 ns to 25 ns. Changed $t_{EHQZ/GHQV}$ time from 25 ns to 23 ns. Changed t_{DVWH} time from 70 ns to 63 ns. Changed block program and erase times in Table 8.8. Minor text edits.
03/26/01	-003	Changed t_{CHQV} time for –95 device from 10ns to 19ns in Table 8.5, *AC Characteristics—Read-Only Operations* [1,2] *—Automotive Temperature* Revised Table 8.8, *Automotive Temperature Block Erase and Program Performance* [1,2,3]

1.0 Introduction

This datasheet contains 8-Mbit 3 Volt Intel® Fast Boot Block Flash memory information. Section 1.0 provides a flash memory overview. Sections 2.0 through 8.0 describe the memory functionality and electrical specifications for automotive temperature product offerings.

1.1 Product Overview

The 3 Volt Fast Boot Block Flash memory provides density upgrades with pinout compatibility for 8-Mbit densities. This family of products is a high-performance, low-voltage memory with a 16-bit data bus and individually erasable blocks. These blocks are optimally sized for code and data storage. Eight 4-Kword parameter blocks are positioned at either the top (denoted by -T suffix) or bottom (denoted by -B suffix) of the address map. The rest of the device is grouped into 32-Kword main blocks. The upper two (or lower two) parameter blocks, and all main blocks, can be locked when WP# = V_{IL} for complete code protection.

The device's optimized architecture and interface dramatically increase read performance. It supports synchronous burst reads and asynchronous page mode reads from main blocks (parameter blocks support single synchronous and asynchronous reads). Upon initial power-up or return from reset, the main blocks of the device default to a page-mode. Page-mode is for non-clocked memory systems and is compatible with page-mode ROM. Synchronous burst reads are enabled by configuring the Read Configuration Register using the standard two-bus-cycle algorithm. In synchronous burst mode, the CLK input increments an internal burst address generator, synchronizes the flash memory with the host CPU, and outputs data on every rising (or falling) CLK edge up to 50 MHz. An output signal, WAIT#, is also provided to ease CPU-to-flash memory communication and synchronization during continuous burst operations that are not initiated on a four-word boundary.

In addition to the enhanced architecture and optimized interface, this family of products incorporates SmartVoltage technology which enables fast 12 Volt factory programming and 3.0 V–3.6 V in system programming for low power designs. Specifically designed for low-voltage systems, 3 Volt Fast Boot Block Flash memory components support read, write and erase operations at 3.0 V–3.6 V. The 12 V V_{PP} option renders the fastest program performance to increase factory programming throughput. With the 3.0 V–3.6 V V_{PP} option, V_{CC} and V_{PP} can be tied together for a simple, low power design. In addition to the voltage flexibility, the dedicated V_{PP} pin gives complete data protection when $V_{PP} \leq V_{PPLK}$.

The flexible input/output (I/O) voltage feature of the device helps reduce system power consumption and simplifies interfacing to sub 3.0 V CPUs. Powered by the V_{CCQ} pins, the I/O buffers can operate independently of the core voltage. The Flexible I/O ring of the device works in the following mode:

- With V_{CC} and V_{CCQ} at 3.0 V–3.6 V the device is an ideal fit for single supply voltage, low power, and battery-powered applications.

The device's Command User Interface (CUI) serves as the interface between the system processor and internal flash memory operation. A valid command sequence written to the CUI initiates device automation. This automation is controlled by an internal Write State Machine (WSM) which automatically executes the algorithms and timings necessary for block erase and program operations. The status register provides WSM feedback by signifying block erase or program completion and status.

Block erase and program automation allows erase and program operations to be executed using an industry-standard two-write command sequence. A block erase operation erases one block at a time, and data is programmed in word (16 bit) increments. The erase suspend feature allows system software to suspend an ongoing block erase operation in order to read from or program data to any other block. The program suspend feature allows system software to suspend an ongoing program operation in order to read from any other location.

The 3 Volt Fast Boot Block Flash memory devices offer two low-power savings features: Automatic Power Savings (APS) and standby mode. The device automatically enters APS mode following the completion of a read cycle. Standby mode is initiated when the system deselects the device by driving CE# inactive or RST# active. RST# also resets the device to read array, provides write protection, and clears the status register. Combined, these two features significantly reduce power consumption.

2.0 Product Description

This section describes the pinout and block architecture of the device family.

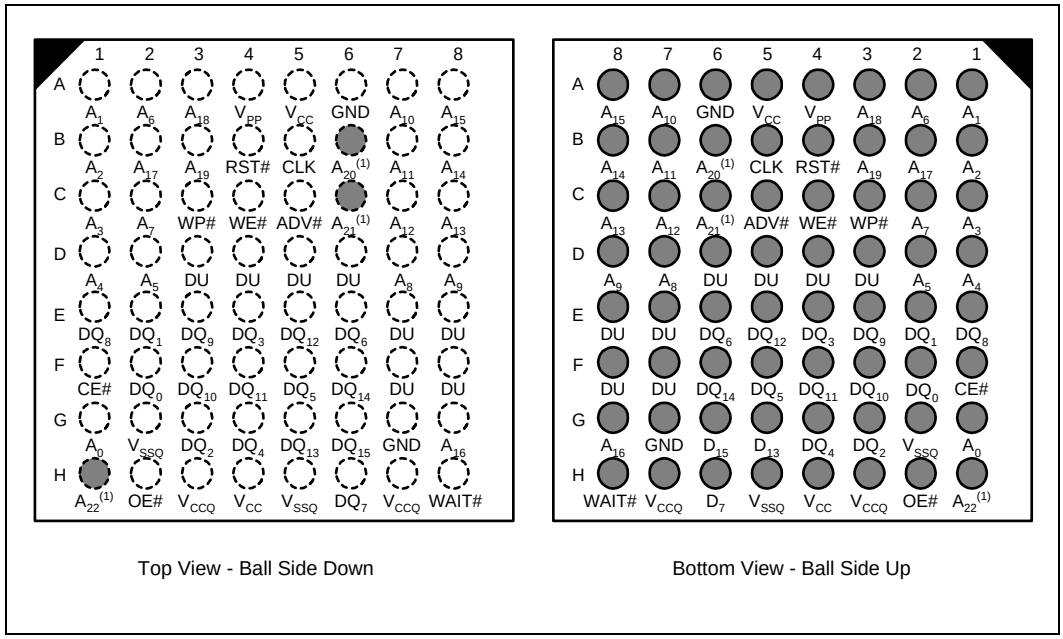
2.1 Pinouts

Intel 3 Volt Fast Boot Block Flash memory provides upgrade paths in each package pinout up to the 8-Mbit density. The family is available in Easy BGA and 56-lead SSOP packages. Ballout for the Easy BGA is illustrated in Figure 1 on page 3. Pinout for the 8-Mbit, 56-Lead SSOP is illustrated in Figure 2 on page 4.

2.2 Pin Description

The pin description table describes pin usage.

Figure 1. 8 x 8 Easy BGA Package Ballout

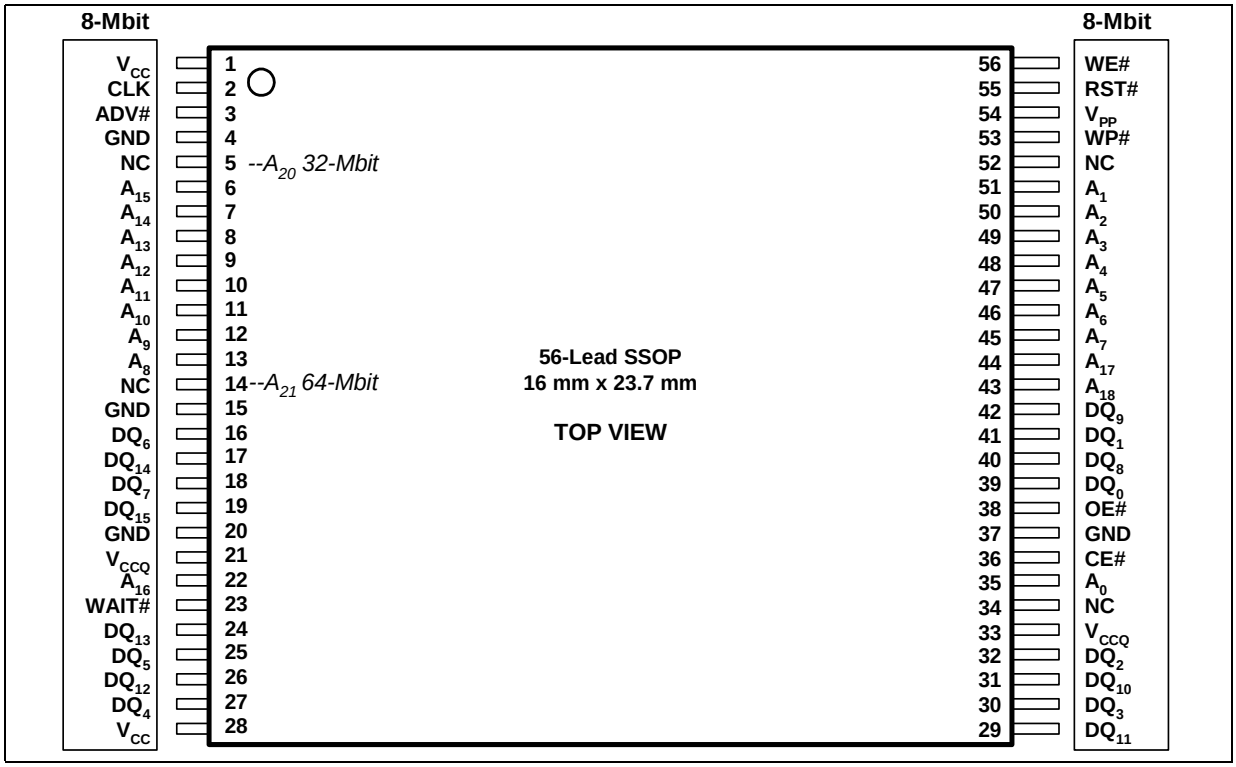


EasyPin01

NOTES:

1. A_{20} is only valid on 32-Mbit densities and above, A_{21} is only valid on 64-Mbit densities and above, A_{22} is only valid on 128-Mbit densities and above. All locations are populated with solder balls.
2. Shaded connections on the Top View indicate possible future upgrade address connections.
3. Reference the *Preliminary Mechanical Specification for Easy BGA Package* at the Intel® Flash Packaging Data website, http://developer.intel.com/design/flash/packdata/index.htm, for detailed package specifications.

Figure 2. SSOP Pinout



NOTE: A_{20} and A_{21} are the upgrade addresses for potential 32-Mbit and 64-Mbit devices.

Table 1. Pin Descriptions (Sheet 1 of 2)

Sym	Type	Name and Function
A_0–A_{19}	INPUT	**ADDRESS INPUTS:** Inputs for addresses during read and write operations. Addresses are internally latched during read and write cycles. 8-Mbit: $A_{0–18}$
$DQ_{0–}$ DQ_{15}	INPUT/ OUTPUT	**DATA INPUT/OUTPUTS:** Inputs data and commands during write cycles, outputs data during memory array, status register (DQ_0–DQ_7), and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle.
CLK	INPUT	**CLOCK:** Synchronizes the flash memory to the system operating frequency during synchronous burst mode read operations. When configured for synchronous burst-mode reads, the address is latched on the first rising (or falling, depending upon the read configuration register setting) CLK edge when ADV# is active or upon a rising ADV# edge, whichever occurs first. CLK is ignored during asynchronous page-mode read and write operations.
ADV#	INPUT	**ADDRESS VALID:** Indicates that a valid address is present on the address inputs. Addresses are latched on the rising edge of ADV# during read and write operations. ADV# may be tied active during asynchronous read and write operations.
CE#	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders, and sense amplifiers. CE#-high deselects the device and reduces power consumption to standby levels.
RST#	INPUT	**RESET:** When driven low, RST# inhibits write operations which provides data protection during power transitions, and it resets internal automation. RST#-high enables normal operation. Exit from reset sets the device to asynchronous read array mode.
OE#	INPUT	**OUTPUT ENABLE:** Gates data outputs during a read cycle.

Table 1. Pin Descriptions (Sheet 2 of 2)

Sym	Type	Name and Function
WE#	INPUT	**WRITE ENABLE:** Controls writes to the CUI and array. Addresses and data are latched on the rising edge of the WE# pulse.
WP#	INPUT	**WRITE PROTECTION:** Provides a method for locking and unlocking all main blocks and two parameter blocks. When WP# is at logic low, lockable blocks are locked. If a program or erase operation is attempted on a locked block, SR.1 and either SR.4 [program] or SR.5 [block erase] will be set to indicate the operation failed. When WP# is at logic high, the lockable blocks are unlocked and can be programmed or erased.
WAIT#	OUTPUT	**WAIT:** Provides data valid feedback only when configured for synchronous burst mode and the burst length is set to continuous. This signal is gated by OE# and CE# and is internally pull-up to V_{CCQ} via a resistor. WAIT# from several components can be tied together to form one system WAIT# signal.
V_{PP}	SUPPLY	**BLOCK ERASE AND PROGRAM POWER SUPPLY (3.0 V–3.6 V, 11.4 V–12.6 V):** For erasing array blocks or programming data, a valid voltage must be applied to this pin. With $V_{PP} \le V_{PPLK}$, memory contents cannot be altered. Block erase and program with an invalid V_{PP} voltage should not be attempted. Applying 11.4 V–12.6 V to V_{PP}can only be done for a maximum of 1000 cycles on main blocks and 2500 cycles on the parameter blocks. V_{PP} may be connected to 12 V for a total of 80 hours maximum (see Section 6.0 for details).
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY (3.0 V–3.6 V):** With $V_{CC} \le V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltages should not be attempted.
V_{CCQ}	SUPPLY	**OUTPUT POWER SUPPLY (3.0 V–3.6 V):** Enables all outputs to be driven to 3.0 V to 3.6 V.
GND	SUPPLY	**GROUND:** Do not float any ground pins.
NC		**NO CONNECT:** Lead is not internally connected; it may be driven or floated. (Pins noted as possible upgrades to 32-Mbit and 64-Mbit densities can be connected to the appropriate address lines to pre-enable designs for possible future devices.).

2.3 Memory Blocking Organization

The 3 Volt Fast Boot Block Flash memory family is an asymmetrically-blocked architecture that enables system integration of code and data within a single flash device. For the address locations of each block, see the memory maps in Figure 3, “8- Mbit Top Boot and Bottom Boot Memory Map” on page 6. 8-Mbit Top Boot and Bottom Boot Blocking.

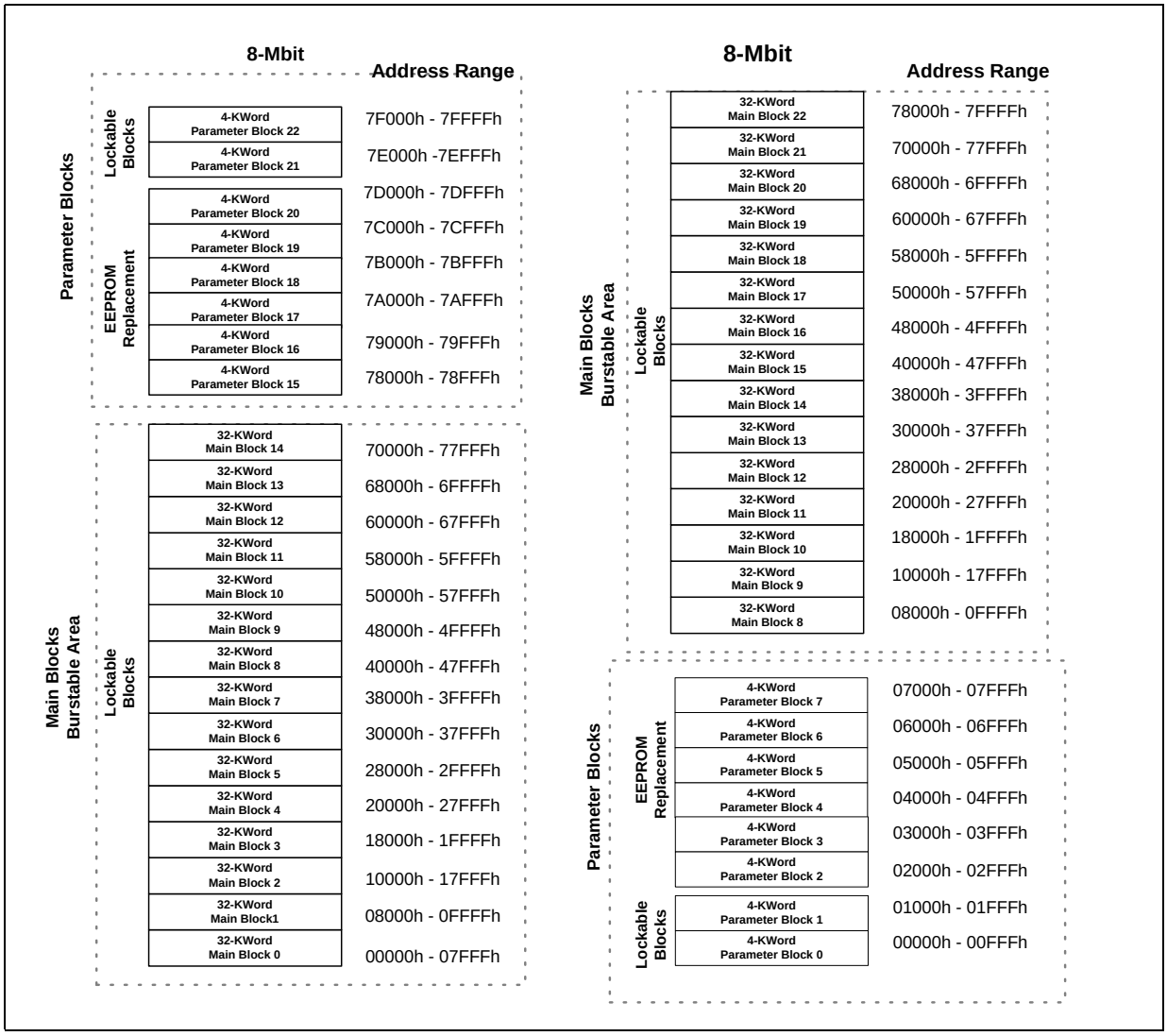
2.3.1 Parameter Blocks

The 3 Volt Fast Boot Block Flash memory architecture includes parameter blocks to facilitate storage of frequently updated small parameters that would normally be stored in an EEPROM. By using software techniques, the word-rewrite functionality of EEPROMs can be emulated. Each 8- Mbit device contains eight 4-Kwords (4,096-words) parameter blocks.

2.3.2 Main Blocks

After the parameter blocks, the remainder of the array is divided into equal size main blocks for code and/or data storage. The main blocks are the area of the device that support four-, eight-, and continuous burst operations. The 8-Mbit device contains fifteen 32-Kword (32,768-word) main blocks.

Figure 3. 8- Mbit Top Boot and Bottom Boot Memory Map



3.0 Principles of Operation

The 3 Volt Fast Boot Block Flash memory components include an on-chip Write State Machine (WSM) to manage block erase and program. It allows for CMOS-level control inputs, fixed power supplies, and minimal processor overhead with RAM-like interface timings.

3.1 Bus Operations

The local CPU reads and writes flash memory in-system. All flash memory read and write cycles conform to standard microprocessor bus cycles.

3.1.1 Read

The flash memory has three read modes available: read array, identifier codes, and status register. These modes are accessible independent of the V_{PP} voltage. The appropriate read command (Read Array, Read Identifier Codes, or Read Status Register) must be written to the CUI to enter the requested read mode. Upon initial power-up or exit from reset, the device defaults to read array mode.

When reading information from main blocks in read array mode, the device supports two high-performance read configurations: synchronous burst mode and asynchronous page mode. Page mode and synchronous burst-mode reads are enabled by writing the Set Read Configuration Register command to any device address.

Synchronous burst mode is enabled by writing to the read configuration register. This sets the read configuration, burst order, burst length, and frequency configuration. In synchronous burst mode, the device latches the initial address then outputs a sequence of data with respect to the input CLK and read configuration setting. Synchronous burst reads can be terminated after one cycle in main blocks. Asynchronous page mode is the default state and provides a high data transfer rate for non-clocked memory subsystems. In this state, data is internally read and stored in a high-speed page buffer. $A_{1:0}$ addresses data in the page buffer. The page size is four words.

Read operations from the parameter blocks, identifier codes and status register transpire as single-synchronous or asynchronous read cycles. The read configuration register setting determines whether or not read operations are synchronous or asynchronous.

For all read operations, CE# must be driven active to enable the devices, ADV# must be driven low to open the internal address latch, and OE# must be driven low to activate the outputs. In asynchronous mode, the address is latched when ADV# is driven high. In synchronous mode, the address is latched by ADV# going high or ADV# low in conjunction with a rising (falling) clock edge, whichever occurs first. WE# must be at V_{IH}. Figure 14 through Figure 19 illustrate the different read cycles.

3.1.2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins DQ_0–DQ_{15} are placed in a high-impedance state.

3.1.3 Standby

Deselecting the device by bringing CE# to a logic-high level (V_{IH}) places the device in standby mode, which substantially reduces device power consumption. In standby, outputs are placed in a high-impedance state independent of OE#. If deselected during program or erase operation, the device continues to consume active power until the program or erase operation is complete.

3.1.4 Write

Commands are written to the CUI using standard microprocessor write timings when ADV#, WE#, and CE# are active and OE# is inactive. The CUI does not occupy an addressable memory location. The address is latched on the rising edge of ADV#, WE#, or CE# (whichever occurs first) and data needed to execute a command is latched on the rising edge of WE# or CE# (whichever goes high first). Write operations are asynchronous. Therefore, CLK is ignored during write operations. Figure 20, “AC Waveform for Write Operations” on page 39 illustrates a write operation.

3.1.5 Reset

The device enters a reset mode when RST# is driven low. In reset mode, internal circuitry is turned off and outputs are placed in a high-impedance state.

After return from reset, a time t_{PHQV} is required until outputs are valid, and a delay (t_{PHWL} or t_{PHEL}) is required before a write sequence can be initiated. After this wake-up interval, normal operation is restored. The device defaults to read array mode, the status register is set to 80H, and the read configuration register defaults to asynchronous page-mode reads.

If RST# is taken low during a block erase or program operation, the operation will be aborted and the memory contents at the aborted location are no longer valid. See Figure 21, “AC Waveform for Reset Operation” on page 40 for detailed information regarding reset timings.

4.0 Command Definitions

Device operations are selected by writing specific commands into the CUI. Table 3 defines these commands.

Table 2. Bus Operations

Mode	Notes	RST#	CE#	ADV#	OE#	WE#	Address	V_{PP}	DQ_{0-15}
Reset		V_{IL}	X	X	X	X	X	X	High Z
Standby		V_{IH}	V_{IH}	X	X	X	X	X	High Z
Output Disable		V_{IH}	V_{IL}	X	V_{IH}	V_{IH}	X	X	High Z
Read	1,2	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}
Read Identifier Codes		V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	See Table 4	X	See Table 4
Write	3,4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}

NOTES:
1. Refer to *DC Characteristics*. When $V_{PP} \le V_{PPLK}$, memory contents can be read, but not altered.
2. X can be V_{IL} or V_{IH} for control and address input pins and V_{PPLK} or $V_{PP1/2}$ for V_{PP}. See *DC Characteristics* for V_{PPLK} and $V_{PP1/2}$ voltages.
3. Command writes involving block erase or program are reliably executed when $V_{PP} = V_{PP1/2}$ and $V_{CC} = V_{CC1/2}$ (see Section 8.0 for operating conditions at different temperatures).
4. Refer to Table 3 for valid D_{IN} during a write operation.

Table 3. Command Definitions(1)

Command	Bus Cycles Required	Notes	First Bus Cycle			Second Bus Cycle		
			Oper(2)	Addr(3)	Data(4)	Oper(2)	Addr(3)	Data(4)
Read Array/Reset	1		Write	X	FFH			
Read Identifier Codes	≥ 2	5	Write	X	90H	Read	IA	ID
Read Status Register	2		Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Block Erase	2	6,7	Write	X	20H	Write	BA	D0H
Program	2	6,7,8	Write	X	40H or 10H	Write	WA	WD
Block Erase and Program Suspend	1	6	Write	X	B0H			
Block Erase and Program Resume	1	6	Write	X	D0H			
Set Read Configuration	2		Write	RCD	60H	Write	RCD	03H

NOTES:
1. Commands other than those shown above are reserved by Intel for future device implementations and should not be used.
2. Bus operations are defined in Table 2.
3. X = Any valid address within the device.
   IA = Identifier Code Address.
   BA = Address within the block being erased.
   WA = Address of memory location to be written.
   RCD = Data to be written to the read configuration register. This data is presented to the device on A_{15-0}; set all other address inputs to "0."

4. SRD = Data read from status register. See Table 5, “Status Register Definition” on page 12 for a description of the status register bits.
   WD = Data to be written at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).
   ID = Data read from identifier codes. See Table 4 for manufacturer and device codes.
   RCD = Data to be written to read configuration register. See Table 6, “Read Configuration Register Definition” on page 14 for a description of the read configuration register bits.
5. Following the Read Identifier Codes command, read operations access manufacturer, device codes, and read configuration register.
6. Following a block erase, program, and suspend operation, read operations access the status register.
7. To issue a block erase, program, or suspend operation to a lockable block, hold WP# at V_{IH}.
8. Either 40H or 10H are recognized by the WSM as the program setup.

4.1 Read Array Command

Upon initial device power-up or exit from reset, the device defaults to read array mode. The read configuration register defaults to asynchronous page mode. The Read Array command also causes the device to enter read array mode. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase or program, the device will not recognize the Read Array command until the WSM completes its operation or unless the WSM is suspended via an Erase or Program Suspend command. The Read Array command functions independently of the V_{PP} voltage.

4.2 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. After writing the command, read cycles retrieve the manufacturer and device codes (see Table 4 for identifier code values). Page mode and burst reads are not supported in this read mode. To terminate the operation, write another valid command, like the Read Array command. The Read Identifier Codes command functions independently of the V_{PP} voltage.

Table 4. Identifier Codes

Code			Address (Hex)	Data (Hex)
Manufacturer Code			00000	0089
Device Code	8 Mbit	-T	00001	88F1
		-B	00001	88F2
Read Configuration Register			00005	RCD(1)

NOTE: 1. Read Configuration Register = RCD.

4.3 Read Status Register Command

The status register can be read at any time by writing the Read Status Register command to the CUI. After writing this command, all subsequent read operations output status register data until another valid command is written. Page mode and burst reads are not supported in this read mode. The status register content is updated and latched on the rising edge of ADV# or rising (falling)

CLK edge when ADV# is low during synchronous burst mode or the falling edge of OE# or CE#, whichever occurs first. The Read Status Register command functions independently of the V_{PP} voltage.

4.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3, and SR.1 are set to "1"s by the WSM and can only be cleared by issuing the Clear Status Register command. These bits indicate various error conditions. By allowing system software to reset these bits, several operations may be performed (such as cumulatively erasing or writing several bytes in sequence). The status register may be polled to determine if a problem occurred during the sequence. The Clear Status Register command functions independently of the applied V_{PP} voltage. After executing this command, the device returns to read array mode.

4.5 Block Erase Command

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is written first, followed by a block erase confirm. This command sequence requires appropriate sequencing and address within the block to be erased (erase changes all block data to FFH). Block preconditioning, erase, and verify are handled internally by the WSM. After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 7, "Automated Block Erase Flowchart" on page 20). The CPU can detect block erase completion by analyzing status register bit SR.7.

When the block erase completes, check status register bit SR.5 for an error flag ("1"). If an error is detected, check status register bits SR.4, SR.3, and SR.1 to understand what caused the failure. After examining the status register, it should be cleared if an error was detected before issuing a new command. The device will remain in status register read mode until another command is written to the CUI.

Table 5. Status Register Definition

WSMS	ESS	ES	PS	VPPS	PSS	DPS	R
7	6	5	4	3	2	1	0

	NOTES:
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Check SR.7 to determine block erase or program completion. SR.6–0 are invalid while SR.7 = “0.”
SR.6 = ERASE SUSPEND STATUS (ESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	When an Erase Suspend command is issued, the WSM halts execution and sets both SR.7 and SR.6 to “1.” SR.6 remains set until an Erase Resume command is written to the CUI.
SR.5 = ERASE STATUS (ES) 1 = Error in Block Erasure 0 = Successful Block Erase	If both SR.5 and SR.4 are “1”s after a block erase or program attempt, an improper command sequence was entered.
SR.4 = PROGRAM STATUS (PS) 1 = Error in Program 0 = Successful Program	
SR.3 = V_{PP} STATUS (VPPS) 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK	SR.3 does not provide a continuous V_{PP} feedback. The WSM interrogates and indicates the V_{PP} level only after a block erase or program operation. SR.3 is not guaranteed to report accurate feedback when $V_{PP} \neq V_{PPH1/2}$ or V_{PPLK}.
SR.2 = PROGRAM SUSPEND STATUS (PSS) 1 = Program Suspended 0 = Program in Progress/Completed	When a Program Suspend command is issued, the WSM halts execution and sets both SR.7 and SR.2 to “1.” SR.2 remains set until a Program Resume command is written to the CUI.
SR.1 = DEVICE PROTECT STATUS (DPS) 1 = Block Erase or Program Attempted on a Locked Block, Operation Abort 0 = Unlocked	If a block erase or program operation is attempted on a locked block, SR.1 is set by the WSM and aborts the operation if WP# = V_{IL}.
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	SR.0 is reserved for future use and should be masked out when polling the status register.

4.6 Program Command

Program operation is executed by a two-cycle command sequence. Program setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data. The WSM then takes over, controlling the internal program algorithm. After the program sequence is written, the device automatically outputs status register data when read (see Figure 8, “Automated Program Flowchart” on page 21). The CPU can detect the completion of the program event by analyzing status register bit SR.7.

When the program operation completes, check status register bit SR.4 for an error flag (“1”). If an error is detected, check status register bits SR.5, SR.3, and SR.1 to understand what caused the problem. After examining the status register, it should be cleared if an error was detected before issuing a new command. The device will remain in status register read mode until another command is written to the CUI.

4.7 Block Erase Suspend/Resume Command

The Block Erase Suspend command allows block erase interruption to read or program data in another block. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase operation after a certain latency period. The device continues to output status register data when read after the Block Erase Suspend command is issued. Status Register bits SR.7 and SR.6 indicate when the block erase operation has been suspended (both will be set to "1"). Specification t_{WHRH2} defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A Program command sequence can also be issued during erase suspend to program data in other blocks. Using the Program Suspend command (see Section 4.8), a program operation can be suspended during an erase suspend. The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume.

During a block erase suspend, the chip can go into a pseudo-standby mode by taking CE# to V_{IH}, which reduces active current draw. V_{PP} must remain at $V_{PP1/2}$ while block erase is suspended. WP# must also remain at V_{IL} or V_{IH}.

To resume the block erase operation, write the Block Erase Resume command to the CUI. This will automatically clear status register bits SR.6 and SR.7. After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 9, "Block Erase Suspend/Resume Flowchart" on page 22). Block erase cannot resume until program operations initiated during block erase suspend have completed.

4.8 Program Suspend/Resume Command

The Program Suspend command allows program interruption to read data in other flash memory locations. Once the program process starts, writing the Program Suspend command requests that the WSM suspend the program operation after a certain latency period. The device continues to output status register data when read after issuing the Program Suspend command. Status register bits SR.7 and SR.2 indicate when the Program operation has been suspended (both will be set to "1"). Specification t_{WHRH1} defines the program suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. The only other valid commands while Program is suspended are Read Status Register and Program Resume.

During a program suspend, the chip can go into a pseudo-standby mode by taking CE# to V_{IH}, which reduces active current draw. V_{PP} must remain at $V_{PP1/2}$ while program is suspended. WP# must also remain at V_{IL} or V_{IH}.

To resume the program, write the Program Resume command to the CUI. This will automatically clear status register bits SR.7 and SR.2. After the Program Resume command is written, the device automatically outputs status register data when read (see Figure 10, "Program Suspend/Resume Flowchart" on page 23).

Table 6. Read Configuration Register Definition

RM	R	FC2	FC1	FC0	R	DOC	WC
15	14	13	12	11	10	9	8
BS	CC	R	R	R	BL2	BL1	BL0
7	6	5	4	3	2	1	0

	NOTES:
RCR.15 = READ MODE (RM) 0 = Synchronous Burst Reads Enabled 1 = page mode Reads Enabled (Default)	Read mode configuration affects reads from main blocks. Parameter block, status register, and identifier reads support single read cycles.
RCR.14 = RESERVED FOR FUTURE ENHANCEMENTS (R)	These bits are reserved for future use. Set these bits to “0.”
RCR.13–11 = FREQUENCY CONFIGURATION (FC2-0) 001 = Code 1 reserved for future use 010 = Code 2 011 = Code 3 100 = Code 4 101 = Code 5 110 = Code 6	See Section 4.9.2 for information about the frequency configuration and its effect on the initial read. Undocumented combinations of bits RCR.14–11 are reserved by Intel Corporation for future implementations and should not be used.
RCR.10 = RESERVED FOR FUTURE ENHANCEMENTS (R)	These bits are reserved for future use. Set these bits to “0.”
RCR.9 = DATA OUTPUT CONFIGURATION (DOC) 0 = Hold Data for One Clock 1 = Hold Data for Two Clocks	Undocumented combinations of bits RCR.10–9 are reserved by Intel Corporation for future implementations and should not be used.
RCR.8 = WAIT CONFIGURATION (WC) 0 = WAIT# Asserted During Delay 1 = WAIT# Asserted One Data Cycle Before Delay	
RCR.7 = BURST SEQUENCE (BS) 0 = Intel Burst Order 1 = Linear Burst Order	
RCR.6 = CLOCK CONFIGURATION (CC) 0 = Burst Starts and Data Output on Falling Clock Edge 1 = Burst Starts and Data Output on Rising Clock Edge	
RCR.5–3 = RESERVED FOR FUTURE ENHANCEMENTS (R)	These bits are reserved for future use. Set these bits to “0.”
RCR.2–0 = BURST LENGTH (BL2–0) 001 = 4 Word Burst 010 = 8 Word Burst 111 = Continuous Burst	In the asynchronous page mode, the burst length always equals four words. Undocumented combinations of bits RCR.2–0 are reserved by Intel Corporation for future implementations and should not be used

4.9 Set Read Configuration Command

The Set Read Configuration command writes data to the read configuration register. This operation is initiated by a standard two bus cycle command sequence. The Read Configuration Setup command (60H) is written and the data to be written to the read configuration is presented, which is then followed by a second write that confirms the operation and again presents the data to be written to the read configuration register. The read configuration register data is placed on the address bus, $A_{15:0}$,during both bus cycles and is latched on the rising edge of ADV#, CE#, or WE# (whichever occurs first). The read configuration register data sets the device’s read configuration, burst order, frequency configuration, burst length and all other parameters. This command functions independently of the applied V_{PP} voltage. After executing this command, the device returns to read array mode.

4.9.1 Read Configuration – (RCR.15)

The device supports two high performance read configurations: Synchronous burst mode and asynchronous page mode. Bit RCR.15 in the read configuration register sets the read configuration to either synchronous burst or asynchronous page mode. Asynchronous page mode is the default read configuration state.

Parameter blocks, status register, and identifier modes only support single-synchronous and asynchronous read operations.

4.9.2 Frequency Configuration Code Setting (FCC) – (RCR.13-11)

The frequency configuration code setting informs the device of the number of clocks that must elapse after ADV# is driven active before data will be available. This value is determined by the input clock frequency and the set up and hold requirements of the target system. See Table 7, “Frequency Configuration Settings” on page 17 for the specific input CLK frequency configuration codes. The frequency configuration codes in Table 7 are derived from equations (1), (2) and (3) with assumed values for the t_{AVQV}, t_{ADD}, t_{DATA} parameters. Below is the example of the calculation to obtain the frequency configuration code:

Flash performance can be determined by the following equations:

$$\{1/\text{Frequency (MHz)}\} = \text{CLK Period (ns)} \quad (1)$$

$$n(\text{CLK Period}) \geq t_{AVQV}\,(\text{ns}) + t_{ADD}(\text{ns}) + t_{DATA}\,(\text{ns}) \quad (2)$$

$$n\text{-}2 = \text{Frequency Configuration Code (FCC)}^{*} \quad (3)$$

n : # of Clock periods (rounded up to the next integer)

*Must use FCC = n - 1 when operating in the continous burst mode.

Parameters defined by CPU:

t_{ADD} = Clock to CE#, ADV#, or Address Valid whichever occurs last.
t_{DATA} = Data set up to Clock

Parameters defined by flash:

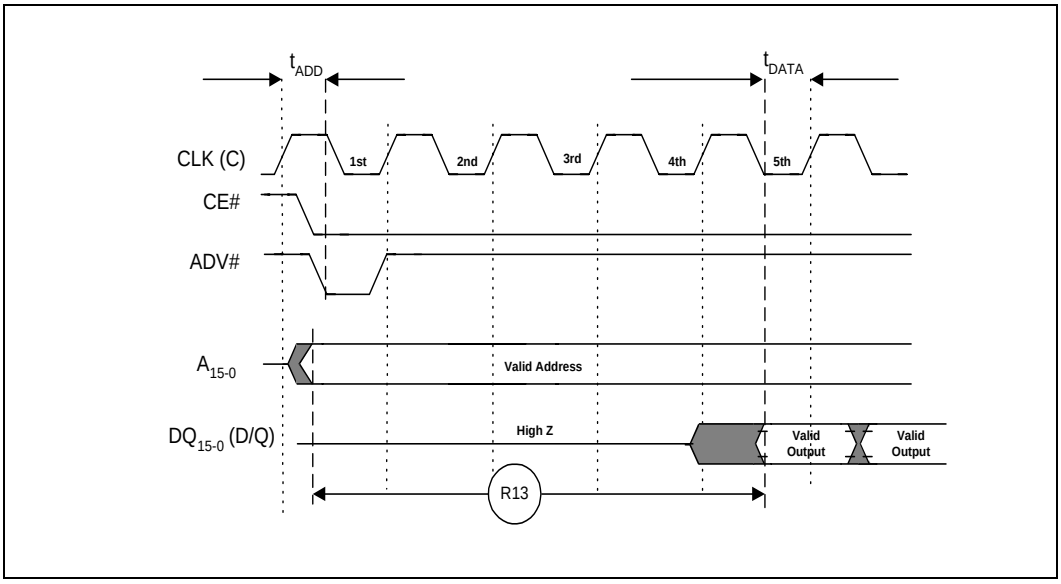
t_{AVQV} = Address to Output Delay

Example:

CPU Clock Speed = 40 MHz
t_{ADD} = 6 ns (typical speed from CPU) (max)
t_{DATA} = 4 ns (typical speed from CPU) (min)
t_{AVQV} = 95 ns (from Section 8.5 AC Characteristic - Read Only Operations Table)
From Eq. (1): $\{1/40\ (\text{MHz})\} = 25$ ns
From Eq. (2) $n(25\ \text{ns}) \geq 95\ \text{ns} + 6\ \text{ns} + 4\ \text{ns}$
$n(25\ \text{ns}) \geq 105\ \text{ns}$
$n \geq 105/25 \geq 5$ (Integer)
From Eq. (3) $n - 2 = 5 - 2 = 3$
Frequency Code Setting to the RCR is Code 3

The formula t_{AVQV} (ns) + t_{ADD}(ns) + t_{DATA} (ns) is also known as initial access time.

Figure 4. Data Output with FCC Setting at Code 3



NOTE:
1. Figure 4 shows the data output available and valid after 4 latencies from ADV# going low in the 1st clock period with the FCC setting at 3.

Figure 5 illustrates data output latency from ADV# going active for different frequency configuration codes.

Figure 5. Frequency Configuration

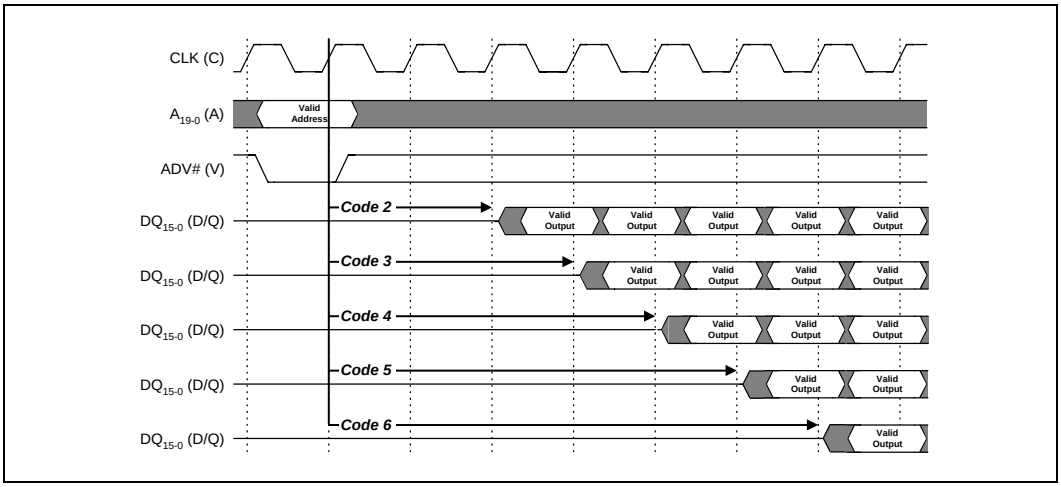


Table 7. Frequency Configuration Settings

Frequency Configuration Code	Input CLK Frequency	
	–80	–95
1	Reserved	Reserved
2	≤ 38 MHz	≤ 29 MHz
3	≤ 47 MHz	≤ 37 MHz
4	≤ 57 MHz	≤ 44 MHz
5	≤ 66 MHz	≤ 51 MHz
6	—	≤ 59 MHz

NOTE: Table derived by using formulas (1), (2) and (3) in Section 4.9.2. Values of t_{ADD}, t_{DATA} defined by CPU, assumed to be 6 ns and 4 ns respectively; value of t_{AVQV} per Section 8.5.

4.9.3 Data Output Configuration – (RCR.9)

The output configuration determines the number of clocks during which data will be held valid. The data hold time is configurable as either one or two clocks.

Subsequent reads in burst mode with zero wait-states can be defined by:

t_{CHQV} (ns) + t_{DATA} (ns) ≤ One CLK Period

In Table 7, consider the CPU clock at 40 MHz, and FCC is 3. The clock period is 25 ns. This data applied to the formula above for the subsequent reads assuming the data output hold time is one clock:

19 ns + 4 ns ≤ 25 ns

Data output will be available and valid at every clock period.

Consider the CPU frequency at 60 MHz, and FCC is 5. Clock period is 16.6 ns. The initial access time is calculated to be 125 ns (5 latencies). This condition satisfies t_{AVQV} (ns) + t_{ADD}(ns) + t_{DATA} (ns) = 95 ns + 6 ns + 4 ns = 105 ns. However, the data output hold time of one clock violates burst data output zero wait-states:

t_{CHQV} (ns) + t_{DATA} (ns) ≤ One CLK Period

19 ns + 4 ns = 23 ns is not less than one clock period. To satisfy the formula above the data output hold time must be set a 2 clocks to correctly allow for data output setup time.

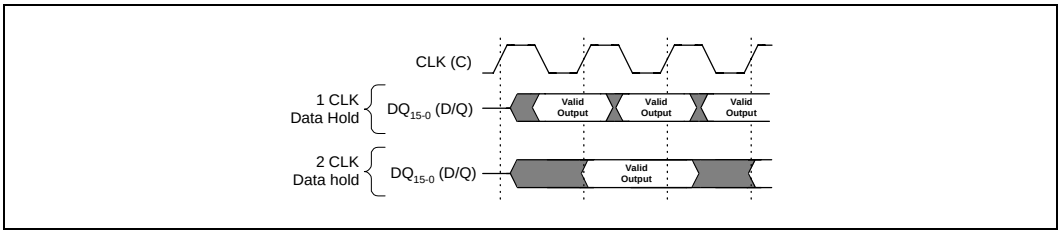
In page mode reads the initial access time can be determined by the formula:

t_{ADD} (ns) + t_{DATA} (ns) + t_{AVQV} (ns)

and subsequent reads in page mode are defined by:

t_{APA} (ns) + t_{DATA} (ns) (minimum time)

Figure 6. Output Configuration



4.9.4 Wait # Configuration – (RCR.8)

The WAIT# configuration bit controls the behavior of the WAIT# output signal. This output signal can be set to be asserted during or one CLK cycle before an output delay when continuous burst length is enabled. Its setting will depend on the system and CPU characteristic.

4.9.5 Burst Sequence – (RCR.7)

The burst sequence specifies the order in which data is addressed in synchronous burst mode. This order is programmable as either linear or Intel burst order. The continuous burst length only supports linear burst order. The order chosen will depend on the CPU characteristic. See Table 8 for more details.

Table 8. Sequence and Burst Length

Starting Addr. (Dec.)	Burst Addressing Sequence (Dec.)				
	4-Word Burst Length		8-Word Burst Length		Continuous Burst
	Linear	Intel	Linear	Intel	Linear
0	0-1-2-3	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-...
1	1-2-3-0	1-0-3-2	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6	1-2-3-4-5-6-7-...
3	2-3-0-1	2-3-0-1	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5	2-3-4-5-6-7-8-...
3	3-0-1-2	3-2-1-0	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4	3-4-5-6-7-8-9-...
4			4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-..
5			5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2	5-6-7-8-9-10-11-...
6			6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1	6-7-8-9-10-11-12-...
7			7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	7-8-9-10-11-12-13-...
8				NA	8-9-10-11-12-13-14-...
9				NA	...
15				NA	15-16-17-18-19-20-21-...

4.9.6 Clock Configuration – (RCR.6)

The clock configuration configures the device to start a burst cycle, output data, and assert WAIT# on the rising or falling edge of the clock. CLK flexibility helps ease 3 Volt Fast Boot Block Flash memory interface to a wide range of burst CPUs.

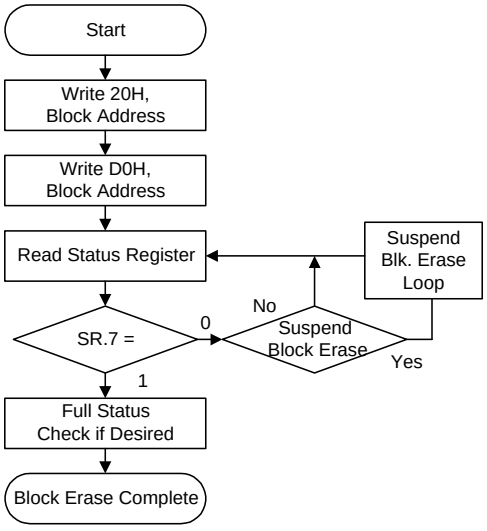
4.9.7 Burst Length – (RCR.2—0)

The burst length is the number of words that the device will output. The device supports burst lengths of four and eight words. In four- or eight-word burst configuration the device will perform a wrap around type burst access (See Table 8). It also supports a continuous burst mode. In continuous burst mode, the device will linearly output data until the internal burst counter reaches the end of the device's burstable address space. Bits RCR.2–0 in the read configuration register set the burst length.

4.9.8 Continuous Burst Length

When operating in the continuous burst mode, the flash memory may incur an output delay when the burst sequence crosses the first 16-word boundary. The starting address dictates whether or not a delay will occur. If the starting address is aligned to a four-word boundary, the delay will not be seen. If the starting address is the end of a four-word boundary, the output delay will be equal to the frequency configuration setting; this is the worst case delay. The delay will only take place once during a continuous burst access, and if the burst sequence never crosses a 16-word boundary, the delay will never happen. Using the WAIT# output pin in the continuous burst configuration, the system is informed if this output delay occurs.

Figure 7. Automated Block Erase Flowchart



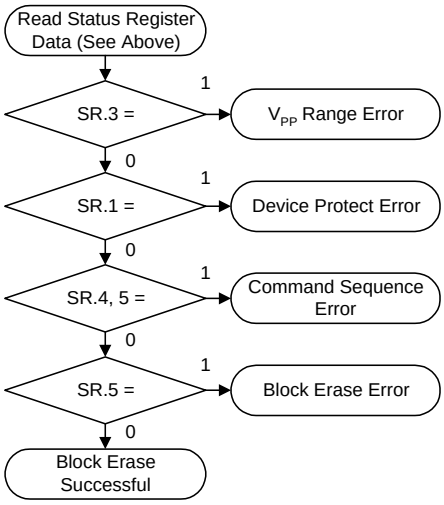
Bus Operation	Command	Comments
Write	Erase Setup	Data = 20H Addr = Within Block to Be Erased
Write	Erase Confirm	Data = D0H Addr = Within Block to Be Erased
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent block erasures.

Full status check can be done after each block erase or after a sequence of block erasures.

Write FFH after the last operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE

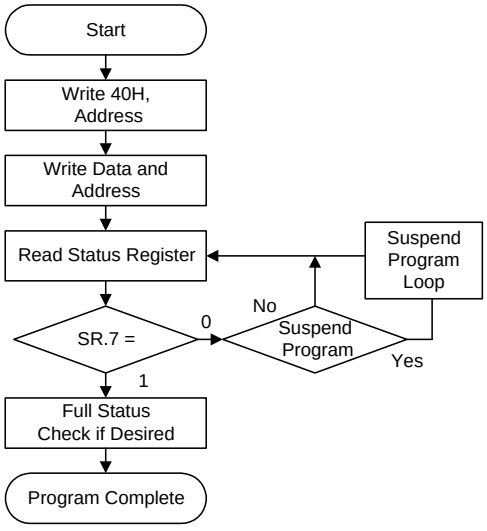


Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect WP# = V_{IL}
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error

SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Staus Register command, in cases where multiple blocks are erased before full status is checked.

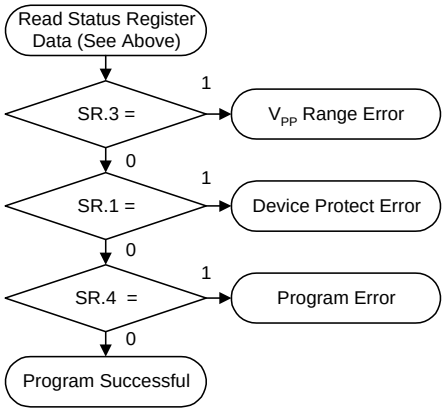
If an error is detected, clear the status register before attempting retry or other error recovery.

Figure 8. Automated Program Flowchart



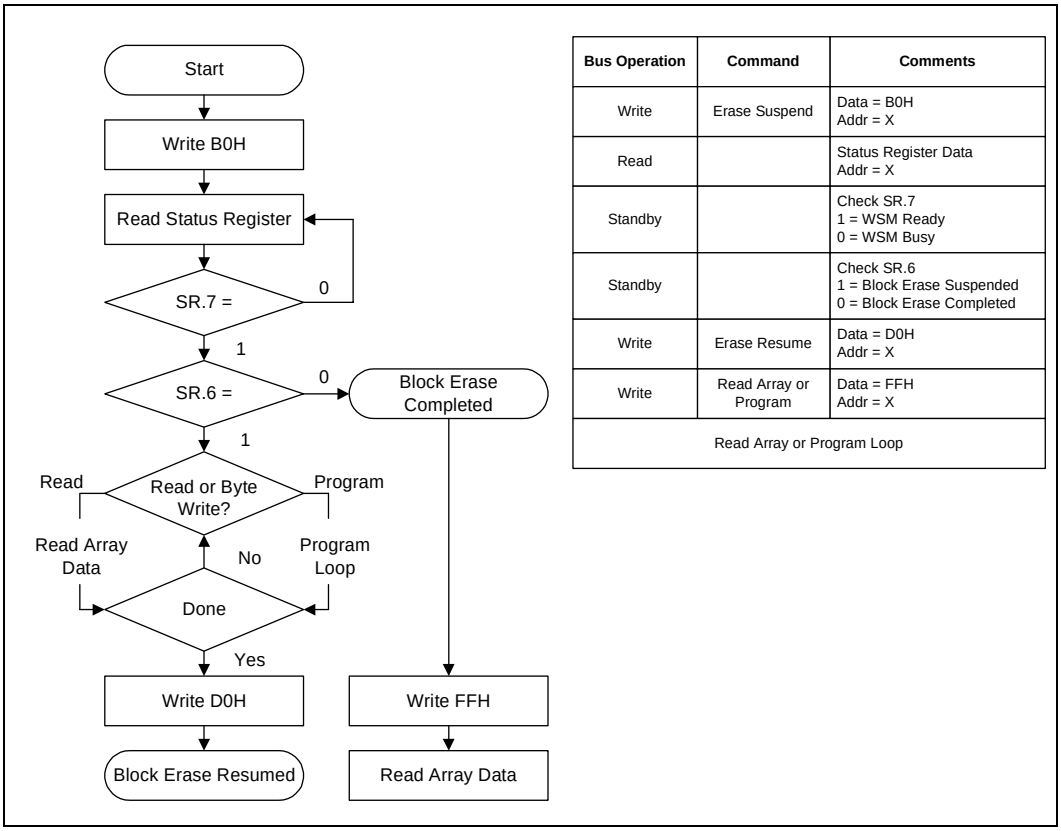
Bus Operation	Command	Comments
Write	Program Setup	Data = 40H Addr = Location to Be Written
Write	Data	Data = Data to Be Written Addr = Location to Be Written
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent byte writes. SR full status check can be done after each byte write or after a sequence of program operations. Write FFH after the last byte write operation to place device in read array mode.		

FULL STATUS CHECK PROCEDURE



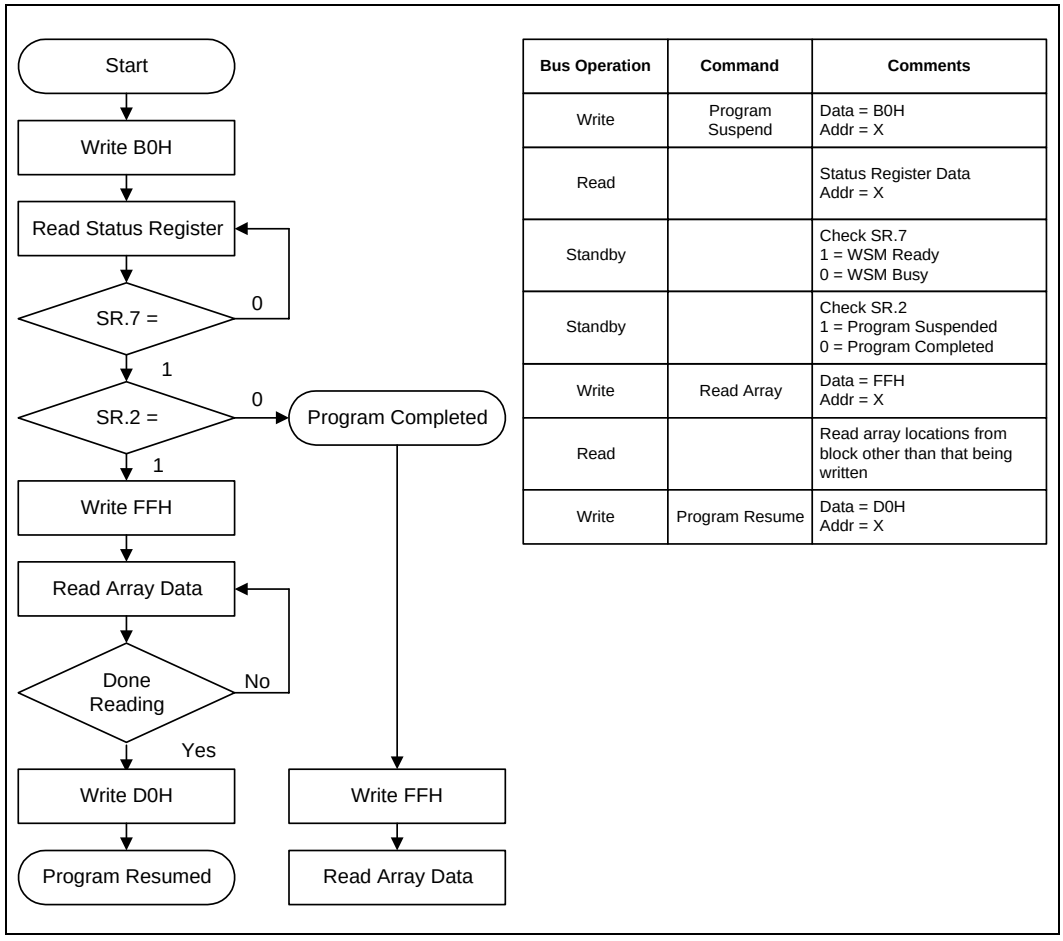
Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect WP# = V_{IL}
Standby		Check SR.4 1 = Data Write Error
SR.4, SR.3 and SR.1 are only cleared by the Clear Staus Register command, in cases where multiple locations are written before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

Figure 9. Block Erase Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Block Erase Suspended 0 = Block Erase Completed
Write	Erase Resume	Data = D0H Addr = X
Write	Read Array or Program	Data = FFH Addr = X
Read Array or Program Loop		

Figure 10. Program Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Program Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.2 1 = Program Suspended 0 = Program Completed
Write	Read Array	Data = FFH Addr = X
Read		Read array locations from block other than that being written
Write	Program Resume	Data = D0H Addr = X

5.0 Data Protection

The 3 Volt Fast Boot Block Flash memory architecture features two hardware-lockable parameter blocks, so critical code can be kept secure while six other parameter blocks can be programmed or erased as necessary to facilitate EEPROM emulation.

5.1 $V_{PP} \leq V_{PPLK}$ for Complete Protection

The V_{PP} programming voltage can be held low for complete write protection of all blocks in the flash device. When V_{PP} is below V_{PPLK}, any block erase or program operation will result in a error, prompting the corresponding status register bit (SR.3) to be set.

5.2 WP# = V_{IL} for Block Locking

The lockable blocks are locked when WP# = V_{IL}; any block erase or program operation to a locked block will result in an error, which will be reflected in the status register. For top configuration, the top two parameter blocks (blocks #21, #22) and all main blocks are lockable. For the bottom configuration, the bottom two parameter blocks (blocks #0, #1) and all main blocks are lockable. Unlocked blocks can be programmed or erased normally (unless V_{PP} is below V_{PPLK}).

5.3 WP# = V_{IH} for Block Unlocking

WP# controls all block locking and V_{PP} provides protection against spurious writes. Table 9 defines the write protection methods.

Table 9. Write Protection Truth Table

V_{PP}	WP#	RST#	Write Protection Provided
X	X	V_{IL}	All Blocks Locked
V_{IL}	X	V_{IH}	All Blocks Locked
$\geq V_{PPLK}$	V_{IL}	V_{IH}	Lockable Blocks Locked
$\geq V_{PPLK}$	V_{IH}	V_{IH}	All Blocks Unlocked

6.0 V_{PP} Voltages

Intel 3 Volt Fast Boot Block Flash memory provides in-system programming and erase at 3.0 V–3.6 V. For customers requiring fast programming in their manufacturing environment, this family of products includes an additional high-performance 12 V programming feature.

The 12 V V_{PP} mode enhances programming performance during short period of time typically found in manufacturing processes; however, it is not intended for extended use. 12 V may be applied to V_{PP} during block erase and program operations for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V_{PP} may be connected to 12 V for a total of 80 hours maximum. Stressing the device beyond these limits may cause permanent damage.

7.0 Power Consumption

While in operation, the flash device consumes active power. However, Intel® Flash devices have power savings that can significantly reduce overall system power consumption. The Automatic Power Savings (APS) feature reduces power consumption when the device is idle. When CE# is not asserted, the flash enters its standby mode, where current consumption is even lower. The combination of these features minimizes overall memory power and system power consumption.

7.1 Active Power

With CE# at a logic-low level and RST# at a logic-high level, the device is in active mode. Active power is the largest contributor to overall system power consumption. Minimizing active current has a profound effect on system power consumption, especially for battery-operated devices.

7.2 Automatic Power Savings

Automatic Power Savings (APS) provides low-power operation during active mode, allowing the flash to put itself into a low current state when not being accessed. After data is read from the memory array, the device's power consumption enters the APS mode where typical I_{CC} current is comparable to I_{CCS}. The flash stays in this static state with outputs valid until a new location is read.

7.3 Standby Power

With CE# at a logic-high level (V_{IH}) and the CUI in read mode, the flash memory is in standby mode, which disables much of the device's circuitry and substantially reduces power consumption. Outputs (DQ_0–DQ_{15}) are placed in a high-impedance state independent of the status of the OE# signal. If CE# transitions to a logic-high level during erase or program operations, the device will continue to perform the operation and consume corresponding active power until the operation is completed.

System engineers should analyze the breakdown of standby time versus active time and quantify the respective power consumption in each mode for their specific application. This will provide a more accurate measure of application-specific power and energy requirements.

7.4 Power-Up/Down Operation

The device is protected against accidental block erasure or programming during power transitions. Power supply sequencing is not required, since the device is indifferent as to which power supply, V_{PP}, V_{CC}, or V_{CCQ}, powers-up first.

7.4.1 RST# Connection

The use of RST# during system reset is important with automated program/erase devices since the system expects to read from the flash memory when it comes out of reset. If a CPU reset occurs without a flash memory reset, proper CPU initialization will not occur because the flash memory may be providing status information instead of array data. Intel recommends connecting RST# to the system reset signal to allow proper CPU/flash initialization following system reset.

System designers must guard against spurious writes when V_{CC} voltages are above V_{LKO} and V_{PP} is active. Since both WE# and CE# must be low for a command write, driving either signal to V_{IH} will inhibit writes to the device. The CUI architecture provides additional protection since alteration of memory contents can only occur after successful completion of the two-step command sequences. The device is also disabled until RST# is brought to V_{IH}, regardless of the state of its control inputs. By holding the device in reset during power-up/down, invalid bus conditions during power-up can be masked, providing yet another level of memory protection.

7.4.2 V_{CC}, V_{PP} and RST# Transitions

The CUI latches commands as issued by system software and is not altered by V_{PP} or CE# transitions or WSM actions. Its default state upon power-up, after exit from deep power-down mode or after V_{CC} transitions above V_{LKO} (Lockout voltage), is read array mode.

After any block erase or program operation is complete (even after V_{PP} transitions down to V_{PPLK}), the CUI must be reset to read array mode via the Read Array command if access to the flash memory array is desired.

7.5 Power Supply Decoupling

Flash memory's power switching characteristics require careful device de-coupling. System designers should consider three supply current issues:

- Standby current levels (I_{CCS})
- Active current levels (I_{CCR})
- Transient peaks produced by falling and rising edges of CE#.

Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper de-coupling capacitor selection will suppress these transient voltage peaks. Each flash device should have a 0.1 µF ceramic capacitor connected between each V_{CC} and GND, and between its V_{PP} and GND. These high- frequency, inherently low-inductance capacitors should be placed as close as possible to the package leads.

7.5.1 V_{PP} Trace on Printed Circuit Boards

Designing for in-system writes to the flash memory requires special consideration of the V_{PP} power supply trace by the printed circuit board designer. The V_{PP} pin supplies the flash memory cells current for programming and erasing. V_{PP} trace widths and layout should be similar to that of V_{CC}. Adequate V_{PP} supply traces, and de-coupling capacitors placed adjacent to the component, will decrease spikes and overshoots.

8.0 Electrical Specifications

8.1 Absolute Maximum Ratings

Parameter	Maximum Rating
Temperature under Bias	–40 °C to +125 °C
Storage Temperature	–65 °C to +125 °C
Voltage On Any Pin (except V_{CC}, V_{CCQ}, and V_{PP})	–0.5 V to +5.5 V(1)
V_{PP} Voltage	–0.5 V to +13.5 V(1, 2, 4)
V_{CC} and V_{CCQ} Voltage	–0.2 V to +5.0 V(1)
Output Short Circuit Current	100 mA(3)

NOTES:
1. All specified voltages are with respect to GND. Minimum DC voltage is –0.5 V on input/output pins and –0.2 V on V_{CC} and V_{PP} pins. During transitions, this level may undershoot to –2.0 V for periods <20 ns. Maximum DC voltage on input/output pins is 5.5 V and V_{CC} and V_{CCQ} is V_{CC} + 0.5 V which, during transitions, may overshoot to V_{CC} +2.0 V for periods <20 ns.
2. Maximum DC voltage on V_{PP} may overshoot to +14.0 V for periods <20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.
4. V_{PP} Program voltage is normally 3.0 V–3.6 V. Connection to supply of 11.4 V–12.6 V can only be done for 1000 cycles on the main blocks and 2500 cycles on the parameter blocks during program/erase. V_{PP} may be connected to 12 V for a total of 80 hours maximum.

NOTICE: This datasheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

Warning: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

8.2 Automotive Temperature Operating Conditions

Symbol	Parameter	Notes	Min	Max	Unit
T_A	Operating Temperature		–40	+125	°C
V_{CC1}	V_{CC} Supply Voltage	1	3.0	3.6	V
V_{CCQ1}	I/O Voltage	1,2	3.0	3.6	V
V_{PP1}	V_{PP} Supply Voltage	1	3.0	3.6	V
V_{PP2}	V_{PP} Supply Voltage	1,3	11.4	12.6	V
Cycling	Parameter Block Erase Cycling		50,000		Cycles
	Main Block Erase Cycling		1,000		Cycles

NOTES:
1. See DC Characteristics tables for voltage range-specific specifications.
2. The voltage swing on the inputs, V_{IN} is required to match V_{CCQ}.
3. Applying V_{PP} = 11.4 V–12.6 V during a program/erase can only be done for a maximum of 1000 cycles on the main and 2500 cycles on the parameter blocks. A hard connection to V_{PP} = 11.4 V–12.6 V is not allowed and can cause damage to the device.

8.3 Capacitance(1)

T_A = +25 °C, f = 1 MHz

Symbol	Parameter	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	6	8	pF	V_{IN} = 0.0 V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0.0 V

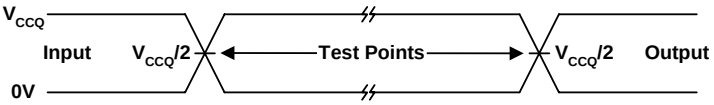
NOTE: 1. Sampled, not 100% tested.

8.4 DC Characteristics—Automotive Temperature(1)

Sym	Parameter	Note	Typ	Max	Unit	Test Condition	
I_{CCS}	V_{CC} Standby Current	2,6	40	100	µA	$V_{CC} = V_{CC}$Max $V_{CCQ} = V_{CCQ}$Max CE# = RST# = V_{IH}= V_{CC}	
I_{CCR}	V_{CC} Read Current	4,6	30	60	mA	Asynchronous t_{AVQV} = Min	$V_{CC} = V_{CC}$Max $V_{CCQ} = V_{CCQ}$Max $V_{IN} = V_{IH}$ or V_{IL} CE# = V_{IL} OE# = V_{IH}
			30	60	mA	Synchronous CLK = 33 MHz	CE# = V_{IL} OE# = V_{IH} Burst length = 8
I_{CCW}	V_{CC} Program Current	3,5,7	8	20	mA	$V_{PP} = V_{PP1}$ (3.0 V–3.6 V) Program in progress	
			8	20	mA	$V_{PP} = V_{PP2}$ (11.4 V–12.6 V) Program in progress	
I_{CCE}	V_{CC} Block Erase Current	3,5,7	8	20	mA	$V_{PP} = V_{PP1}$ (3.0 V–3.6 V) Block erase in progress	
			8	20	mA	$V_{PP} = V_{PP2}$ (11.4 V–12.6 V) Block erase in progress	
I_{PPW}	V_{PP} Program Current	3,5,7	15	40	mA	$V_{PP} = V_{PP1}$ (3.0 V–3.6 V) Program in progress	
			10	25	mA	$V_{PP} = V_{PP2}$ (11.4 V–12.6 V) Program in progress	
I_{PPE}	V_{PP} Block Erase Current	3,5,7	13	25	mA	$V_{PP} = V_{PP1}$ (3.0 V–3.6 V) Block erase in progress	
			8	25	mA	$V_{PP} = V_{PP2}$ (11.4 V–12.6 V) Block erase in progress	

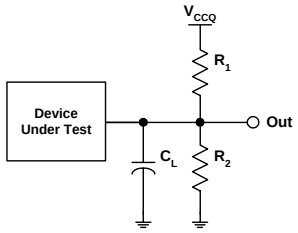
NOTES:
1. All currents are in RMS unless otherwise noted. Typical values at normal V_{CC}, T_A = +25 °C.
2. Erases and program operations are inhibited when $V_{PP} \le V_{PPLK}$, and not guaranteed outside the valid V_{PP} ranges of V_{PP1} and V_{PP2}.
3. Sampled, not 100% tested.
4. Automatic Power Savings (APS) reduces I_{CCR} to approximately standby levels, in static operation.
5. 12 V (11.4 V–12.6 V) can only be applied to V_{PP} for a maximum of 80 hours over the lifetime of the device. V_{PP} should not be permanently tied to 12 V.
6. The specification is the sum of V_{CC} and V_{CCQ} currents.

Figure 11. AC Input/Output Reference Waveform for V_{CC} = 3.3 V ± 0.3 V



NOTE: AC test inputs are driven at 3.0 V for a Logic "1" and 0.0 V for a Logic "0." Input timing begins, and output timing ends, at $V_{CCQ}/2$. Input rise and fall times (10% to 90%) < 5 ns. Worst case speed conditions are when V_{CCQ} = 3.0 V.

Figure 12. AC Equivalent Testing Load Circuit



NOTE: See table for component values.

Test Configuration Component Value for Worst Case Speed Conditions

Test Configuration	C_L (pF)	R_1 (Ω)	R_2 (Ω)
3 V Automotive Test	80	25K	25K
3 V Standard Test	50	25K	25K

NOTE: C_L includes jig capacitance.

8.5 AC Characteristics—Read-Only Operations[1,2]— Automotive Temperature

#	Symbol	Parameter	Product	–80		–95		Unit
			V_{CC}	3.0 V— 3.6 V		3.0 V— 3.6 V		
			Notes	Min	Max	Min	Max	
R1	t_{CLK}	CLK Period		15		15		ns
R2	$t_{CH}(t_{CL})$	CLK High (Low) Time		2.5		2.5		ns
R3	t_{CHCL}	CLK Fall (Rise) Time			5		5	ns
R4	t_{AVCH}	Address Valid Setup to CLK		10		10		ns
R5	t_{VLCH}	ADV# Low Setup to CLK		10		10		ns
R6	t_{ELCH}	CE# Low Setup to CLK		10		10		ns
R7	t_{CHQV}	CLK to Output Delay			17		19	ns
R8	t_{CHQX}	Output Hold from CLK	3	3		3		ns
R9	t_{CHAX}	Address Hold from CLK	4	10		10		ns
R10	t_{CHTL}	CLK to WAIT# delay	3		19		19	ns
R11	t_{AVVH}	Address Setup to ADV# High		10		10		ns
R12	t_{ELVH}	CE# Low to ADV# High		10		10		ns
R13	t_{AVQV}	Address to Output Delay			80		95	ns
R14	t_{ELQV}	CE# Low to Output Delay	5		80		95	ns
R15	t_{VLQV}	ADV# Low to Output Delay			80		95	ns
R16	t_{VLVH}	ADV# Pulse Width Low		10		10		ns
R17	t_{VHVL}	ADV# Pulse Width High		10		10		ns
R18	t_{VHAX}	Address Hold from ADV# High	4	3		3		ns
R19	t_{APA}	Page Address Access Time			25		25	ns
R20	t_{GLQV}	OE# Low to Output Delay			40		40	ns
R21	t_{PHQV}	RST# High to Output Delay			600		600	ns
R22	t_{EHQZ} t_{GHQZ}	CE# or OE# High to Output in High Z, Whichever Occurs First	3		23		25	ns
R23	t_{OH}	Output Hold from Address, CE#, or OE# Change, Whichever Occurs First	3	0		0		ns
R24	t_{EHEL}	CE# High Pulse Width	6	0		0		ns

NOTES:
1. See Figure 11, “AC Input/Output Reference Waveform for VCC = 3.3 V ± 0.3 V” on page 31 for timing measurements and maximum allowable input slew rate.
2. Data bus voltage must be less than or equal to V_{CCQ} when a read operation is initiated to guarantee AC specifications.
3. Sampled, not 100% tested.
4. Address hold in synchronous burst mode is defined as t_{CHAX} or t_{VHAX}, whichever timing specification is satisfied first.
5. OE# may be delayed up to t_{ELQV}–t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
6. ADV# tied to ground, t_{EHEL} (CE# High Pulse Width) must be held high for a minimum of 15 ns.

Figure 13. AC Waveform for CLK Input

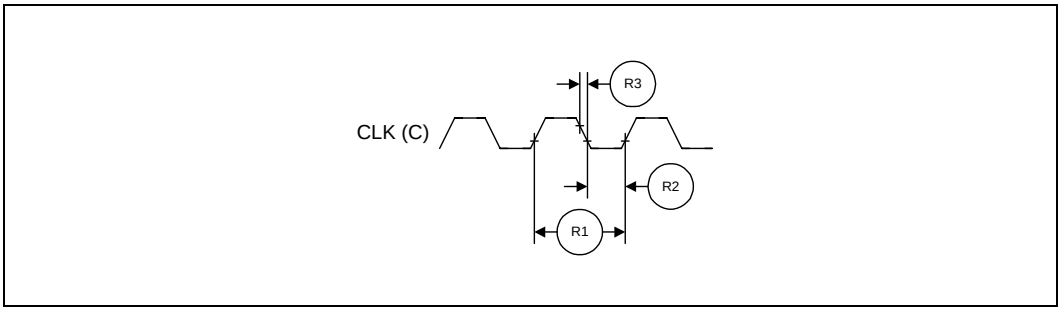


Figure 14. AC Waveform for Single Asynchronous Read Operations from Parameter Blocks, Status Register, Identifier Codes

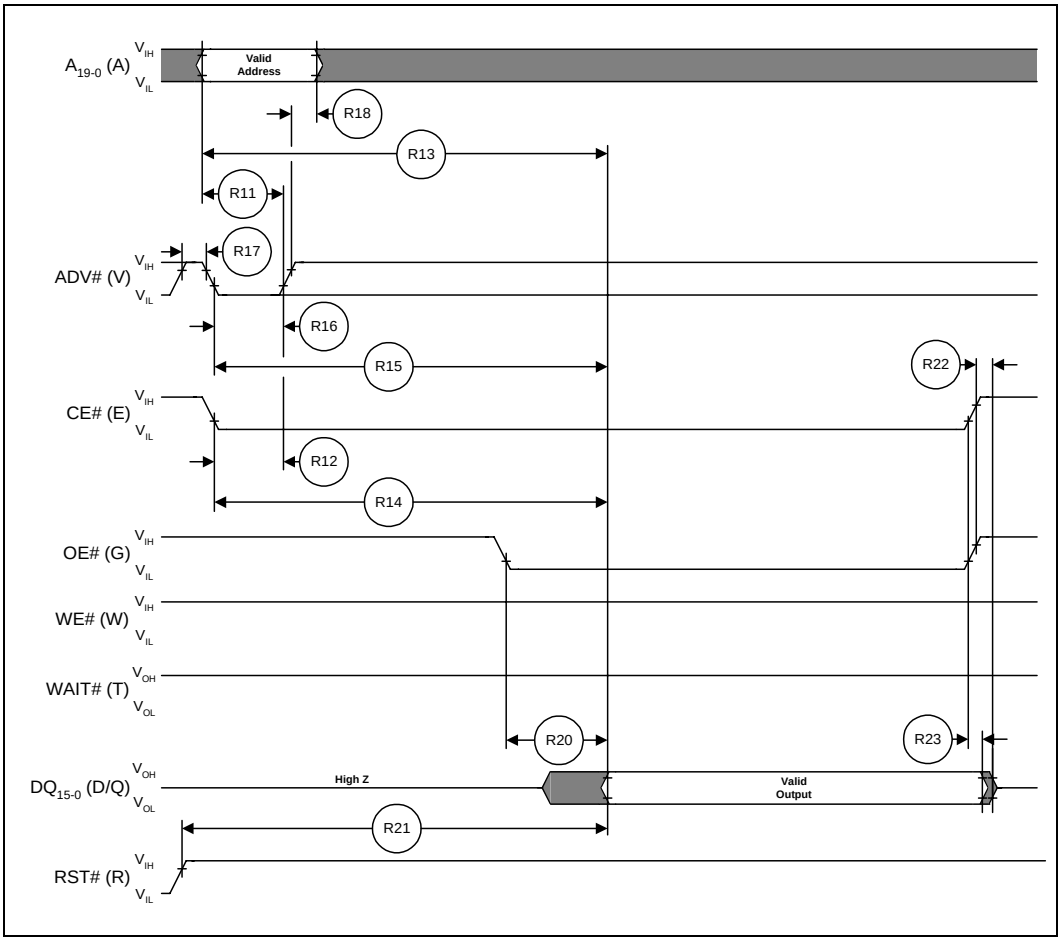


Figure 15. AC Waveform for Asynchronous Page Mode Read Operations from Main Blocks

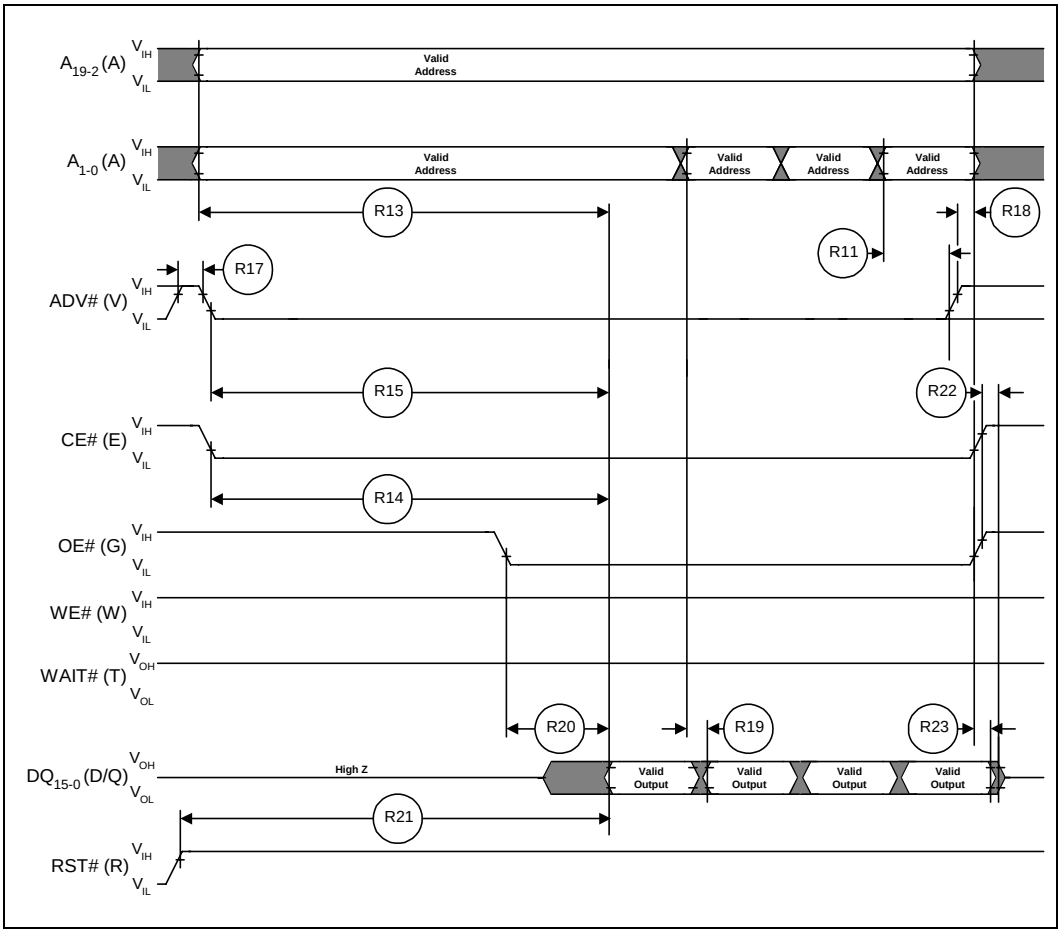
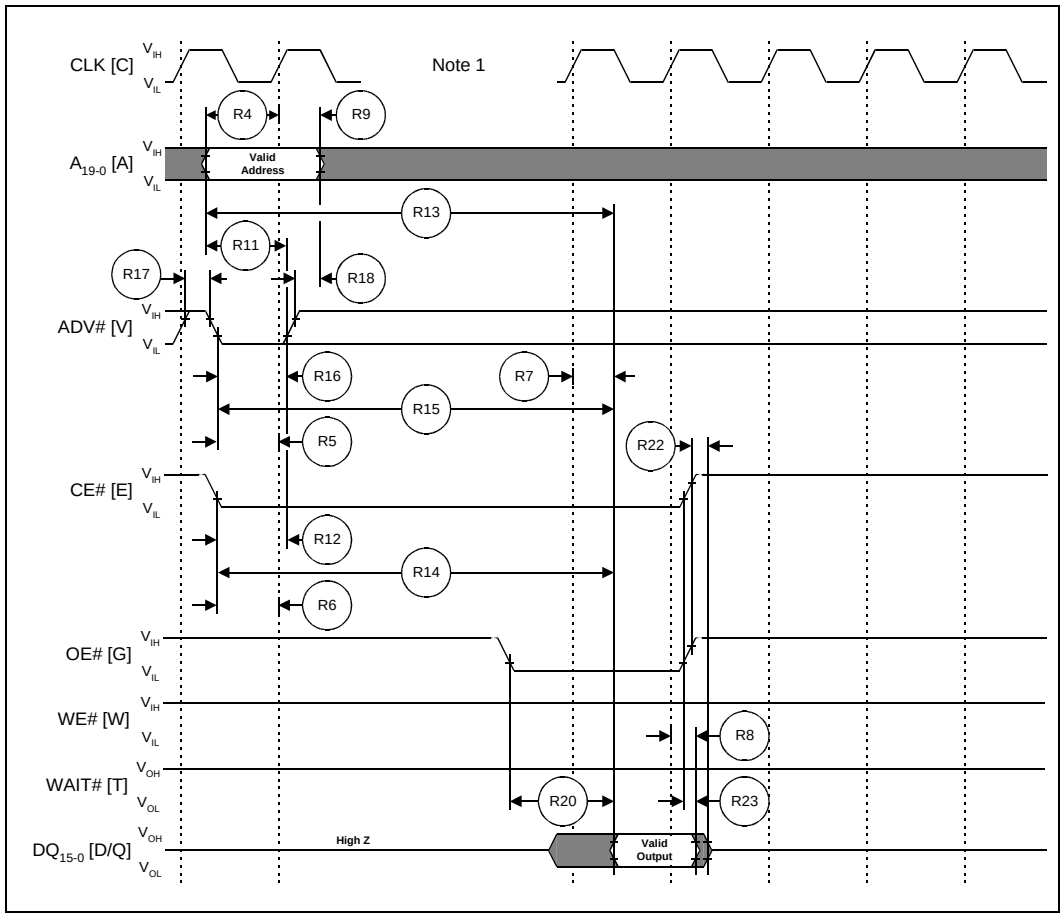


Figure 16. AC Waveform for Single Synchronous Read Operations from Parameter Blocks, Status Register, Identifier Codes

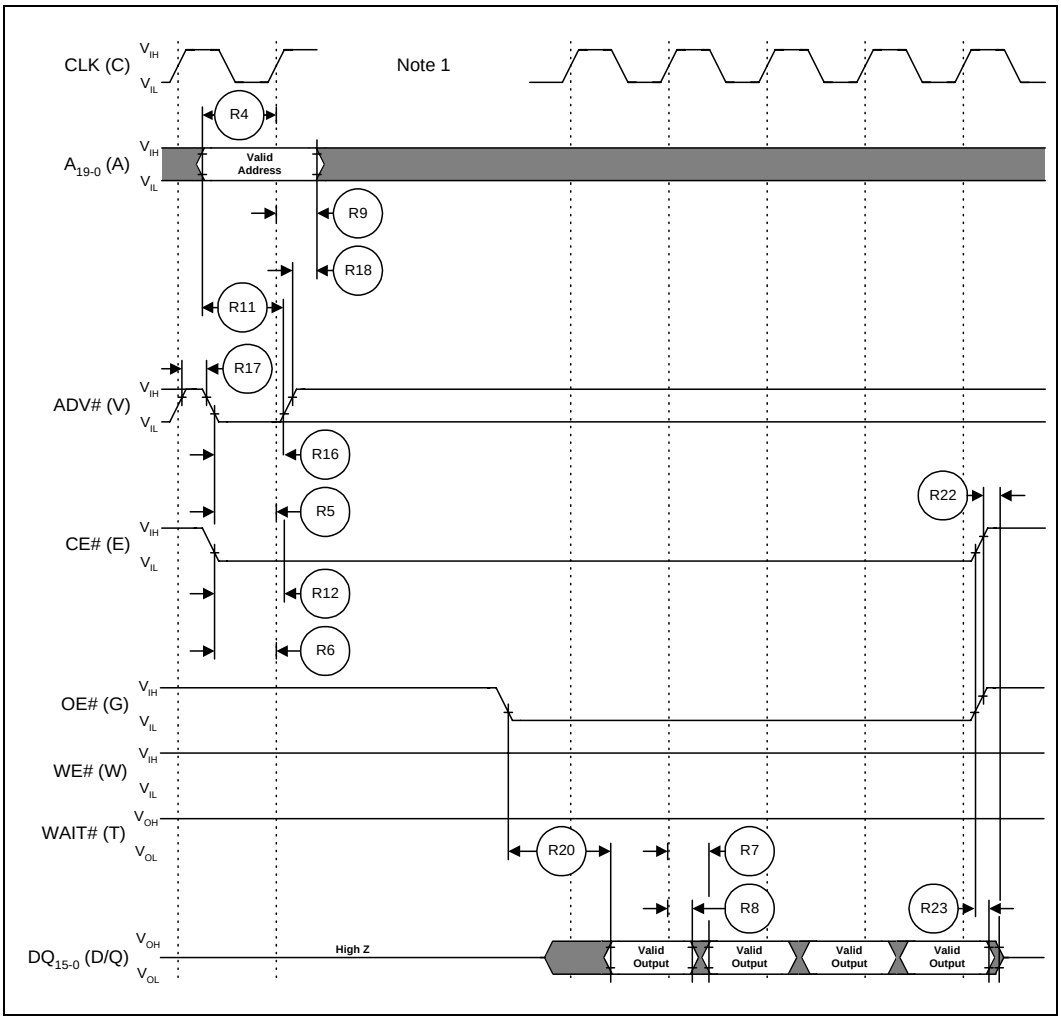


NOTES:

1. 1.Depending upon the frequency configuration code value in the read configuration register, insert clock cycles:
   - Frequency Configuration 2 insert two clock cycles
   - Frequency Configuration 3 insert three clock cycles
   - Frequency Configuration 4 insert four clock cycles
   - Frequency Configuration 5 insert five clock cycles
   - Frequency Configuration 6 insert six clock cycles

See Section 4.9.2 for further information about the frequency configuration and its effect on the initial read.

Figure 17. AC Waveform for Synchronous Burst Read Operations, Four-Word Burst Length, from Main Blocks

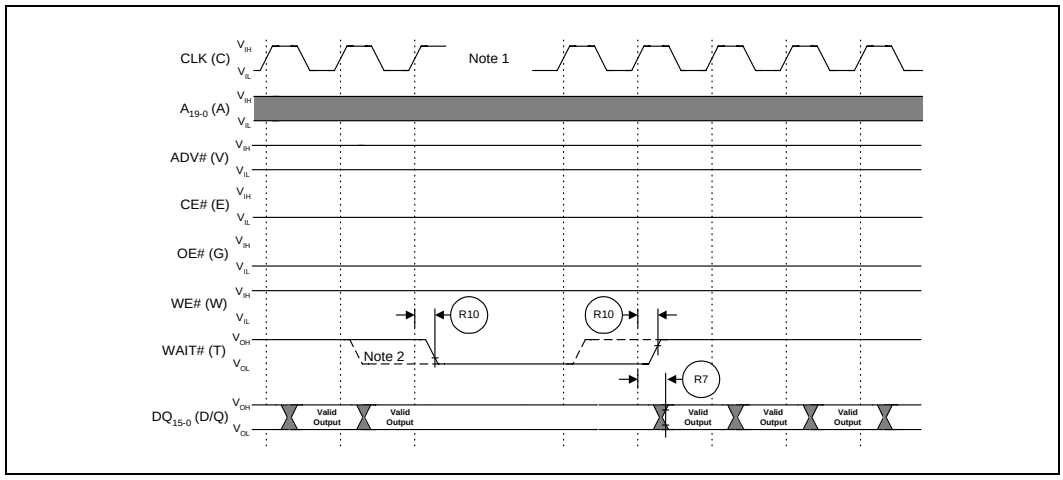


NOTES:

1. 1.Depending upon the frequency configuration code value in the read configuration register, insert clock cycles:
   - Frequency Configuration 2 insert two clock cycles
   - Frequency Configuration 3 insert three clock cycles
   - Frequency Configuration 4 insert four clock cycles
   - Frequency Configuration 5 insert five clock cycles
   - Frequency Configuration 6 insert six clock cycles

See Section 4.9.2 for further information about the frequency configuration and its effect on the initial read.

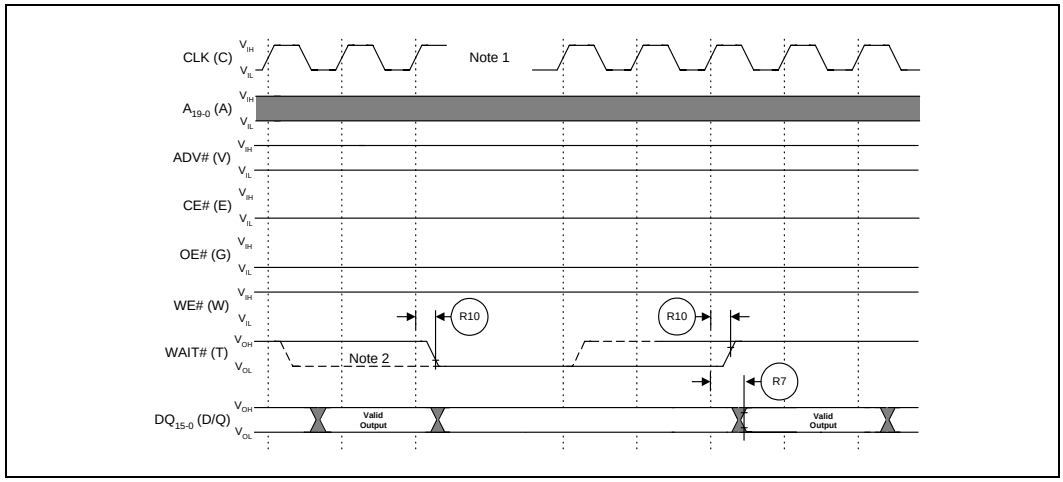
Figure 18. AC Waveform for Continuous Burst Read, Showing an Output Delay with Data Output Configuration Set to One Clock



NOTES:
1. This delay will only occur when burst length is configured as continuous. See Section 4.9.7 for further information about burst length configuration.
2. WAIT# is configurable. It can be set to assert during or one CLK cycle before an output delay.

See Section for further information about the frequency configuration and its effect on the initial read.

Figure 19. AC Waveform for Continuous Burst Read, Showing an Output Delay with Data Output Configuration Set to Two Clocks



NOTES:
1. This delay will only occur when burst length is configured as continuous. See Section 4.9.7 for further information about burst length configuration.
2. WAIT# is configurable. It can be set to assert during or two CLK cycles before an output delay.

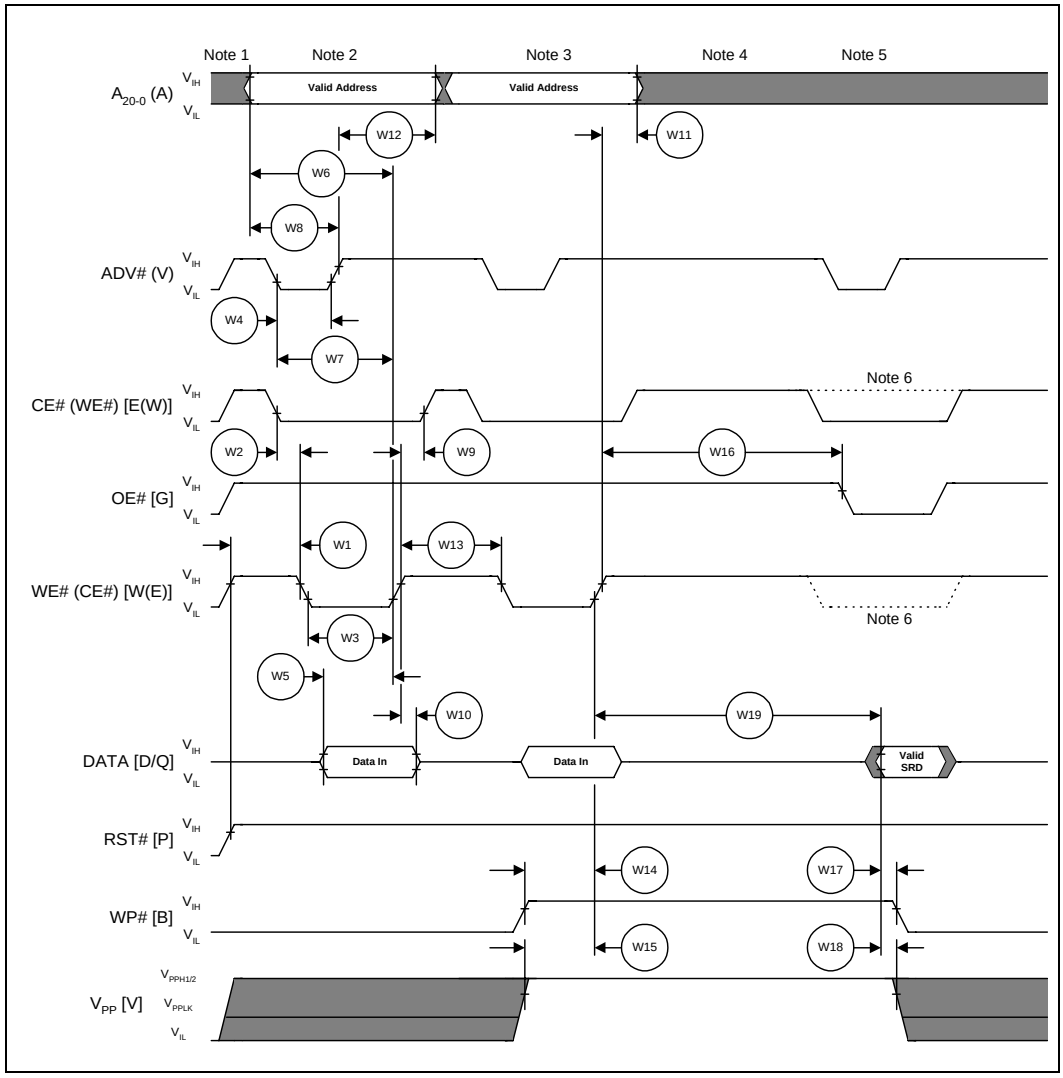
See Section for further information about the frequency configuration and its effect on the initial read.

8.6 AC Characteristics—Write Operations[1, 2]—Automotive Temperature

#	Sym	Parameter	Valid for All Speed and Voltage Combinations			Unit
			Notes	Min	Max	
W1	t_{PHWL} (t_{PHEL})	RST# High Recovery to WE# (CE#) Going Low	3	600		ns
W2	t_{ELWL} (t_{WLEL})	CE# (WE#) Setup to WE# (CE#) Going Low	4	0		ns
W3	t_{WP} (t_{WLWH})	Write Pulse Width	4	75		ns
W4	t_{VLVH}	ADV# Pulse Width		10		ns
W5	t_{DVWH} (t_{DVEH})	Data Setup to WE# (CE#) Going High	5	63		ns
W6	t_{AVWH} (t_{AVEH})	Address Setup to WE# (CE#) Going High	5	75		ns
W7	t_{VLEH} (t_{VLWH})	ADV# Setup to WE# (CE#) Going High		75		ns
W8	t_{AVVH}	Address Setup to ADV# Going High		10		ns
W9	t_{WHEH} (t_{EHWH})	CE# (WE#) Hold from WE# (CE#) High		0		ns
W10	t_{WHDX} (t_{EHDX})	Data Hold from WE# (CE#) High		0		ns
W11	t_{WHAX} (t_{EHAX})	Address Hold from WE# (CE#) High		0		ns
W12	t_{VHAX}	Address Hold from ADV# Going High		3		ns
W13	t_{WPH} (t_{WHWL})	Write Pulse Width High	6	20		ns
W14	t_{BHWH} (t_{BHEH})	WP# Setup to WE# (CE#) Going High	3	200		ns
W15	t_{VPWH} (t_{VPEH})	V_{PP} Setup to WE# (CE#) Going High	3	200		ns
W16	t_{WHGL} (t_{EHGL})	Write Recovery before Read	7	15		ns
W17	t_{QVBL}	WP# Hold from Valid SRD	3,8	0		ns
W18	t_{QVVL}	V_{PP} Hold from Valid SRD	3,8	0		ns

NOTES:
1. See Figure 11, “AC Input/Output Reference Waveform for VCC = 3.3 V ± 0.3 V” on page 31 for timing measurements and maximum allowable input slew rate.
2. A write operation can be initiated and terminated with either CE# or WE#.
3. Sampled, not 100% tested.
4. Write pulse width (t_{WP}) is defined from CE# or WE# going low (whichever goes low last) to CE# or WE# going high (whichever goes high first). Hence, $t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$.
5. Refer to Table 3 for valid A_{IN} and D_{IN} for block erase or program.
6. Write pulse width high (t_{WPH}) is defined from CE# or WE# going high (whichever goes high first) to CE# or WE# going low (whichever goes low last). Hence, $t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$.
7. t_{WHGL} is 15 ns unless resuming a program suspend or erase suspend command; then 30 ns is required before read can be commenced.
8. V_{PP} should be held at $V_{PPH1/2}$ until determination of block erase or program success.

Figure 20. AC Waveform for Write Operations



NOTES:

1. V_{CC} power-up and standby.
2. Write block erase or program setup.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. For read operations, OE# and CE# must be driven active, and WE# de-asserted.

8.7 AC Characteristics—Reset Operation—Automotive Temperature

Figure 21. AC Waveform for Reset Operation

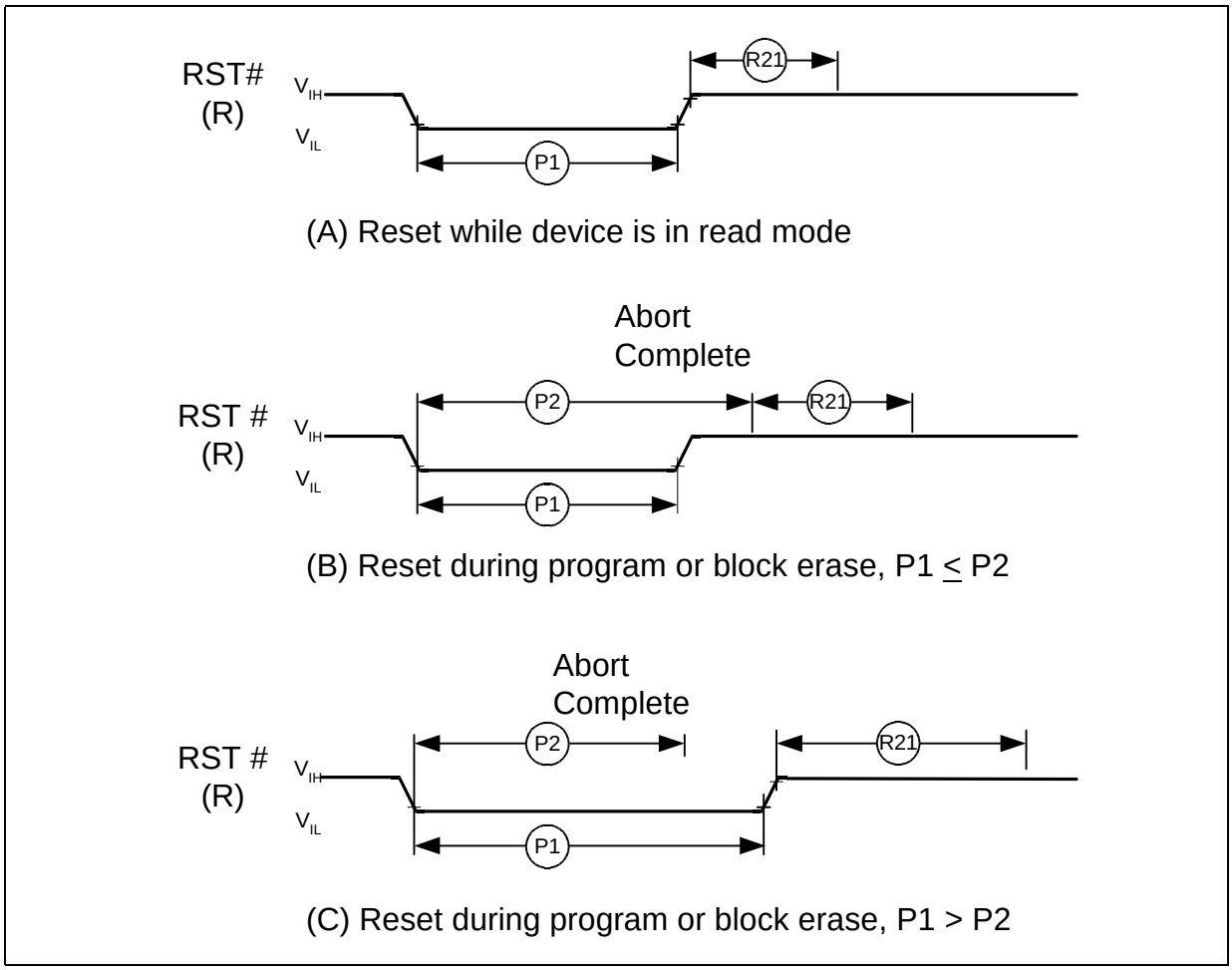


Table 10. Reset Specifications(1)

Number	Symbol	Parameter	Notes	Min	Max	Unit
P1	t_{PLPH}	RST# Low to Reset during Read (If RST# is tied to V_{CC}, this specification is not applicable)	2,3	100		ns
P2	t_{PLRH}	RST# Low to Reset during Block Erase or Program	3,4		22	µs

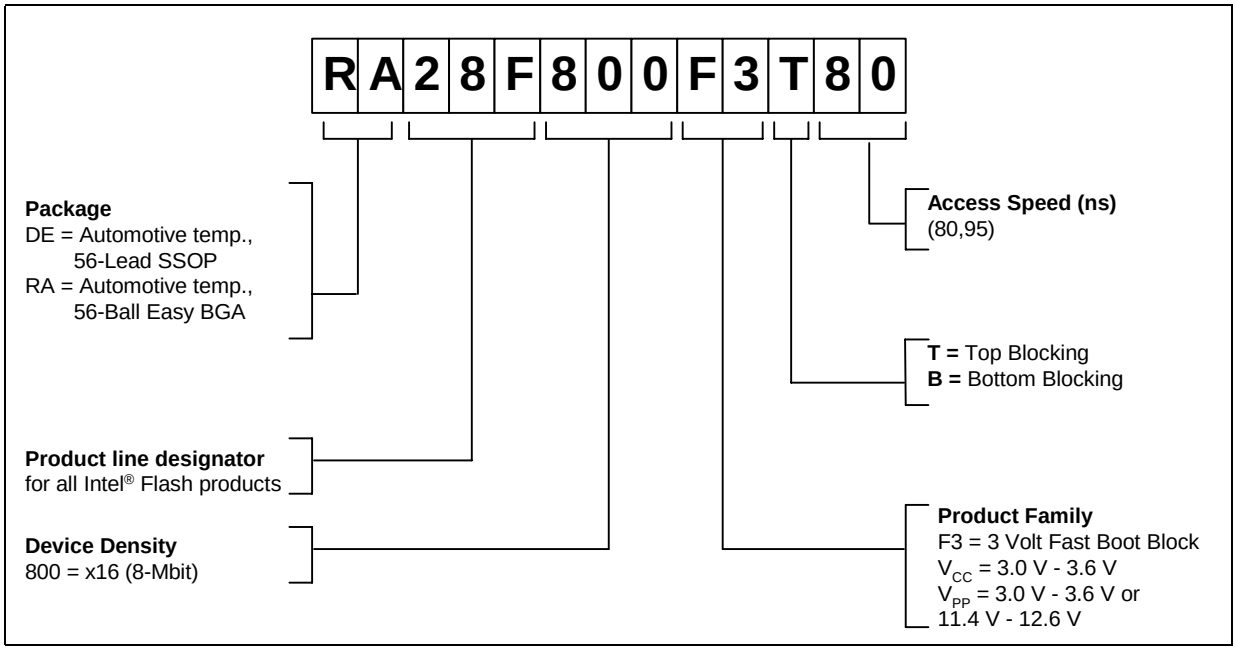
NOTES:
1. These specifications are valid for all product versions (packages and speeds).
2. If t_{PLPH} is < 100 ns the device may still reset but this is not guaranteed.
3. Sampled, but not 100% tested.
4. If RST# is asserted while a block erase or word program operation is not executing, the reset will complete within 100 ns.

8.8 Automotive Temperature Block Erase and Program Performance[1,2,3]

#	Sym	Parameter	Notes	3.3 V V_{PP}		12 V V_{PP}		Unit
				Typ[4]	Max	Typ[4]	Max	
W19	t_{WHRH}, t_{EHRH1}	Program Time	5	23.5	200	8	185	µs
		Block Program Time (Parameter)	5	0.1	0.3	0.03	0.1	sec
		Block Program Time (Main)	5	0.8	2.4	0.24	0.8	sec
	t_{WHRH}, t_{EHRH2}	Block Erase Time (Parameter)	5	0.5	1.0	0.5	1.0	sec
		Block Erase Time (Main)	5	1.5	3.0	1.5	3.0	sec
	t_{WHRH}, t_{EHRH5}	Program Suspend Latency		6	10	5	10	µs
	t_{WHRH}, t_{EHRH6}	Erase Suspend Time		13	20	10	12	µs

NOTES:
1. These performance numbers are valid for all speed versions.
2. Sampled, but not 100% tested.
3. Reference the Figure 20, “AC Waveform for Write Operations” on page 39
4. Typical values measured at T_A = +25°C and nominal voltages. Subject to change based on device characterization.
5. Excludes system-level overhead.

9.0 Ordering Information



Valid Combinations

	56-Lead SSOP	8 x 8 Easy BGA
Automotive 8 M	DE28F800F3T80	RA28F800F3T80
	DE28F800F3B80	RA28F800F3B80
	DE28F800F3T95	RA28F800F3T95
	DE28F800F3B95	RA28F800F3B95