Intel® Advanced Boot Block Flash Memory (B3)

28F008/800B3, 28F016/160B3, 28F320B3, 28F640B3

Datasheet

Product Features

- Flexible SmartVoltage Technology
  - —2.7 V – 3.6 V read/program/erase
  - —12 V V_{PP} fast production programming
- 1.65 V – .5 V or 2.7 V – 3.6 V I/O option
  - —Reduces overall system power
- High Performance
  - —2.7 V – 3.6 V: 70 ns max access time
- Optimized Block Sizes
  - —Eight 8-KB blocks for data, top or bottom locations
  - —Up to 127 x 64-KB blocks for code
- Block Locking
  - —V_{CC}-level control through Write Protect WP#
- Low Power Consumption
  - —9 mA typical read current
- Absolute Hardware-Protection
  - —V_{PP} = GND option
  - —V_{CC} lockout voltage
- Extended Temperature Operation
  - —–40 °C to +85 °C
- Automated Program and Block Erase
  - —Status registers
- Intel® Flash Data Integrator Software
  - —Flash Memory Manager
  - —System Interrupt Manager
  - —Supports parameter storage, streaming data (for example, voice)
- Extended Cycling Capability
  - —Minimum 100,000 block erase cycles guaranteed
- Automatic Power Savings Feature
  - —Typical I_{CCS} after bus inactivity
- Standard Surface Mount Packaging
  - —48-Ball CSP packages
  - —40- and 48-Lead TSOP packages
- Density and Footprint Upgradeable for common package
  - —8-, 16-, 32-, and 64-Mbit densities
- ETOX™ VIII (0.13 µm) Flash Technology
  - —16 and 32-Mbit densities
- ETOX™ VII (0.18 µm) Flash Technology
  - —16-, 32-, and 64-Mbit densities
- ETOX ™ VI (0.25µm) Flash Technology
  - —8-, 16-, and 32-Mbit densities
- The x8 option is not recommended for new designs

The Intel® Advanced Boot Block Flash Memory (B3) device, manufactured on the Intel 0.13 µm and 0.18 µm technologies, represents a feature-rich solution at overall lower system cost. The B3 device in x16 will be available in 48-lead TSOP and 48-ball CSP packages. The x8 option of this product family is available only in 40-lead TSOP and 48-ball µBGA* packages. Additional information about this product family can be obtained by accessing Intel's website at: http://www.intel.com/design/flash.

Notice: This specification is subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

290580-019
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Contents

Revision History

Number	Description
-001	Original version
-002	Section 3.4, V_{PP} *Program and Erase Voltages*, added Updated Figure 9: *Automated Block Erase Flowchart* Updated Figure 10: *Erase Suspend/Resume Flowchart* (added program to table) Updated Figure 16: *AC Waveform: Program and Erase Operations* (updated notes) I_{PPR} maximum specification change from ±25 µA to ±50 µA Program and Erase Suspend Latency specification change Updated Appendix A: *Ordering Information* (included 8 M and 4 M information) Updated Figure, Appendix D: *Architecture Block Diagram* (Block info. in words not bytes) Minor wording changes
-003	Combined byte-wide specification (previously 290605) with this document Improved speed specification to 80 ns (3.0 V) and 90 ns (2.7 V) Improved 1.8 V I/O option to minimum 1.65 V (Section 3.4) Improved several DC characteristics (Section 4.4) Improved several AC characteristics (Sections 4.5 and 4.6) Combined 2.7 V and 1.8 V DC characteristics (Section 4.4) Added 5 V V_{PP} read specification (Section 3.4) Removed 120 ns and 150 ns speed offerings Moved *Ordering Information* from Appendix to Section 6.0; updated information Moved *Additional Information* from Appendix to Section 7.0 Updated figure Appendix B, *Access Time vs. Capacitive Load* Updated figure Appendix C, *Architecture Block Diagram* Moved Program and Erase Flowcharts to Appendix E Updated *Program Flowchart* Updated *Program Suspend/Resume Flowchart* Minor text edits throughout
-004	Added 32-Mbit density Added 98H as a reserved command (Table 4) A_1–A_{20} = 0 when in read identifier mode (Section 3.2.2) Status register clarification for SR3 (Table 7) V_{CC} and V_{CCQ} absolute maximum specification = 3.7 V (Section 4.1) Combined I_{PPW} and I_{CCW} into one specification (Section 4.4) Combined I_{PPE} and I_{CCE} into one specification (Section 4.4) Max Parameter Block Erase Time (t_{WHQV2}/t_{EHQV2}) reduced to 4 sec (Section 4.7) Max Main Block Erase Time (t_{WHQV3}/t_{EHQV3}) reduced to 5 sec (Section 4.7) Erase suspend time @ 12 V (t_{WHRH2}/t_{EHRH2}) changed to 5 µs typical and 20 µs maximum (Section 4.7) *Ordering Information* updated (Section 6.0) Write State Machine Current/Next States Table updated (Appendix A) Program Suspend/Resume Flowchart updated (Appendix F) Erase Suspend/Resume Flowchart updated (Appendix F) Text clarifications throughout
-005	µBGA package diagrams corrected (Figures 3 and 4) I_{PPD} test conditions corrected (Section 4.4) 32-Mbit ordering information corrected (Section 6) µBGA package top side mark information added (Section 6)
-006	V_{IH} and V_{IL}Specification change (Section 4.4) I_{CCS} test conditions clarification (Section 4.4) Added Command Sequence Error Note (Table 7) Data sheet renamed from *Smart 3 Advanced Boot Block 4-Mbit, 8-Mbit, 16-Mbit Flash Memory Family.* Added device ID information for 4-Mbit x8 device Removed 32-Mbit x8 to reflect product offerings Minor text changes
-007	Corrected RP# pin description in Table 2, *3 Volt Advanced Boot Block Pin Descriptions* Corrected typographical error fixed in *Ordering Information*

Number	Description
-008	4-Mbit packaging and addressing information corrected throughout document
-009	Corrected 4-Mbit memory addressing tables in Appendices D and E
-010	Max I_{CCD} changed to 25 µA V_{CC}Max on 32 M (28F320B3) changed to 3.3 V
-011	Added 64-Mbit density and faster speed offerings Removed access time vs. capacitance load curve
-012	Changed references of 32Mbit 80ns devices to 70ns devices to reflect the faster product offering. Changed VccMax=3.3V reference to indicate the affected product is the 0.25µm 32Mbit device. Minor text edits throughout document.
-013	Added New Pin-1 indicator information on 40 and 48Lead TSOP packages. Minor text edits throughout document.
-014	Added specifications for 0.13 micron product offerings throughout document
-015	Minor text edits throughout document.
-016	Adjusted ordering information. Adjusted specifications for 0.13 micron product offerings. Revised and corrected DC Characteristics Table. Adjusted package diagram information. Minor text edits throughout document.
-017	Updated ordering information. Adjusted specifications for 0.13 micron product offerings. Updated AC/DC Characteristics Table. Added TSOP and µBGA* package diagram information. Minor text edits throughout document.
-018	Updated the layout of the datasheet.
-019	Added line items to Table 31 “Ordering Information: Valid Combinations” on page 69.

1.0 Introduction

This datasheet describes the specifications for the Intel® Advanced Boot Block Flash Memory (B3) device (hereafter referred to as the B3 flash memory device). It is optimized for portable, low-power, systems. This family of products features 1.65 V to 2.5 V or 2.7 V to 3.6 V I/Os, and a low V_{CC}/V_{PP} operating range of 2.7 V to 3.6 V for Read, Program, and Erase operations. In addition, it is capable of fast programming at 12 V. Throughout this document, the term "2.7 V" refers to the full voltage range 2.7 V to 3.6 V (except where noted otherwise) and "V_{PP} = 12 V" refers to 12 V ±5%.

1.1 Nomenclature

0x	Hexadecimal prefix
0b	Binary prefix
Byte	8 bits
Word	16 bits
KW or Kword	1024 words
Mword	1,048,576 words
Kb	1024 bits
KB	1024 bytes
Mb	1,048,576 bits
MB	1,048,576 bytes
APS	Automatic Power Savings
CSP	Chip Scale Package
CUI	Command User Interface
OTP	One Time Programmable
PR	Protection Register
PRD	Protection Register Data
PLR	Protection Lock Register
RFU	Reserved for Future Use
SR	Status Register
SRD	Status Register Data
WSM	Write State Machine

1.2 Conventions

The terms **pin** and **signal** are often used interchangeably to refer to the external signal connections on the package; for chip scale package (CSP) the term *ball* is used.

Group Membership Brackets: Square brackets will be used to designate group membership or to define a group of signals with similar function (i.e. A[21:1], SR[4:1])

Set: When referring to registers, the term set means the bit is a logical 1.

Clear: When referring to registers, the term clear means the bit is a logical 0.

Block: A group of bits (or words) that erase simultaneously with one block erase instruction.

Main Block: A block that contains 32 Kwords.

Parameter Block: A block that contains 4 Kwords.

2.0 Functional Overview

The B3 flash memory device features the following:

- Enhanced blocking for easy segmentation of code and data or additional design flexibility
- Program Suspend to Read command
- V_{CCQ} input of 1.65 V to 2.5 V or 2.7 V to 3.6 V on all I/Os. See Figures 1 through 4 for pinout diagrams and V_{CCQ} location
- Maximum program and erase time specification for improved data storage.

Table 1. B3 Device Feature Summary

Feature	28F008B3, 28F016B3	28F800B3, 28F160B3, 28F320B3[3], 28F640B3	Reference
V_{CC} Read Voltage	2.7 V– 3.6 V		Section 6.2, Section 7.2
V_{CCQ} I/O Voltage	1.65 V–2.5 V or 2.7 V– 3.6 V		Section 4.2, 4.4
V_{PP} Program/Erase Voltage	2.7 V– 3.6 V or 11.4 V– 12.6 V		Section 4.2, 4.4
Bus Width	8 bit	16 bit	Table 25
Speed	70 ns, 80 ns, 90 ns, 100 ns, 110 ns		Section 8.1
Memory Arrangement	1024 Kbit x 8 (8 Mbit), 2048 Kbit x 8 (16 Mbit)	512 Kbit x 16 (8 Mbit), 1024 Kbit x 16 (16 Mbit), 2048 Kbit x 16 (32 Mbit), 4096 Kbit x 16 (64 Mbit)	Section 3.2
Blocking (top or bottom)	Eight 8-Kbyte parameter blocks **and** Fifteen 64-Kbyte blocks (8 Mbit) or Thirty-one 64-Kbyte main blocks (16 Mbit) Sixty-three 64-Kbyte main blocks (32 Mbit) One hundred twenty-seven 64-Kbyte main blocks (64 Mbit)		Section 3.2 "Memory Maps and Block Organization" on page 10
Locking	WP# locks/unlocks parameter blocks All other blocks protected using V_{PP}		Section 12.0 Table 30
Operating Temperature	Extended: –40 °C to +85 °C		Section 6.2, Section 7.2
Program/Erase Cycling	100,000 cycles		Section 6.2, Section 7.2
Packages	40-lead TSOP[1], 48-Ball µBGA* CSP[2]	48-Lead TSOP, 48-Ball µBGA CSP[2], 48-Ball VF BGA	Figure 8, Figure 9

NOTES:
1. 32-Mbit and 64-Mbit densities not available in 40-lead TSOP.
2. 8-Mbit densities not available in µBGA* CSP.
3. V_{CC}Max is 3.3 V on 0.25µm 32-Mbit devices.

3.0 Functional Overview

Intel provides the most flexible voltage solution in the flash industry, providing three discrete voltage supply pins: V_{CC} for Read operation, V_{CCQ} for output swing, and V_{PP} for Program and Erase operation. All B3 flash memory devices provide program/erase capability at 2.7 V or 12 V (for fast production programming), and read with V_{CC} at 2.7 V. Since many designs read from the flash memory a large percentage of the time, 2.7 V V_{CC} operation can provide substantial power savings.

The B3 flash memory device family is available in either x8 or x16 packages in the following densities (see Appendix C, "Ordering Information," for availability):

- 8-Mbit (8, 388, 608-bit) flash memory organized as 512 Kwords of 16 bits each or 1024 Kbytes of 8-bits each
- 16-Mbit (16, 777, 216-bit) flash memory organized as 1024 Kwords of 16 bits each or 2048 Kbytes of 8-bits each
- 32-Mbit (33, 554, 432-bit) flash memory organized as 2048 Kwords of 16 bits each
- 64-Mbit (67, 108, 864-bit) flash memory organized as 4096 Kwords of 16 bits each

The parameter blocks are located at either the top (denoted by -T suffix) or the bottom (-B suffix) of the address map in order to accommodate different microprocessor protocols for kernel code location. The upper two (or lower two) parameter blocks can be locked to provide complete code security for system initialization code. Locking and unlocking is controlled by Write Protect WP# (see Section 12.0, "Block Locking" on page 60 for details).

The Command User Interface (CUI) serves as the interface between the microprocessor or microcontroller and the internal operation of the flash memory. The internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for Program and Erase operations, including verification, thereby unburdening the microprocessor or microcontroller. The Status Register indicates the status of the WSM by signifying block erase or word program completion and status.

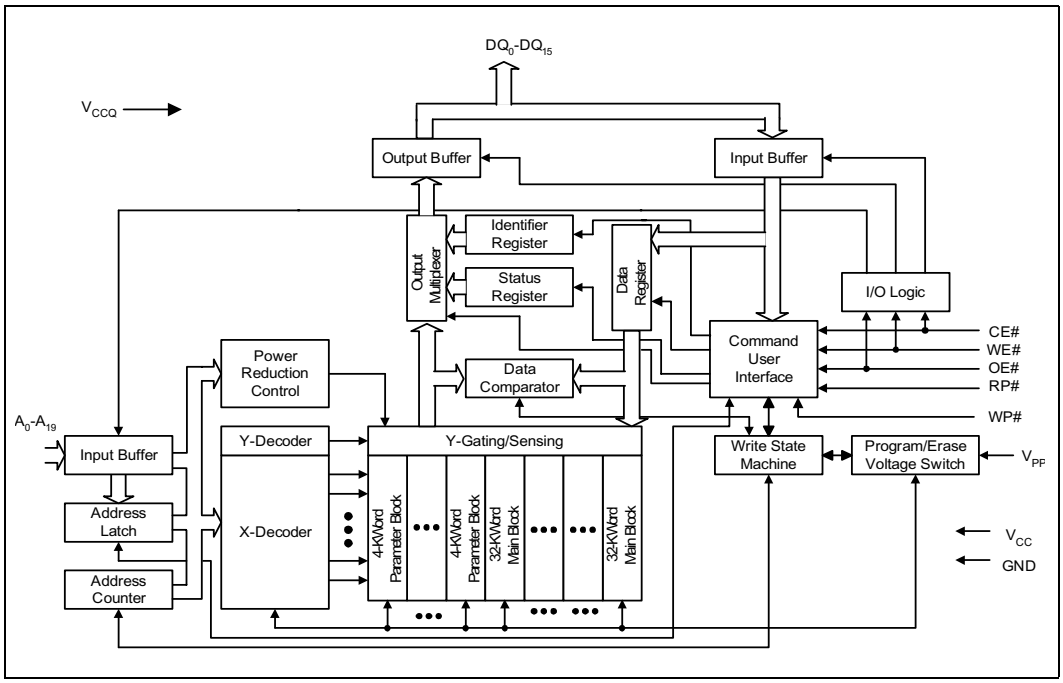
The B3 flash memory device is also designed with an Automatic Power Savings (APS) feature, which minimizes system current drain and allows for very low power designs. This mode is entered following the completion of a read cycle (approximately 300 ns later).

The RP# pin provides additional protection against unwanted command writes that may occur during system reset and power-up/down sequences due to invalid system bus conditions (see "Power and Reset Specifications" on page 49).

Section 10.0, "Operations Overview" on page 52 gives detailed explanation of the different modes of operation. Section 7.0, "Electrical Specifications" on page 35 and Section 8.0, "AC Characteristics" on page 38 provide complete current and voltage specifications. Refer to Section 8.1, "AC Read Characteristics" on page 38 for read, program, and erase performance specifications.

3.1 Architecture Diagram

Figure 1. B3 Architecture Block Diagram



3.2 Memory Maps and Block Organization

The B3 flash memory device is an asymmetrically blocked architecture that enables system integration of code and data within a single flash device. Each block can be erased independently of the others up to 100,000 times. For the address locations of each block, see the following memory maps:

- Table 2, “16- and 32-Mbit Word-Wide Memory Addressing Map” on page 11
- Table 3, “4- and 8-Mbit Word-Wide Memory Addressing Map” on page 14
- Table 4, “16-, 32-, and 64-Mbit Word-Wide Memory Addressing Map” on page 15
- Table 5, “8- and 16-Mbit Byte-Wide Memory Addressing Map” on page 20
- Table 6, “4-Mbit Byte Wide Memory Addressing Map” on page 23

3.2.1 Parameter Blocks

The B3 flash memory device architecture includes parameter blocks to facilitate storage of frequently updated small parameters (i.e., data that would normally be stored in an EEPROM). The word-rewrite functionality of EEPROMs can be emulated using software techniques. Each device contains eight parameter blocks of 8 Kbytes/4 Kwords (8192 bytes/4,096 words) each.

3.2.2 Main Blocks

After the parameter blocks, the remainder of the array is divided into equal-size main blocks (65,536 bytes/32,768 words) for data or code storage. The 8-Mbit device contains 15 main blocks; 16-Mbit flash has 31 main blocks; 32-Mbit has 63 main blocks; 64-Mbit has 127 main blocks.

3.2.3 4-, 8-, 16-, 32-, and 64-Mbit Word-Wide Memory Maps

Table 2. 16- and 32-Mbit Word-Wide Memory Addressing Map (Sheet 1 of 3)

16-Mbit and 32-Mbit Word-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KW)		16 Mbit	32 Mbit	Size (KW)	8 Mbit	16 Mbit	32 Mbit
4		FF000-FFFFF	1FF000-1FFFFF	32			1F8000-1FFFFF
4		FE000-FEFFF	1FE000-1FEFFF	32			1F0000-1F7FFF
4		FD000-FDFFF	1FD000-1FDFFF	32			1E8000-1EFFFF
4		FC000-FCFFF	1FC000-1FCFFF	32			1E0000-1E7FFF
4		FB000-FBFFF	1FB000-1FBFFF	32			1D8000-1DFFFF
4		FA000-FAFFF	1FA000-1FAFFF	32			1D0000-1D7FFF
4		F9000-F9FFF	1F9000-1F9FFF	32			1C8000-1CFFFF
4		F8000-F8FFF	1F8000-1F8FFF	32			1C0000-1C7FFF
32		F0000-F7FFF	1F0000-1F7FFF	32			1B8000-1BFFFF
32		E8000-EFFFF	1E8000-1EFFFF	32			1B0000-1B7FFF
32		E0000-E7FFF	1E0000-1E7FFF	32			1A8000-1AFFFF
32		D8000-DFFFF	1D8000-1DFFFF	32			1A0000-1A7FFF
32		D0000-D7FFF	1D0000-1D7FFF	32			198000-19FFFF
32		C8000-CFFFF	1C8000-1CFFFF	32			190000-197FFF
32		C0000-C7FFF	1C0000-1C7FFF	32			188000-18FFFF
32		B8000-BFFFF	1B8000-1BFFFF	32			180000-187FFF
32		B0000-B7FFF	1B0000-1B7FFF	32			178000-17FFFF
32		A8000-AFFFF	1A8000-1AFFFF	32			170000-177FFF
32		A0000-A7FFF	1A0000-1A7FFF	32			168000-16FFFF
32		98000-9FFFF	198000-19FFFF	32			160000-167FFF
32		90000-97FFF	190000-197FFF	32			158000-15FFFF
32		88000-8FFFF	188000-18FFFF	32			150000-157FFF
32		80000-87FFF	180000-187FFF	32			148000-14FFFF
32		78000-7FFFF	178000-17FFFF	32			140000-147FFF
32		70000-77FFF	170000-177FFF	32			138000-13FFFF
32		68000-6FFFF	168000-16FFFF	32			130000-137FFF
32		60000-67FFF	160000-167FFF	32			128000-12FFFF
32		58000-5FFFF	158000-15FFFF	32			120000-127FFF
32		50000-57FFF	150000-157FFF	32			118000-11FFFF
32		48000-4FFFF	148000-14FFFF	32			110000-117FFF

Table 2. 16- and 32-Mbit Word-Wide Memory Addressing Map (Sheet 2 of 3)

32		40000-47FFF	140000-147FFF	32			108000-10FFFF
32		38000-3FFFF	138000-13FFFF	32			100000-107FFF
32		30000-37FFF	130000-137FFF	32		F8000-FFFFF	0F8000-0FFFFF
32		28000-2FFFF	128000-12FFFF	32		F0000-F7FFF	0F0000-0F7FFF
32		20000-27FFF	120000-127FFF	32		E8000-EFFFF	0E8000-0EFFFF
32		18000-1FFFF	118000-11FFFF	32		E0000-E7FFF	0E0000-0E7FFF
32		10000-17FFF	110000-117FFF	32		D8000-DFFFF	0D8000-0DFFFF
32		08000-0FFFF	108000-10FFFF	32		D0000-D7FFF	0D0000-0D7FFF
32		00000-07FFF	100000-107FFF	32		C8000-CFFFF	0C8000-0CFFFF
This column continues on next page				This column continues on next page			

Table 2. 16- and 32-Mbit Word-Wide Memory Addressing Map (Sheet 3 of 3)

16-Mbit and 32-Mbit Word-Wide Memory Addressing (Continued)

Top Boot				Bottom Boot			
Size (KW)		16 Mbit	32 Mbit	Size (KW)		16 Mbit	32 Mbit
32			0F8000-0FFFFF	32		C0000-C7FFF	0C0000-0C7FFF
32			0F0000-0F7FFF	32		B8000-BFFFF	0B8000-0BFFFF
32			0E8000-0EFFFF	32		B0000-B7FFF	0B0000-0B7FFF
32			0E0000-0E7FFF	32		A8000-AFFFF	0A8000-0AFFFF
32			0D8000-0DFFFF	32		A0000-A7FFF	0A0000-0A7FFF
32			0D0000-0D7FFF	32		98000-9FFFF	098000-09FFFF
32			0C8000-0CFFFF	32		90000-97FFF	090000-097FFF
32			0C0000-0C7FFF	32		88000-8FFFF	088000-08FFFF
32			0B8000-0BFFFF	32		80000-87FFF	080000-087FFF
32			0B0000-0B7FFF	32		78000-7FFFF	78000-7FFFF
32			0A8000-0AFFFF	32		70000-77FFF	70000-77FFF
32			0A0000-0A7FFF	32		68000-6FFFF	68000-6FFFF
32			098000-09FFFF	32		60000-67FFF	60000-67FFF
32			090000-097FFF	32		58000-5FFFF	58000-5FFFF
32			088000-08FFFF	32		50000-57FFF	50000-57FFF
32			080000-087FFF	32		48000-4FFFF	48000-4FFFF
32			078000-07FFFF	32		40000-47FFF	40000-47FFF
32			070000-077FFF	32		38000-3FFFF	38000-3FFFF
32			068000-06FFFF	32		30000-37FFF	30000-37FFF
32			060000-067FFF	32		28000-2FFFF	28000-2FFFF
32			058000-05FFFF	32		20000-27FFF	20000-27FFF
32			050000-057FFF	32		18000-1FFFF	18000-1FFFF
32			048000-04FFFF	32		10000-17FFF	10000-17FFF
32			040000-047FFF	32		08000-0FFFF	08000-0FFFF
32			038000-03FFFF	4		07000-07FFF	07000-07FFF
32			030000-037FFF	4		06000-06FFF	06000-06FFF
32			028000-02FFFF	4		05000-05FFF	05000-05FFF
32			020000-027FFF	4		04000-04FFF	04000-04FFF
32			018000-01FFFF	4		03000-03FFF	03000-03FFF
32			010000-017FFF	4		02000-02FFF	02000-02FFF
32			008000-00FFFF	4		01000-01FFF	01000-01FFF
32			000000-007FFF	4		00000-00FFF	00000-00FFF

Table 3. 4- and 8-Mbit Word-Wide Memory Addressing Map

4-Mbit and 8-Mbit Word-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KW)	4 Mbit			Size (KW)	4 Mbit	8 Mbit	
	3F000-3FFFF	7F000-7FFFF		32		78000-7FFFF	
	3E000-3EFFF	7E000-7EFFF		32		70000-77FFF	
	3D000-3DFFF	7D000-7DFFF		32		68000-6FFFF	
	3C000-3CFFF	7C000-7CFFF		32		60000-67FFF	
	3B000-3BFFF	7B000-7BFFF		32		58000-5FFFF	
	3A000-3AFFF	7A000-7AFFF		32		50000-57FFF	
	39000-39FFF	79000-79FFF		32		48000-4FFFF	
	38000-38FFF	78000-78FFF		32		40000-47FFF	
4	30000-37FFF	70000-77FFF		32	38000-3FFFF	38000-3FFFF	
4	28000-2FFFF	68000-6FFFF		32	30000-37FFF	30000-37FFF	
4	20000-27FFF	60000-67FFF		32	28000-2FFFF	28000-2FFFF	
4	18000-1FFFF	58000-5FFFF		32	20000-27FFF	20000-27FFF	
4	10000-17FFF	50000-57FFF		32	18000-1FFFF	18000-1FFFF	
4	08000-0FFFF	48000-4FFFF		32	10000-17FFF	10000-17FFF	
4	00000-07FFF	40000-47FFF		32	08000-0FFFF	08000-0FFFF	
4		38000-3FFFF		4	07000-07FFF	07000-07FFF	
32		30000-37FFF		4	06000-06FFF	06000-06FFF	
32		28000-2FFFF		4	05000-05FFF	05000-05FFF	
32		20000-27FFF		4	04000-04FFF	04000-04FFF	
32		18000-1FFFF		4	03000-03FFF	03000-03FFF	
32		10000-17FFF		4	02000-02FFF	02000-02FFF	
32		08000-0FFFF		4	01000-01FFF	01000-01FFF	
32		00000-07FFF		4	00000-00FFF	00000-00FFF	

Table 4. 16-, 32-, and 64-Mbit Word-Wide Memory Addressing Map (Sheet 1 of 5)

16-Mbit, 32-Mbit, and 64-Mbit Word-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KW)	16 Mbit	32 Mbit	64 Mbit	Size (KW)	16 Mbit	32 Mbit	64 Mbit
4	FF000-FFFFF	1FF000-1FFFFF	3FF000-3FFFFF	32			3F8000-3FFFFF
4	FE000-FEFFF	1FE000-1FEFFF	3FE000-3FEFFF	32			3F0000-3F7FFF
4	FD000-FDFFF	1FD000-1FDFFF	3FD000-3FDFFF	32			3E8000-3EFFFF
4	FC000-FCFFF	1FC000-1FCFFF	3FC000-3FCFFF	32			3E0000-3E7FFF
4	FB000-FBFFF	1FB000-1FBFFF	3FB000-3FBFFF	32			3D8000-3DFFFF
4	FA000-FAFFF	1FA000-1FAFFF	3FA000-3FAFFF	32			3D0000-3D7FFF
4	F9000-F9FFF	1F9000-1F9FFF	3F9000-3F9FFF	32			3C8000-3CFFFF
4	F8000-F8FFF	1F8000-1F8FFF	3F8000-3F8FFF	32			3C0000-3C7FFF
32	F0000-F7FFF	1F0000-1F7FFF	3F0000-3F7FFF	32			3B8000-3BFFFF
32	E8000-EFFFF	1E8000-1EFFFF	3E8000-3EFFFF	32			3B0000-3B7FFF
32	E0000-E7FFF	1E0000-1E7FFF	3E0000-3E7FFF	32			3A8000-3AFFFF
32	D8000-DFFFF	1D8000-1DFFFF	3D8000-3DFFFF	32			3A0000-3A7FFF
32	D0000-D7FFF	1D0000-1D7FFF	3D0000-3D7FFF	32			398000-39FFFF
32	C8000-CFFFF	1C8000-1CFFFF	3C8000-3CFFFF	32			390000-397FFF
32	C0000-C7FFF	1C0000-1C7FFF	3C0000-3C7FFF	32			388000-38FFFF
32	B8000-BFFFF	1B8000-1BFFFF	3B8000-3BFFFF	32			380000-387FFF
32	B0000-B7FFF	1B0000-1B7FFF	3B0000-3B7FFF	32			378000-37FFFF
32	A8000-AFFFF	1A8000-1AFFFF	3A8000-3AFFFF	32			370000-377FFF
32	A0000-A7FFF	1A0000-1A7FFF	3A0000-3A7FFF	32			368000-36FFFF
32	98000-9FFFF	198000-19FFFF	398000-39FFFF	32			360000-367FFF
32	90000-97FFF	190000-197FFF	390000-397FFF	32			358000-35FFFF
32	88000-8FFFF	188000-18FFFF	388000-38FFFF	32			350000-357FFF
32	80000-87FFF	180000-187FFF	380000-387FFF	32			348000-34FFFF
32	78000-7FFFF	178000-17FFFF	378000-37FFFF	32			340000-347FFF
32	70000-77FFF	170000-177FFF	370000-377FFF	32			338000-33FFFF
32	68000-6FFFF	168000-16FFFF	368000-36FFFF	32			330000-337FFF
32	60000-67FFF	160000-167FFF	360000-367FFF	32			328000-32FFFF
32	58000-5FFFF	158000-15FFFF	358000-35FFFF	32			320000-327FFF
32	50000-57FFF	150000-157FFF	350000-357FFF	32			318000-31FFFF
32	48000-4FFFF	148000-14FFFF	348000-34FFFF	32			310000-317FFF
32	40000-47FFF	140000-147FFF	340000-347FFF	32			308000-30FFFF
32	38000-3FFFF	138000-13FFFF	338000-33FFFF	32			300000-307FFF
32	30000-37FFF	130000-137FFF	330000-337FFF	32			2F8000-2FFFFF
32	28000-2FFFF	128000-12FFFF	328000-32FFFF	32			2F0000-2F7FFF
32	20000-27FFF	120000-127FFF	320000-327FFF	32			2E8000-2EFFFF
32	18000-1FFFF	118000-11FFFF	318000-31FFFF	32			2E0000-2E7FFF
32	10000-17FFF	110000-117FFF	310000-317FFF	32			2D8000-2DFFFF

Table 4. 16-, 32-, and 64-Mbit Word-Wide Memory Addressing Map (Sheet 2 of 5)

32	08000-0FFFF	108000-10FFFF	308000-30FFFF	32			2D0000-2D7FFF
32	00000-07FFF	100000-107FFF	300000-307FFF	32			2C8000-2CFFFF
32		0F8000-0FFFFF	2F8000-2FFFFF	32			2C0000-2C7FFF
32		0F0000-0F7FFF	2F0000-2F7FFF	32			2B8000-2BFFFF
32		0E8000-0EFFFF	2E8000-2EFFFF	32			2B0000-2B7FFF
32		0E0000-0E7FFF	2E0000-2E7FFF	32			2A8000-2AFFFF
32		0D8000-0DFFFF	2D8000-2DFFFF	32			2A0000-2A7FFF
32		0D0000-0D7FFF	2D0000-2D7FFF	32			298000-29FFFF
32		0C8000-0CFFFF	2C8000-2CFFFF	32			290000-297FFF
32		0C0000-0C7FFF	2C0000-2C7FFF	32			288000-28FFFF
32		0B8000-0BFFFF	2B8000-2BFFFF	32			280000-287FFF
32		0B0000-0B7FFF	2B0000-2B7FFF	32			278000-27FFFF
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Table 4. 16-, 32-, and 64-Mbit Word-Wide Memory Addressing Map (Sheet 3 of 5)

16-Mbit, 32-Mbit, and 64-Mbit Word-Wide Memory Addressing (Continued)

Top Boot				Bottom Boot			
Size (KW)	16 Mbit	32 Mbit	64 Mbit	Size (KW)	16 Mbit	32 Mbit	64 Mbit
32		0A8000-0AFFFF	2A8000-2AFFFF	32			270000-277FFF
32		0A0000-0A7FFF	2A0000-2A7FFF	32			268000-26FFFF
32		098000-09FFFF	298000-29FFFF	32			260000-267FFF
32		090000-097FFF	290000-297FFF	32			258000-25FFFF
32		088000-08FFFF	288000-28FFFF	32			250000-257FFF
32		080000-087FFF	280000-287FFF	32			248000-24FFFF
32		078000-07FFFF	278000-27FFFF	32			240000-247FFF
32		070000-077FFF	270000-277FFF	32			238000-23FFFF
32		068000-06FFFF	268000-26FFFF	32			230000-237FFF
32		060000-067FFF	260000-267FFF	32			228000-22FFFF
32		058000-05FFFF	258000-25FFFF	32			220000-227FFF
32		050000-057FFF	250000-257FFF	32			218000-21FFFF
32		048000-04FFFF	248000-24FFFF	32			210000-217FFF
32		040000-047FFF	240000-247FFF	32			208000-20FFFF
32		038000-03FFFF	238000-23FFFF	32			200000-207FFF
32		030000-037FFF	230000-237FFF	32		1F8000-1FFFFF	1F8000-1FFFFF
32		028000-02FFFF	228000-22FFFF	32		1F0000-1F7FFF	1F0000-1F7FFF
32		020000-027FFF	220000-227FFF	32		1E8000-1EFFFF	1E8000-1EFFFF
32		018000-01FFFF	218000-21FFFF	32		1E0000-1E7FFF	1E0000-1E7FFF
32		010000-017FFF	210000-217FFF	32		1D8000-1DFFFF	1D8000-1DFFFF
32		008000-00FFFF	208000-21FFFF	32		1D0000-1D7FFF	1D0000-1D7FFF
32		000000-007FFF	200000-207FFF	32		1C8000-1CFFFF	1C8000-1CFFFF
32			1F8000-1FFFFF	32		1C0000-1C7FFF	1C0000-1C7FFF
32			1F0000-1F7FFF	32		1B8000-1BFFFF	1B8000-1BFFFF
32			1E8000-1EFFFF	32		1B0000-1B7FFF	1B0000-1B7FFF
32			1E0000-1E7FFF	32		1A8000-1AFFFF	1A8000-1AFFFF
32			1D8000-1DFFFF	32		1A0000-1A7FFF	1A0000-1A7FFF
32			1D0000-1D7FFF	32		198000-19FFFF	198000-19FFFF
32			1C8000-1CFFFF	32		190000-197FFF	190000-197FFF
32			1C0000-1C7FFF	32		188000-18FFFF	188000-18FFFF
32			1B8000-1BFFFF	32		180000-187FFF	180000-187FFF
32			1B0000-1B7FFF	32		178000-17FFFF	178000-17FFFF
32			1A8000-1AFFFF	32		170000-177FFF	170000-177FFF
32			1A0000-1A7FFF	32		168000-16FFFF	168000-16FFFF
32			198000-19FFFF	32		160000-167FFF	160000-167FFF
32			190000-197FFF	32		158000-15FFFF	158000-15FFFF
32			188000-18FFFF	32		150000-157FFF	150000-157FFF

Table 4. 16-, 32-, and 64-Mbit Word-Wide Memory Addressing Map (Sheet 4 of 5)

32			180000-187FFF	32		148000-14FFFF	148000-14FFFF
32			178000-17FFFF	32		140000-147FFF	140000-147FFF
32			170000-177FFF	32		138000-13FFFF	138000-13FFFF
32			168000-16FFFF	32		130000-137FFF	130000-137FFF
32			160000-167FFF	32		128000-12FFFF	128000-12FFFF
32			158000-15FFFF	32		120000-127FFF	120000-127FFF
32			150000-157FFF	32		118000-11FFFF	118000-11FFFF
32			148000-14FFFF	32		110000-117FFF	110000-117FFF
32			140000-147FFF	32		108000-10FFFF	108000-10FFFF
32			138000-13FFFF	32		100000-107FFF	100000-107FFF
32			130000-137FFF	32	F8000-FFFFF	F8000-FFFFF	F8000-FFFFF
32			128000-12FFFF	32	F0000-F7FFF	F0000-F7FFF	F0000-F7FFF
32			120000-127FFF	32	E8000-EFFFF	E8000-EFFFF	E8000-EFFFF
32			118000-11FFFF	32	E0000-E7FFF	E0000-E7FFF	E0000-E7FFF
32			110000-117FFF	32	D8000-DFFFF	D8000-DFFFF	D8000-DFFFF
32			108000-10FFFF	32	D0000-D7FFF	D0000-D7FFF	D0000-D7FFF
32			100000-107FFF	32	C8000-CFFFF	C8000-CFFFF	C8000-CFFFF
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Table 4. 16-, 32-, and 64-Mbit Word-Wide Memory Addressing Map (Sheet 5 of 5)

16-Mbit, 32-Mbit, and 64-Mbit Word-Wide Memory Addressing (Continued)

Top Boot				Bottom Boot			
Size (KW)	16 Mbit	32 Mbit	64 Mbit	Size (KW)	16 Mbit	32 Mbit	64 Mbit
32			0F8000-0FFFFF	32	C0000-C7FFF	C0000-C7FFF	C0000-C7FFF
32			0F0000-0F7FFF	32	B8000-BFFFF	B8000-BFFFF	B8000-BFFFF
32			0E8000-0EFFFF	32	B0000-B7FFF	B0000-B7FFF	B0000-B7FFF
32			0E0000-0E7FFF	32	A8000-AFFFF	A8000-AFFFF	A8000-AFFFF
32			0D8000-0DFFFF	32	A0000-A7FFF	A0000-A7FFF	A0000-A7FFF
32			0D0000-0D7FFF	32	98000-9FFFF	98000-9FFFF	98000-9FFFF
32			0C8000-0CFFFF	32	90000-97FFF	90000-97FFF	90000-97FFF
32			0C0000-0C7FFF	32	88000-8FFFF	88000-8FFFF	88000-8FFFF
32			0B8000-0BFFFF	32	80000-87FFF	80000-87FFF	80000-87FFF
32			0B0000-0B7FFF	32	78000-7FFFF	78000-7FFFF	78000-7FFFF
32			0A8000-0AFFFF	32	70000-77FFF	70000-77FFF	70000-77FFF
32			0A0000-0A7FFF	32	68000-6FFFF	68000-6FFFF	68000-6FFFF
32			098000-09FFFF	32	60000-67FFF	60000-67FFF	60000-67FFF
32			090000-097FFF	32	58000-5FFFF	58000-5FFFF	58000-5FFFF
32			088000-08FFFF	32	50000-57FFF	50000-57FFF	50000-57FFF
32			080000-087FFF	32	48000-4FFFF	48000-4FFFF	48000-4FFFF
32			078000-07FFFF	32	40000-47FFF	40000-47FFF	40000-47FFF
32			070000-077FFF	32	38000-3FFFF	38000-3FFFF	38000-3FFFF
32			068000-06FFFF	32	30000-37FFF	30000-37FFF	30000-37FFF
32			060000-067FFF	32	28000-2FFFF	28000-2FFFF	28000-2FFFF
32			058000-05FFFF	32	20000-27FFF	20000-27FFF	20000-27FFF
32			050000-057FFF	32	18000-1FFFF	18000-1FFFF	18000-1FFFF
32			048000-04FFFF	32	10000-17FFF	10000-17FFF	10000-17FFF
32			040000-047FFF	32	08000-0FFFF	08000-0FFFF	08000-0FFFF
32			038000-03FFFF	4	07000-07FFF	07000-07FFF	07000-07FFF
32			030000-037FFF	4	06000-06FFF	06000-06FFF	06000-06FFF
32			028000-02FFFF	4	05000-05FFF	05000-05FFF	05000-05FFF
32			020000-027FFF	4	04000-04FFF	04000-04FFF	04000-04FFF
32			018000-01FFFF	4	03000-03FFF	03000-03FFF	03000-03FFF
32			010000-017FFF	4	02000-02FFF	02000-02FFF	02000-02FFF
32			008000-00FFFF	4	01000-01FFF	01000-01FFF	01000-01FFF
32			000000-007FFF	4	00000-00FFF	00000-00FFF	00000-00FFF

3.2.4 4-, 8-, and 16-Mbit Byte-Wide Memory Maps

Table 5. 8- and 16-Mbit Byte-Wide Memory Addressing Map (Sheet 1 of 3)

8-Mbit and 16-Mbit Byte-Wide Byte-Wide Memory Addressing

Top Boot			Bottom Boot		
Size (KB)	8 Mbit	16 Mbit	Size (KB)	8 Mbit	16 Mbit
8	FE000-FFFFF	1FE000-1FFFFF	64		
8	FC000-FDFFF	1FC000-1FDFFF	64		
8	FA000-FBFFF	1FA000-1FBFFF	64		
8	F8000-F9FFF	1F8000-1F9FFF	64		
8	F6000-F7FFF	1F6000-1F7FFF	64		
8	F4000-F5FFF	1F4000-1F5FFF	64		
8	F2000-F3FFF	1F2000-1F3FFF	64		
8	F0000-F1FFF	1F0000-1F1FFF	64		
64	E0000-EFFFF	1E0000-1EFFFF	64		
64	D0000-DFFFF	1D0000-1DFFFF	64		
64	C0000-CFFFF	1C0000-1CFFFF	64		
64	B0000-BFFFF	1B0000-1BFFFF	64		
64	A0000-AFFFF	1A0000-1AFFFF	64		
64	90000-9FFFF	190000-19FFFF	64		
64	80000-8FFFF	180000-18FFFF	64		
64	70000-7FFFF	170000-17FFFF	64		
64	60000-6FFFF	160000-16FFFF	64		
64	50000-5FFFF	150000-15FFFF	64		
64	40000-4FFFF	140000-14FFFF	64		
64	30000-3FFFF	130000-13FFFF	64		
64	20000-2FFFF	120000-12FFFF	64		
64	10000-1FFFF	110000-11FFFF	64		
64	00000-0FFFF	100000-10FFFF	64		
64		0F0000-0FFFFF	64		
64		0E0000-0EFFFF	64		
64		0D0000-0DFFFF	64		
64		0C0000-0CFFFF	64		
64		0B0000-0BFFFF	64		
64		0A0000-0AFFFF	64		
64		090000-09FFFF	64		
64		080000-08FFFF	64		
64		070000-07FFFF	64		
64		060000-06FFFF	64		1F0000-1FFFFF

Table 5. 8- and 16-Mbit Byte-Wide Memory Addressing Map (Sheet 2 of 3)

64		050000-05FFFF	64		1E0000-1EFFFF
64		040000-04FFFF	64		1D0000-1DFFFF
64		030000-03FFFF	64		1C0000-1CFFFF
64		020000-02FFFF	64		1B0000-1BFFFF
64		010000-01FFFF	64		1A0000-1AFFFF
64		000000-00FFFF	64		190000-19FFFF
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Table 5. 8- and 16-Mbit Byte-Wide Memory Addressing Map (Sheet 3 of 3)

8-Mbit and 16-Mbit Byte-Wide Memory Addressing (Continued)

Top Boot			Bottom Boot		
Size (KB)	8 Mbit	16 Mbit	Size (KB)	8 Mbit	16 Mbit
64			64		180000-18FFFF
64			64		170000-17FFFF
64			64		160000-16FFFF
64			64		150000-15FFFF
64			64		140000-14FFFF
64			64		130000-13FFFF
64			64		120000-12FFFF
64			64		110000-11FFFF
64			64		100000-10FFFF
64			64	F0000-FFFFF	0F0000-0FFFFF
64			64	E0000-EFFFF	0E0000-0EFFFF
64			64	D0000-DFFFF	0D0000-0DFFFF
64			64	C0000-CFFFF	0C0000-0CFFFF
64			64	B0000-BFFFF	0B0000-0BFFFF
64			64	A0000-AFFFF	0A0000-0AFFFF
64			64	90000-9FFFF	090000-09FFFF
64			64	80000-8FFFF	080000-08FFFF
64			64	70000-7FFFF	070000-07FFFF
64			64	60000-6FFFF	060000-06FFFF
64			64	50000-5FFFF	050000-05FFFF
64			64	40000-4FFFF	040000-04FFFF
64			64	30000-3FFFF	030000-03FFFF
64			64	20000-2FFFF	020000-02FFFF
64			64	10000-1FFFF	010000-01FFFF
64			8	0E000-0FFFF	00E000-00FFFF
64			8	0C000-0DFFF	00C000-00DFFF
64			8	0A000-0BFFF	00A000-00BFFF
64			8	08000-09FFF	008000-009FFF
64			8	06000-07FFF	006000-007FFF
64			8	04000-05FFF	004000-005FFF
64			8	02000-03FFF	002000-003FFF
64			8	00000-01FFF	000000-001FFF

Table 6. 4-Mbit Byte Wide Memory Addressing Map

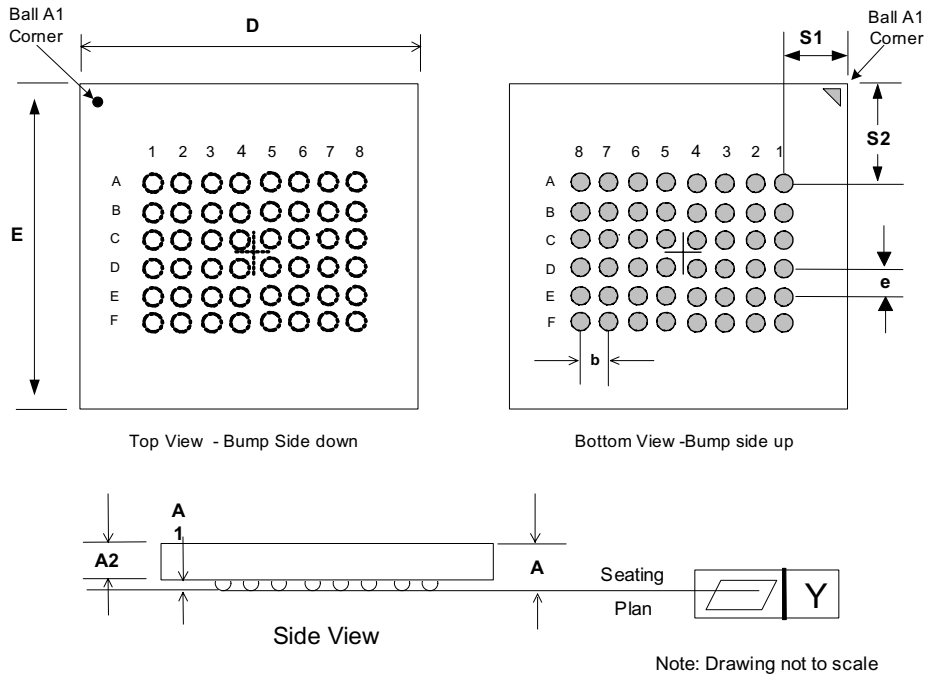
4-Mbit Byte-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KB)	4 Mbit			Size (KB)	4 Mbit		
8	7E000-7FFFF			64	70000-7FFFF		
8	7C000-7DFFF			64	60000-6FFFF		
8	7A000-7BFFF			64	50000-5FFFF		
8	78000-79FFF			64	40000-4FFFF		
8	76000-77FFF			64	30000-3FFFF		
8	74000-75FFF			64	20000-2FFFF		
8	72000-73FFF			64	10000-1FFFF		
8	70000-71FFF			8	0E000-0FFFF		
64	60000-6FFFF			8	0C000-0DFFF		
64	50000-5FFFF			8	0A000-0BFFF		
64	40000-4FFFF			8	08000-09FFF		
64	30000-3FFFF			8	06000-07FFF		
64	20000-2FFFF			8	04000-05FFF		
64	10000-1FFFF			8	02000-03FFF		
64	00000-0FFFF			8	00000-01FFF		

4.0 Package Information

4.1 µBGA* and Very Thin Profile Fine Pitch Ball Grid Array (VF BGA) Package

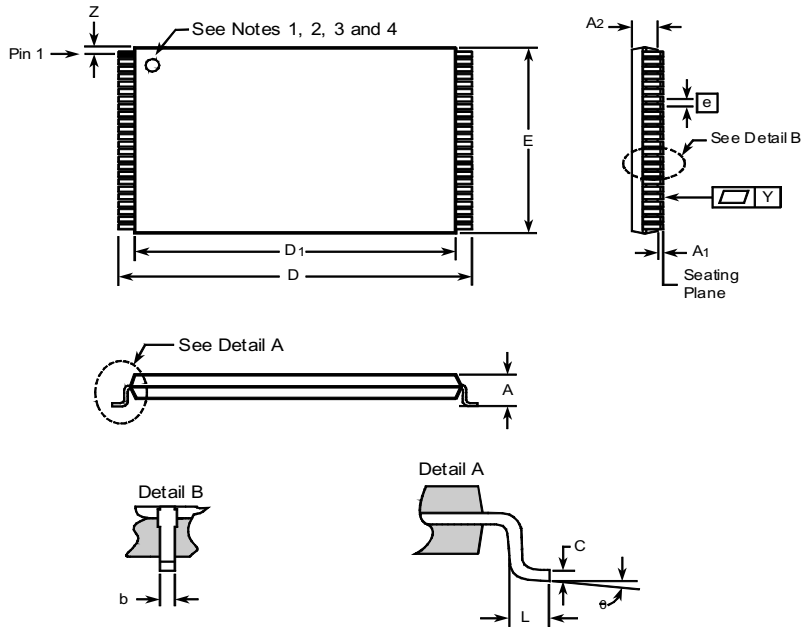
Figure 2. µBGA* and VF BGA Package Drawing



		Millimeters			Inches		
Dimensions	**Symbol**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
Package Height	A			1.000			0.0394
Ball Height	A1	0.150			0.0059		
Package Body Thickness	A2		0.665			0.0262	
Ball (Lead) Width	b	0.325	0.375	0.425	0.0128	0.0148	0.0167
Package Body Length 8M (.25)	D	7.810	7.910	8.010			
Package Body Length 16M (.25/.18/.13) 32M (.25/.18/.13)	D	7.186	7.286	7.386	0.2829	0.2868	0.2908
Package Body Length 64M (.18)	D	7.600	7.700	7.800	0.2992	0.3031	0.3071
Package Body Width 8M (.25)	E	6.400	6.500	6.600	0.2520	0.2559	0.2598
Package Body Width 16M (.25/.18/.13) 32M (.18/.13)	E	6.864	6.964	7.064	0.2702	0.2742	0.2781
Package Body Width 32M (.25)	E	10.750	10.850	10.860	0.4232	0.4272	0.4276
Package Body Width 64M (.18)	E	8.900	9.000	9.100	0.3504	0.3543	0.3583
Pitch	e		0.750			0.0295	
Ball (Lead) Count 8M, 16M	N		46			46	
Ball (Lead) Count 32M	N		47			47	
Ball (Lead) Count 64M	N		48			48	
Seating Plane Coplanarity	Y			0.100			0.0039
Corner to Ball A1 Distance Along D 8M (.25)	S1	1.230	1.330	1.430	0.0484	0.0524	0.0563
Corner to Ball A1 Distance Along D 16M (.25/.18/.13) 32M (.18/.13)	S1	0.918	1.018	1.118	0.0361	0.0401	0.0440
Corner to Ball A1 Distance Along D 64M (.18)	S1	1.125	1.225	1.325	0.0443	0.0482	0.0522
Corner to Ball A1 Distance Along E 8M (.25)	S2	1.275	1.375	1.475	0.0502	0.0541	0.0581
Corner to Ball A1 Distance Along E 16M (.25/.18/.13) 32M (.18/.13)	S2	1.507	1.607	1.707	0.0593	0.0633	0.0672
Corner to Ball A1 Distance Along E 32M (.25)	S2	3.450	3.550	3.650	0.1358	0.1398	0.1437
Corner to Ball A1 Distance Along E 64M (.18)	S2	2.525	2.625	2.725	0.0994	0.1033	0.1073

4.2 TSOP Package

Figure 3. TSOP Package Drawing



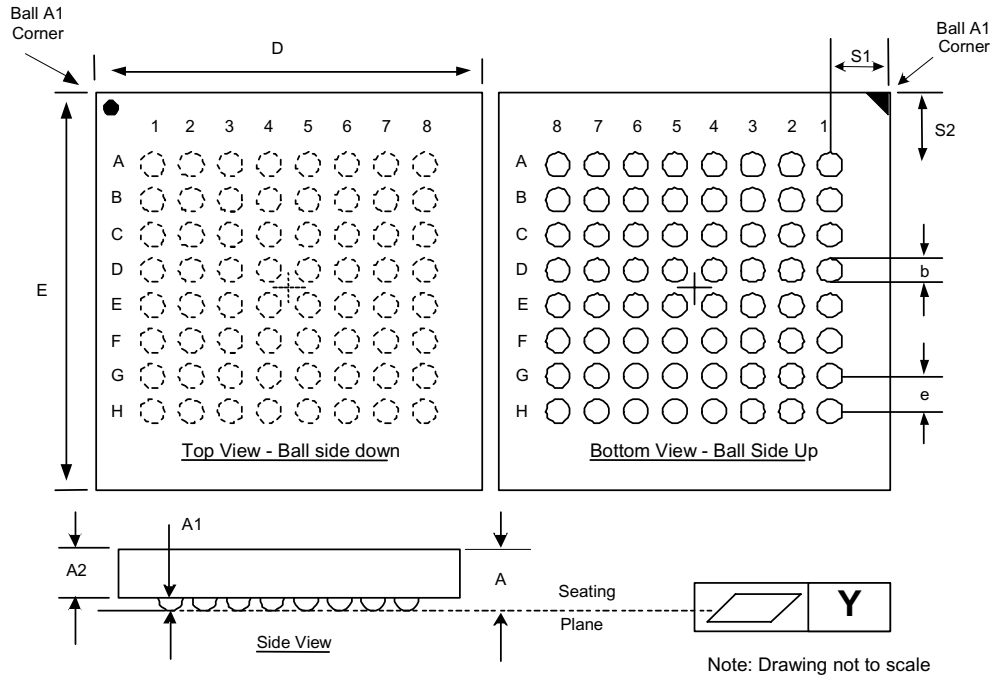
Dimensions

Family: Thin Small Outline Package									
	Symbol	Millimeters				Inches			
		Min	Nom	Max	Notes	Min	Nom	Max	Notes
Package Height	A			1.200				0.047	
Standoff	A1	0.050				0.002			
Package Body Thickness	A2	0.950	1.000	1.050		0.037	0.039	0.041	
Lead Width	b	0.150	0.200	0.300		0.006	0.008	0.012	
Lead Thickness	c	0.100	0.150	0.200		0.004	0.006	0.008	
Plastic Body Length	D1	18.200	18.400	18.600		0.717	0.724	0.732	
Package Body Width	E	11.800	12.000	12.200		0.465	0.472	0.480	
Lead Pitch	e		0.500				0.0197		
Terminal Dimension	D	19.800	20.000	20.200		0.780	0.787	0.795	
Lead Tip Length	L	0.500	0.600	0.700		0.020	0.024	0.028	
Lead Count	N		48				48		
Lead Tip Angle	Ø	0°	3°	5°		0°	3°	5°	
Seating Plane Coplanarity	Y			0.100				0.004	
Lead to Package Offset	Z	0.150	0.250	0.350		0.006	0.010	0.014	

NOTES:
1. One dimple on package denotes Pin 1.
2. If two dimples, then the larger dimple denotes Pin 1.
3. Pin 1 will always be in the upper left corner of the package, in reference to the product mark.

4.3 Easy BGA Package

Figure 4. Easy BGA Package Drawing



Dimensions Table

		Millimeters				Inches		
	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.200				0.0472
Ball Height	A1	0.250				0.0098		
Package Body Thickness	A2		0.780				0.0307	
Ball (Lead) Width	b	0.330	0.430	0.530		0.0130	0.0169	0.0209
Package Body Width	D	9.900	10.000	10.100	1	0.3898	0.3937	0.3976
Package Body Length	E	12.900	13.000	13.100	1	0.5079	0.5118	0.5157
Pitch	[e]		1.000				0.0394	
Ball (Lead) Count	N		64				64	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along D	S1	1.400	1.500	1.600	1	0.0551	0.0591	0.0630
Corner to Ball A1 Distance Along E	S2	2.900	3.000	3.100	1	0.1142	0.1181	0.1220

Note: (1) Package dimensions are for reference only. These dimensions are estimates based on die size, and are subject to change.

5.0 Pinout and Signal Descriptions

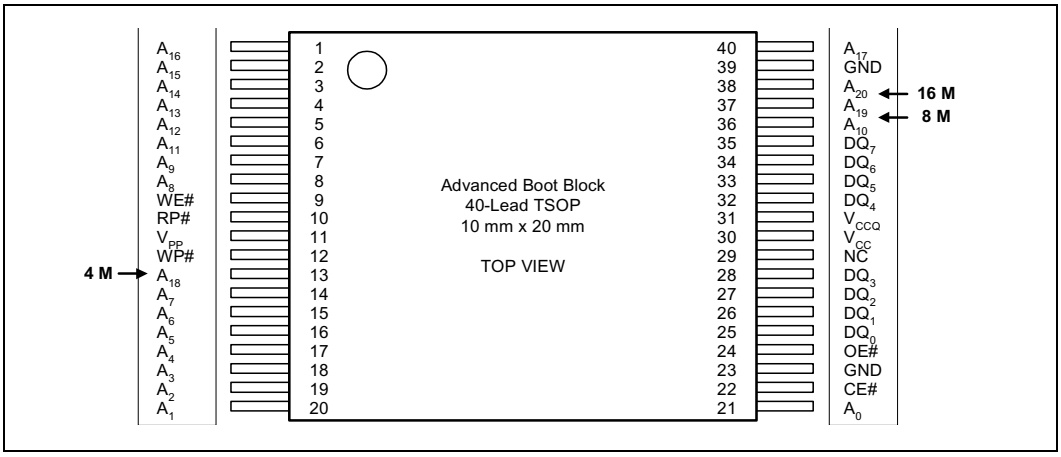
This section explains the package pinout and signal descriptions.

5.1 Signal Pinouts

The B3 flash memory device is available in 40-lead TSOP (x8, Figure 5), 48-lead TSOP (x16, Figure 6), 48-ball µBGA(x8 and x16, Figure 8 and Figure 9, respectively), and 48-ball VF BGA (x16, Figure 9) packages.

5.1.1 40-Lead and 48-Lead TSOP Packages

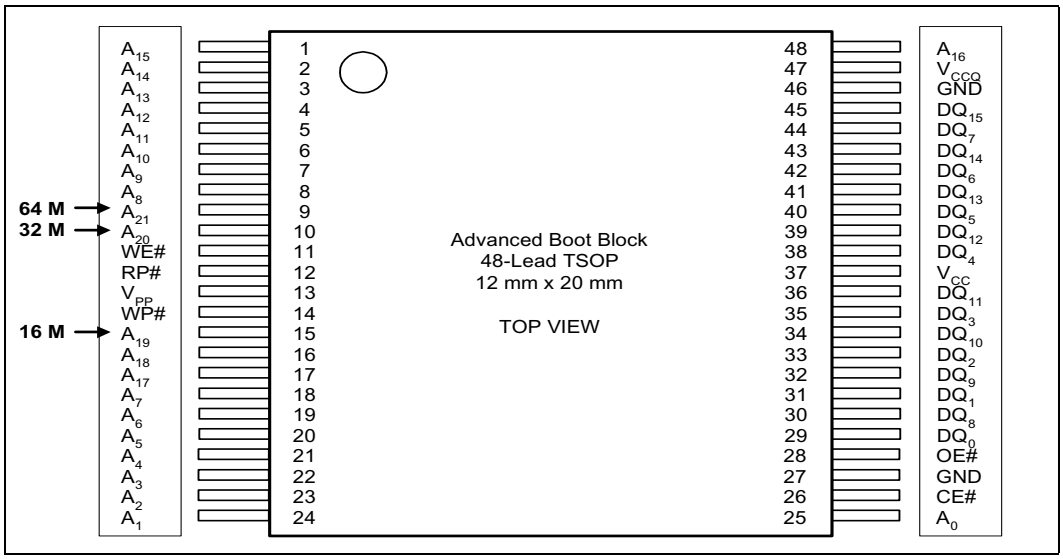
Figure 5. 40-Lead TSOP Package for x8 Configurations



0580_01

NOTES:
1. 40-Lead TSOP available for 8-Mbit and 16-Mbit densities only.
2. Lower densities have NC on the upper address pins. For example, an 8-Mbit device will have NC on Pin 38.

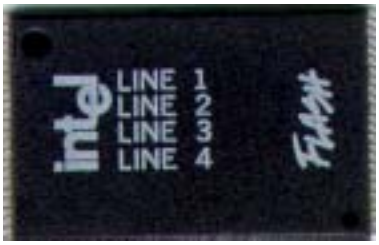
Figure 6. 48-Lead TSOP Package for x16 Configurations



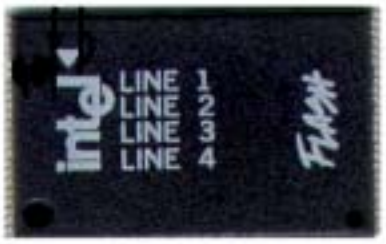
0580_02

Figure 7. New Mark for Pin-1 Indicator: 40-Lead 8/16 Mb TSOP and 48-Lead 8/16/32 Mb TSOP

Current Mark:



New Mark:



Note: The topside marking on 8-Mb, 16-Mb, and 32-Mb Intel® Advanced Boot Block 40L and 48L TSOP products will convert to a white ink triangle as a Pin-1 indicator. Products without the white triangle will continue to use a dimple as a Pin-1 indicator. There are no other changes in package size, materials, functionality, customer handling, or manufacturability. Product will continue to

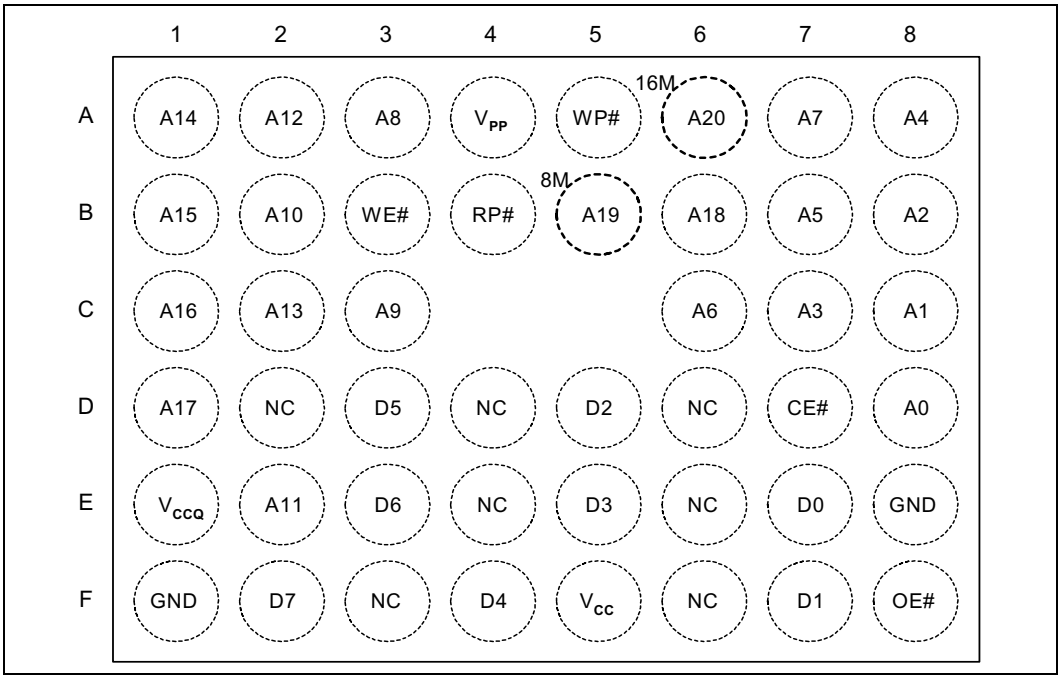
meet stringent Intel quality requirements. Table 7 lists the ordering codes of the affected products. See also Table 31, “Ordering Information: Valid Combinations” on page 69.

Table 7. B3 Flash Memory Device Ordering Information

Ordering Information Valid Combinations

	40-Lead TSOP		48-Lead TSOP	
Ext. Temp. 64 Mbit			TE28F640B3TC70	TE28F640B3BC70
Ext. Temp. 32 Mbit			TE28F320B3TD70 TE28F320B3TC70 TE28F320B3TC90 TE28F320B3TA100 TE28F320B3TA110	TE28F320B3BD70 TE28F320B3BC70 TE28F320B3BC90 TE28F320B3BA100 TE28F320B3BA110
Ext. Temp. 16 Mbit	TE28F016B3TA90 TE28F016B3TA110	TE28F016B3BA90 TE28F016B3BA110	TE28F160B3TC70 TE28F160B3TC80 TE28F160B3TA90 TE28F160B3TA110	TE28F160B3BC70 TE28F160B3BC80 TE28F160B3BA90 TE28F160B3BA110
Ext. Temp. 8 Mbit	TE28F008B3TA90 TE28F008B3TA110	TE28F008B3BA90 TE28F008B3BA110	TE28F800B3TA90 TE28F800B3TA110	TE28F800B3BA90 TE28F800B3BA110

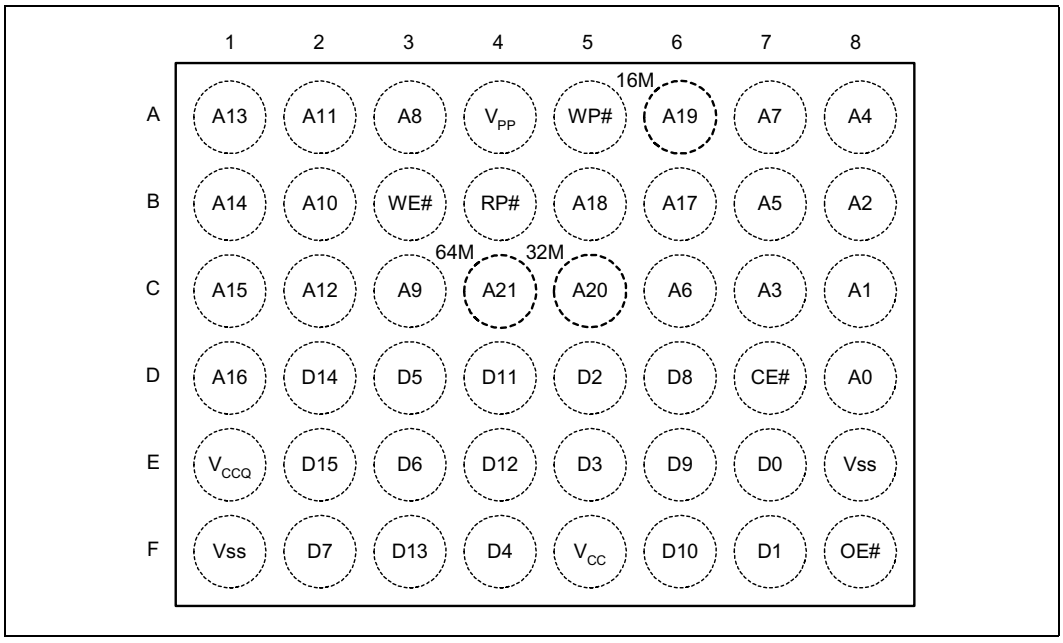
Figure 8. x8 48-Ball µBGA* Chip Size Package (Top View, Ball Down)



0580_04

NOTES:
1. A19 and A20 indicate the upgrade address connections. Lower density devices will not have the upper address solder balls. Intel recommends that routing is not done in this area. A_{20} is the upgrade address for the 16-Mbit device.

Figure 9. x16 48-Ball VF BGA and µBGA* Chip Size Package (Top View, Ball Down)



0580_03

NOTES:

1. A19, A20, and A21 indicate the upgrade address connections. Lower density devices will not have the upper address solder balls. Intel recommends that routing is not done in this area. A_{19} is the upgrade address for the
   16-Mbit device. A_{20} is the upgrade address for the 32-Mbit device. A_{21} is the upgrade address for the 64-Mbit device.
2. Table 8, “B3 Flash memory Device Signal Descriptions” on page 31 details the usage of each device pin.

5.2 Signal Descriptions

Table 8, "B3 Flash memory Device Signal Descriptions" on page 31 describes the active signals.

Table 8. B3 Flash memory Device Signal Descriptions (Sheet 1 of 2)

Symbol	Type	Description
A_0–A_{21}	Input	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a program or erase cycle. 28F008B3: A[0-19], 28F016B3: A[0-20], 28F800B3: A[0-18], 28F160B3: A[0-19], 28F320B3: A[0-20], 28F640B3: A[0-21]
DQ_0–DQ_7	Input/ Output	**DATA INPUTS/OUTPUTS:** Inputs array data on the second CE# and WE# cycle during a Program command. Inputs commands to the Command User Interface when CE# and WE# are active. Data is internally latched. Outputs array, identifier and Status Register data. The data pins float to tristate when the chip is de-selected or the outputs are disabled.
DQ_8–DQ_{15}	Input/ Output	**DATA INPUTS/OUTPUTS:** Inputs array data on the second CE# and WE# cycle during a Program command. Data is internally latched. Outputs array and identifier data. The data pins float to tristate when the chip is de-selected. **Not included on x8 products.**
CE#	Input	**CHIP ENABLE:** Activates the internal control logic, input buffers, decoders and sense amplifiers. CE# is active low. CE# high de-selects the memory device and reduces power consumption to standby levels.
OE#	Input	**OUTPUT ENABLE:** Enables the device's outputs through the data buffers during a Read operation. OE# is active low.
WE#	Input	**WRITE ENABLE:** Controls writes to the Command Register and memory array. WE# is active low. Addresses and data are latched on the rising edge of the second WE# pulse.
RP#	Input	**RESET/DEEP POWER-DOWN:** Uses two voltage levels (V_{IL}, V_{IH}) to control reset/deep power-down mode. **When RP# is at logic low, the device is in reset/deep power-down mode**, which drives the outputs to High-Z, resets the Write State Machine, and minimizes current levels (I_{CCD}). **When RP# is at logic high, the device is in standard operation**. When RP# transitions from logic-low to logic-high, the device defaults to the read array mode.
WP#	Input	**WRITE PROTECT:** Provides a method for locking and unlocking the two lockable parameter blocks. **When WP# is at logic low, the lockable blocks are locked**, preventing Program and Erase operations to those blocks. If a Program or Erase operation is attempted on a locked block, SR.1 and either SR.4 [program] or SR.5 [erase] will be set to indicate the operation failed. **When WP# is at logic high, the lockable blocks are unlocked** and can be programmed or erased. See Section 12.0, "Block Locking" on page 60 for details on write protection.
V_{CCQ}	Input	**OUTPUT V_{CC}:** Enables all outputs to be driven to 1.8 V to 2.5 V while the V_{CC} is at 2.7 V to 3.3 V. If the V_{CC} is regulated to 2.7 V to 2.85 V, V_{CCQ} can be driven at 1.65 V to 2.5 V to achieve lowest power operation (see Section 7.2, "DC Voltage Characteristics" on page 37). This input can be tied directly to V_{CC} (2.7 V to 3.6 V).
V_{CC}	Power	**DEVICE Power Supply:** 2.7 V to 3.6 V

Table 8. B3 Flash memory Device Signal Descriptions (Sheet 2 of 2)

Symbol	Type	Description
V_{PP}	Power	**PROGRAM/ERASE Power Supply:** Supplies power for Program and Erase operations. V_{PP} can be the same as V_{CC} (2.7 V to 3.6 V) for single supply voltage operation. For fast programming at manufacturing, 11.4 V to 12.6 V can be supplied to V_{PP}. This pin cannot be left floating. Applying 11.4 V to 12.6 V to V_{PP} can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V_{PP} can be connected to 12 V for a total of 80 hours maximum (see Section 13.0, "V_{PP} Program and Erase Voltages" on page 62 for details). $V_{PP} < V_{PPLK}$ protects memory contents against inadvertent or unintended program and erase commands.
GND	—	**Ground:** For all internal circuitry. All ground inputs **must** be connected.
NC	—	**No Connect:** Pin can be driven or left floating.

6.0 Maximum Ratings and Operating Conditions

6.1 Absolute Maximum Ratings

Warning: Stressing the device beyond the "Absolute Maximum Ratings" can cause permanent damage. These ratings are stress ratings only. Intel recommends that you do not operate the device beyond the "Operating Conditions" as extended exposure beyond the "Operating Conditions" can affect device reliability.

NOTICE: Specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

Table 9. Absolute Maximum Ratings

Parameter	Maximum Rating	Notes
Extended Operating Temperature		
During Read	–40 °C to +85 °C	
During Block Erase and Program	–40 °C to +85 °C	
Temperature under Bias	–40 °C to +85 °C	
Storage Temperature	–65 °C to +125 °C	
Voltage On Any Pin (except V_{CC} and V_{PP}) with Respect to GND	–0.5 V to +3.7 V	1
V_{PP} Voltage (for Block Erase and Program) with Respect to GND	–0.5 V to +13.5 V	1,2,3
V_{CC} and V_{CCQ} Supply Voltage with Respect to GND	–0.2 V to +3.6 V	
Output Short Circuit Current	100 mA	4

NOTES:
1. Minimum DC voltage is –0.5 V on input/output pins. During transitions, this level may undershoot to –2.0 V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} +0.5 V which, during transitions, may overshoot to V_{CC} +2.0 V for periods <20 ns.
2. Maximum DC voltage on V_{PP} may overshoot to +14.0 V for periods <20 ns.
3. V_{PP} Program voltage is normally 1.65 V to 3.6 V. Connection to a 11.4 V to 12.6 V supply can be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks during program/erase. V_{PP} may be connected to 12 V for a total of 80 hours maximum.
4. Output shorted for no more than one second. No more than one output shorted at a time.

6.2 Operating Conditions

Table 10. Temperature and Voltage Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
T_A	Operating Temperature	–40	+85	°C	
V_{CC1}	V_{CC} Supply Voltage	2.7	3.6	Volts	1, 2
V_{CC2}		3.0	3.6		1, 2
V_{CCQ1}	I/O Supply Voltage	2.7	3.6	Volts	1
V_{CCQ2}		1.65	2.5		
V_{CCQ3}		1.8	2.5		
V_{PP1}	Supply Voltage	1.65	3.6	Volts	1
V_{PP2}		11.4	12.6	Volts	1, 3
Cycling	Block Erase Cycling	100,000		Cycles	3

NOTES:
1. V_{CC} and V_{CCQ} must share the same supply when they are in the V_{CC1} range.
2. V_{CC}Max = 3.3 V for 0.25µm 32-Mbit devices.
3. Applying V_{PP} = 11.4 V–12.6 V during a program/erase can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V_{PP} can be connected to 12 V for a total of 80 hours maximum.

7.0 Electrical Specifications

7.1 DC Current Characteristics

Table 11. DC Current Characteristics (Sheet 1 of 2)

Sym	Parameter	V_{CC}	2.7 V–3.6 V		2.7 V–2.85 V		2.7 V–3.3 V		Unit	Test Conditions
		V_{CCQ}	2.7 V–3.6 V		1.65 V–2.5 V		1.8 V–2.5 V			
		Note	Typ	Max	Typ	Max	Typ	Max		
I_{LI}	Input Load Current	1,2		± 1		± 1		± 1	µA	$V_{CC} = V_{CC}Max$ $V_{CCQ} = V_{CCQ}Max$ $V_{IN} = V_{CCQ}$ or GND
I_{LO}	Output Leakage Current	1,2		± 10		± 10		± 10	µA	$V_{CC} = V_{CC}Max$ $V_{CCQ} = V_{CCQ}Max$ $V_{IN} = V_{CCQ}$ or GND
I_{CCS}	V_{CC} Standby Current for 0.13 and 0.18 Micron Product	1	7	15	20	50	150	250	µA	$V_{CC} = V_{CC}Max$ CE# = RP# = V_{CCQ} or during Program/ Erase Suspend WP# = V_{CCQ} or GND
	V_{CC} Standby Current for 0.25 Micron Product	1	10	25	20	50	150	250	µA	
I_{CCD}	V_{CC} Power-Down Current for 0.13 and 0.18 Micron Product	1,2	7	15	7	20	7	20	µA	$V_{CC} = V_{CC}Max$ $V_{CCQ} = V_{CCQ}Max$ $V_{IN} = V_{CCQ}$ or GND RP# = GND ± 0.2 V
	V_{CC} Power-Down Current for 0.25 Product	1,2	7	25	7	25	7	25	µA	
I_{CCR}	V_{CC} Read Current for 0.13 and 0.18 Micron Product	1,2,3	9	18	8	15	9	15	mA	$V_{CC} = V_{CC}Max$ $V_{CCQ} = V_{CCQ}Max$ OE# = V_{IH}, CE# = V_{IL} f = 5 MHz, I_{OUT}=0 mA Inputs = V_{IL} or V_{IH}
	V_{CC} Read Current for 0.25 Micron Product	1,2,3	10	18	8	15	9	15	mA	
I_{PPD}	V_{PP} Deep Power-Down Current	1	0.2	5	0.2	5	0.2	5	µA	RP# = GND ± 0.2 V $V_{PP} \le V_{CC}$
I_{CCW}	V_{CC} Program Current	1,4	18	55	18	55	18	55	mA	$V_{PP} = V_{PP1}$, Program in Progress
			8	22	10	30	10	30	mA	$V_{PP} = V_{PP2\ (12v)}$ Program in Progress
I_{CCE}	V_{CC} Erase Current	1,4	16	45	21	45	21	45	mA	$V_{PP} = V_{PP1}$, Erase in Progress
			8	15	16	45	16	45	mA	$V_{PP} = V_{PP2\ (12v)}$, Erase in Progress
I_{CCES}/ I_{CCWS}	V_{CC} Erase Suspend Current for 0.13 and 0.18 Micron Product	1,4,5	7	15	50	200	50	200	µA	CE# = V_{IH}, Erase Suspend in Progress
	V_{CC} Erase Suspend Current for 0.25 Micron Product		10	25	50	200	50	200	µA	
I_{PPR}	V_{PP} Read Current	1,4	2	±15	2	±15	2	±15	µA	$V_{PP} \le V_{CC}$
			50	200	50	200	50	200	µA	$V_{PP} > V_{CC}$

Table 11. DC Current Characteristics (Sheet 2 of 2)

Sym	Parameter	V_{CC}	2.7 V–3.6 V		2.7 V–2.85 V		2.7 V–3.3 V		Unit	Test Conditions
		V_{CCQ}	2.7 V–3.6 V		1.65 V–2.5 V		1.8 V–2.5 V			
		Note	Typ	Max	Typ	Max	Typ	Max		
I_{PPW}	V_{PP} Program Current	1,4	0.05	0.1	0.05	0.1	0.05	0.1	mA	V_{PP} =V_{PP1}, Program in Progress
			8	22	8	22	8	22	mA	V_{PP} = $V_{PP2\ (12v)}$ Program in Progress
I_{PPE}	V_{PP} Erase Current	1,4	0.05	0.1	0.05	0.1	0.05	0.1	mA	V_{PP} = V_{PP1}, Erase in Progress
			8	22	16	45	16	45	mA	V_{PP} = $V_{PP2\ (12v)}$, Erase in Progress
I_{PPES}/ I_{PPWS}	V_{CC} Erase Suspend Current	1,4	0.2	5	0.2	5	0.2	5	µA	V_{PP} = V_{PP1}, Program or Erase Suspend in Progress
			50	200	50	200	50	200	µA	V_{PP} = $V_{PP2\ (12v)}$, Program or Erase Suspend in Progress

NOTES:
1. All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC}, T_A = +25 °C.
2. The test conditions V_{CC}Max, V_{CCQ}Max, V_{CC}Min, and V_{CCQ}Min refer to the maximum or minimum V_{CC} or V_{CCQ} voltage listed at the top of each column. V_{CC}Max = 3.3 V for 0.25µm 32-Mbit devices.
3. Automatic Power Savings (APS) reduces I_{CCR} to approximately standby levels in static operation (CMOS inputs).
4. Sampled, not 100% tested.
5. I_{CCES} or I_{CCWS} is specified with device de-selected. If device is read while in erase suspend, current draw is sum of I_{CCES} and I_{CCR}. If the device is read while in program suspend, current draw is the sum of I_{CCWS} and I_{CCR}.

7.2 DC Voltage Characteristics

Table 12. DC Voltage Characteristics

Symbol	Parameter	V_{CC}	2.7 V–3.6 V		2.7 V–2.85 V		2.7 V–3.3 V		Unit	Test Conditions
		V_{CCQ}	2.7 V–3.6 V		1.65 V–2.5 V		1.8 V–2.5 V			
		Note	Min	Max	Min	Max	Min	Max		
V_{IL}	Input Low Voltage		–0.4	V_{CC} * 0.22 V	–0.4	0.4	–0.4	0.4	V	
V_{IH}	Input High Voltage		2.0	V_{CCQ} +0.3V	V_{CCQ} – 0.4V	V_{CCQ} +0.3V	V_{CCQ} – 0.4V	V_{CCQ} +0.3V	V	
V_{OL}	Output Low Voltage		–0.1	0.1	-0.1	0.1	-0.1	0.1	V	$V_{CC} = V_{CC}$Min $V_{CCQ} = V_{CCQ}$Min I_{OL} = 100 µA
V_{OH}	Output High Voltage		V_{CCQ} –0.1V		V_{CCQ} – 0.1V		V_{CCQ} – 0.1V		V	$V_{CC} = V_{CC}$Min $V_{CCQ} = V_{CCQ}$Min I_{OH} = –100 µA
V_{PPLK}	V_{PP} Lock-Out Voltage	1		1.0		1.0		1.0	V	Complete Write Protection
V_{PP1}	V_{PP} during Program / Erase Operations	1	1.65	3.6	1.65	3.6	1.65	3.6	V	
V_{PP2}		1,2	11.4	12.6	11.4	12.6	11.4	12.6	V	
V_{LKO}	V_{CC} Prog/ Erase Lock Voltage		1.5		1.5		1.5		V	
V_{LKO2}	V_{CCQ} Prog/ Erase Lock Voltage		1.2		1.2		1.2		V	

NOTES:
1. Erase and Program are inhibited when $V_{PP} < V_{PPLK}$ and not guaranteed outside the valid V_{PP} ranges of V_{PP1} and V_{PP2}.
2. Applying V_{PP} = 11.4 V–12.6 V during program/erase can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V_{PP} can be connected to 12 V for a total of 80 hours maximum.

8.0 AC Characteristics

8.1 AC Read Characteristics

Table 13. Read Operations—8-Mbit Density

#	Sym	Parameter	Density	8 Mbit								Unit
			Product	90 ns				110 ns				
			V_{CC}	3.0 V – 3.6 V		2.7 V – 3.6 V		3.0 V – 3.6 V		2.7 V – 3.6 V		
			Note	Min	Max	Min	Max	Min	Max	Min	Max	
R1	t_{AVAV}	Read Cycle Time	3,4	80		90		100		110		ns
R2	t_{AVQV}	Address to Output Delay	3,4		80		90		100		110	ns
R3	t_{ELQV}	CE# to Output Delay	1,3,4		80		90		100		110	ns
R4	t_{GLQV}	OE# to Output Delay	1,3,4		30		30		30		30	ns
R5	t_{PHQV}	RP# to Output Delay	3,4		150		150		150		150	ns
R6	t_{ELQX}	CE# to Output in Low Z	2,3,4	0		0		0		0		ns
R7	t_{GLQX}	OE# to Output in Low Z	2,3,4	0		0		0		0		ns
R8	t_{EHQZ}	CE# to Output in High Z	2,3,4		20		20		20		20	ns
R9	t_{GHQZ}	OE# to Output in High Z	2,3,4		20		20		20		20	ns
R10	t_{OH}	Output Hold from Address, CE#, or OE# Change, Whichever Occurs First	2,3,4	0		0		0		0		ns

NOTES:
1. OE# may be delayed up to t_{ELQV}–t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
2. Sampled, but not 100% tested.
3. See Figure 10, “Read Operation Waveform” on page 41.
4. See Figure 12, “AC Input/Output Reference Waveform” on page 47 for timing measurements and maximum allowable input slew rate.

Table 14. Read Operations—16-Mbit Density

#	Sym	Parameter	Density	16 Mbit												Unit	Notes
			Product	70 ns		80 ns		90 ns				110 ns					
			V_{CC}	2.7 V–3.6 V		2.7 V–3.6 V		3.0 V–3.6 V		2.7 V–3.6 V		3.0 V–3.6V		2.7 V–3.6V			
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
R1	t_{AVAV}	Read Cycle Time		70		80		80		90		100		110		ns	3,4
R2	t_{AVQV}	Address to Output Delay			70		80		80		90		100		110	ns	3,4
R3	t_{ELQV}	CE# to Output Delay			70		80		80		90		100		110	ns	1,3,4
R4	t_{GLQV}	OE# to Output Delay			20		20		30		30		30		30	ns	1,3,4
R5	t_{PHQV}	RP# to Output Delay			150		150		150		150		150		150	ns	3,4
R6	t_{ELQX}	CE# to Output in Low Z		0		0		0		0		0		0		ns	2,3,4
R7	t_{GLQX}	OE# to Output in Low Z		0		0		0		0		0		0		ns	2,3,4
R8	t_{EHQZ}	CE# to Output in High Z			20		20		20		20		20		20	ns	2,3,4
R9	t_{GHQZ}	OE# to Output in High Z			20		20		20		20		20		20	ns	2,3,4
R10	t_{OH}	Output Hold from Address, CE#, or OE# Change, Whichever Occurs First		0		0		0		0		0		0		ns	2,3,4

NOTES:
1. OE# may be delayed up to t_{ELQV}–t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
2. Sampled, but not 100% tested.
3. See Figure 10, “Read Operation Waveform” on page 41.
4. See Figure 12, “AC Input/Output Reference Waveform” on page 47 for timing measurements and maximum allowable input slew rate.

Table 15. Read Operations—32-Mbit Density

#	Sym	Para-meter	Density	32 Mbit												Unit	Notes
			Product	70 ns		90 ns		100 ns				110 ns					
			V_{CC}	2.7 V–3.6 V		2.7 V–3.6 V		3.0 V–3.3 V		2.7 V–3.3 V		3.0 V–3.3 V		2.7 V–3.3 V			
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
R1	t_{AVAV}	Read Cycle Time		70		90		90		100		100		110		ns	3,4
R2	t_{AVQV}	Address to Output Delay			70		90		90		100		100		110	ns	3,4
R3	t_{ELQV}	CE# to Output Delay			70		90		90		100		100		110	ns	1,3,4
R4	t_{GLQV}	OE# to Output Delay			20		20		30		30		30		30	ns	1,3,4
R5	t_{PHQV}	RP# to Output Delay			150		150		150		150		150		150	ns	3,4
R6	t_{ELQX}	CE# to Output in Low Z		0		0		0		0		0		0		ns	2,3,4
R7	t_{GLQX}	OE# to Output in Low Z		0		0		0		0		0		0		ns	2,3,4
R8	t_{EHQZ}	CE# to Output in High Z			20		20		20		20		20		20	ns	2,3,4
R9	t_{GHQZ}	OE# to Output in High Z			20		20		20		20		20		20	ns	2,3,4
R10	t_{OH}	Output Hold from Address, CE#, or OE# Change, Whichever Occurs First		0		0		0		0		0		0		ns	2,3,4

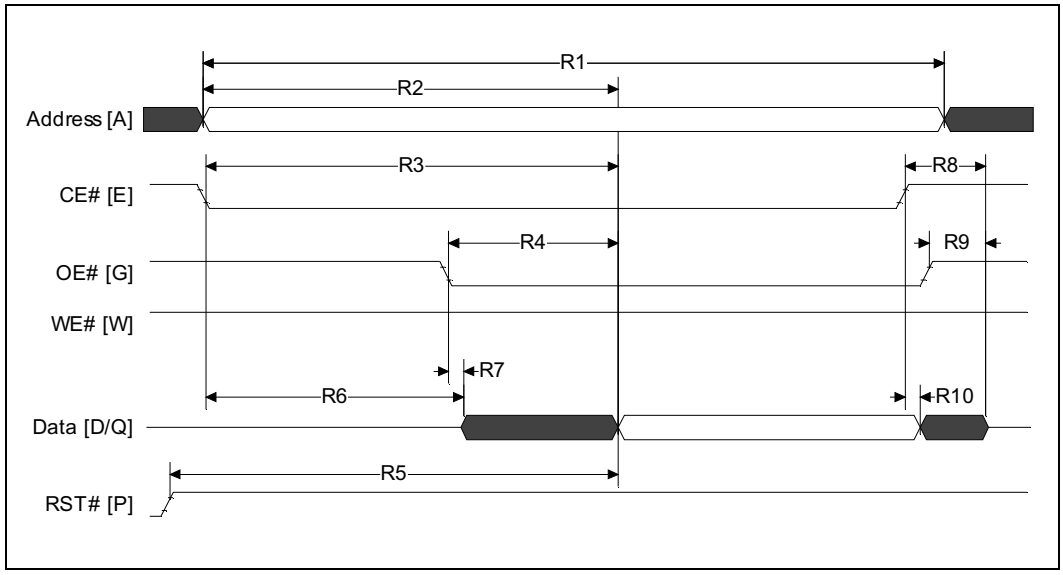
NOTES:
1. OE# may be delayed up to t_{ELQV}–t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
2. Sampled, but not 100% tested.
3. See Figure 10, “Read Operation Waveform” on page 41.
4. See Figure 12, “AC Input/Output Reference Waveform” on page 47 for timing measurements and maximum allowable input slew rate.

Table 16. Read Operations — 64-Mbit Density

#	Sym	Parameter	Density	64 Mbit				Unit
			Product	70 ns		80 ns		
			V_{CC}	2.7 V–3.6 V		2.7 V–3.6 V		
			Note	Min	Max	Min	Max	
R1	t_{AVAV}	Read Cycle Time	3,4	70		80		ns
R2	t_{AVQV}	Address to Output Delay	3,4		70		80	ns
R3	t_{ELQV}	CE# to Output Delay	1,3,4		70		80	ns
R4	t_{GLQV}	OE# to Output Delay	1,3,4		20		20	ns
R5	t_{PHQV}	RP# to Output Delay	3,4		150		150	ns
R6	t_{ELQX}	CE# to Output in Low Z	2,3,4	0		0		ns
R7	t_{GLQX}	OE# to Output in Low Z	2,3,4	0		0		ns
R8	t_{EHQZ}	CE# to Output in High Z	2,3,4		20		20	ns
R9	t_{GHQZ}	OE# to Output in High Z	2,3,4		20		20	ns
R10	t_{OH}	Output Hold from Address, CE#, or OE# Change, Whichever Occurs First	2,3,4	0		0		ns

NOTES:
1. OE# may be delayed up to t_{ELQV}–t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
2. Sampled, but not 100% tested.
3. See Figure 10, “Read Operation Waveform” on page 41.
4. See Figure 12, “AC Input/Output Reference Waveform” on page 47 for timing measurements and maximum allowable input slew rate.

Figure 10. Read Operation Waveform



8.2 AC Write Characteristics

Table 17. Write Operations—8-Mbit Density

#	Sym	Parameter	Density			8 Mbit				Unit
			Product			90 ns		110 ns		
			V_{CC}	3.0 V – 3.6 V		80		100		
				2.7 V – 3.6 V			90		110	
					Note	Min	Min	Min	Min	
W1	t_{PHWL} / t_{PHEL}	RP# High Recovery to WE# (CE#) Going Low			4,5	150	150	150	150	ns
W2	t_{ELWL} / t_{WLEL}	CE# (WE#) Setup to WE# (CE#) Going Low			4,5	0	0	0	0	ns
W3	t_{WLWH} / t_{ELEH}	WE# (CE#) Pulse Width			4,5	50	60	70	70	ns
W4	t_{DVWH} / t_{DVEH}	Data Setup to WE# (CE#) Going High			2,4,5	50	50	60	60	ns
W5	t_{AVWH} / t_{AVEH}	Address Setup to WE# (CE#) Going High			2,4,5	50	60	70	70	ns
W6	t_{WHEH} / t_{EHWH}	CE# (WE#) Hold Time from WE# (CE#) High			4,5	0	0	0	0	ns
W7	t_{WHDX} / t_{EHDX}	Data Hold Time from WE# (CE#) High			2,4,5	0	0	0	0	ns
W8	t_{WHAX} / t_{EHAX}	Address Hold Time from WE# (CE#) High			2,4,5	0	0	0	0	ns
W9	t_{WHWL} / t_{EHEL}	WE# (CE#) Pulse Width High			2,4,5	30	30	30	30	ns
W10	t_{VPWH} / t_{VPEH}	V_{PP} Setup to WE# (CE#) Going High			3,4,5	200	200	200	200	ns
W11	t_{QVVL}	V_{PP} Hold from Valid SRD			3,4	0	0	0	0	ns
W12	t_{BHWH} / t_{BHEH}	WP# Setup to WE# (CE#) Going High			3,4	0	0	0	0	ns
W13	t_{QVBL}	WP# Hold from Valid SRD			3,4	0	0	0	0	ns
W14	t_{WHGL}	WE# High to OE# Going Low			3,4	30	30	30	30	ns

NOTES:
1. Write pulse width (t_{WP}) is defined from CE# or WE# going low (whichever goes low last) to CE# or WE# going high (whichever goes high first). Hence, $t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$. Similarly, write pulse width high (t_{WPH}) is defined from CE# or WE# going high (whichever goes high first) to CE# or WE# going low (whichever goes low last). Hence, $t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$.
2. Refer to Table 25, "Bus Operations[1]" on page 52 for valid A_{IN} or D_{IN}.
3. Sampled, but not 100% tested.
4. See Figure 12, "AC Input/Output Reference Waveform" on page 47 for timing measurements and maximum allowable input slew rate.
5. See Figure 11, "Write Operations Waveform" on page 46.

Table 18. Write Operations—16-Mbit Density

#	Sym	Parameter	Density		16 Mbit						Unit
			Product		70 ns	80 ns	90 ns		110 ns		
			V_{CC}	3.0 V – 3.6 V			80		100		
				2.7 V – 3.6 V	70	80		90		110	
				Note	Min	Min	Min	Min	Min	Min	
W1	t_{PHWL} / t_{PHEL}	RP# High Recovery to WE# (CE#) Going Low		4,5	150	150	150	150	150	150	ns
W2	t_{ELWL} / t_{WLEL}	CE# (WE#) Setup to WE# (CE#) Going Low		4,5	0	0	0	0	0	0	ns
W3	t_{WLWH} / t_{ELEH}	WE# (CE#) Pulse Width		1,4,5	45	50	50	60	70	70	ns
W4	t_{DVWH} / t_{DVEH}	Data Setup to WE# (CE#) Going High		2,4,5	40	40	50	50	60	60	ns
W5	t_{AVWH} / t_{AVEH}	Address Setup to WE# (CE#) Going High		2,4,5	50	50	50	60	70	70	ns
W6	t_{WHEH} / t_{EHWH}	CE# (WE#) Hold Time from WE# (CE#) High		4,5	0	0	0	0	0	0	ns
W7	t_{WHDX} / t_{EHDX}	Data Hold Time from WE# (CE#) High		2,4,5	0	0	0	0	0	0	ns
W8	t_{WHAX} / t_{EHAX}	Address Hold Time from WE# (CE#) High		2,4,5	0	0	0	0	0	0	ns
W9	t_{WHWL} / t_{EHEL}	WE# (CE#) Pulse Width High		1,4,5	25	30	30	30	30	30	ns
W10	t_{VPWH} / t_{VPEH}	V_{PP} Setup to WE# (CE#) Going High		3,4,5	200	200	200	200	200	200	ns
W11	t_{QVVL}	V_{PP} Hold from Valid SRD		3,4	0	0	0	0	0	0	ns
W12	t_{BHWH} / t_{BHEH}	WP# Setup to WE# (CE#) Going High		3,4	0	0	0	0	0	0	ns
W13	t_{QVBL}	WP# Hold from Valid SRD		3,4	0	0	0	0	0	0	ns
W14	t_{WHGL}	WE# High to OE# Going Low		3,4	30	30	30	30	30	30	ns

NOTES:
1. Write pulse width (t_{WP}) is defined from CE# or WE# going low (whichever goes low last) to CE# or WE# going high (whichever goes high first). Hence, $t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$. Similarly, write pulse width high (t_{WPH}) is defined from CE# or WE# going high (whichever goes high first) to CE# or WE# going low (whichever goes low last). Hence, $t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$.
2. Refer to Table 25, "Bus Operations[1]" on page 52 for valid A_{IN} or D_{IN}.
3. Sampled, but not 100% tested.
4. See Figure 12, "AC Input/Output Reference Waveform" on page 47 for timing measurements and maximum allowable input slew rate.
5. See Figure 11, "Write Operations Waveform" on page 46.

Table 19. Write Operations—32-Mbit Density

#	Sym	Parameter	Density	32 Mbit						Unit
			Product	70 ns	90 ns	100 ns		110 ns		
			V_{CC} 3.0 V – 3.6 V[6]			90		100		
			V_{CC} 2.7 V – 3.6 V	70	90		100		110	
			Note	Min	Min	Min	Min	Min	Min	
W1	t_{PHWL} / t_{PHEL}	RP# High Recovery to WE# (CE#) Going Low	4,5	150	150	150	150	150	150	ns
W2	t_{ELWL} / t_{WLEL}	CE# (WE#) Setup to WE# (CE#) Going Low	4,5	0	0	0	0	0	0	ns
W3	t_{WLWH} / t_{ELEH}	WE# (CE#) Pulse Width	1,4,5	45	60	60	70	70	70	ns
W4	t_{DVWH}/ t_{DVEH}	Data Setup to WE# (CE#) Going High	2,4,5	40	40	50	60	60	60	ns
W5	t_{AVWH} / t_{AVEH}	Address Setup to WE# (CE#) Going High	2,4,5	50	60	60	70	70	70	ns
W6	t_{WHEH}/ t_{EHWH}	CE# (WE#) Hold Time from WE# (CE#) High	4,5	0	0	0	0	0	0	ns
W7	t_{WHDX}/ t_{EHDX}	Data Hold Time from WE# (CE#) High	2,4,5	0	0	0	0	0	0	ns
W8	t_{WHAX}/ t_{EHAX}	Address Hold Time from WE# (CE#) High	2,4,5	0	0	0	0	0	0	ns
W9	t_{WHWL} / t_{EHEL}	WE# (CE#) Pulse Width High	1,4,5	25	30	30	30	30	30	ns
W10	t_{VPWH} / t_{VPEH}	V_{PP} Setup to WE# (CE#) Going High	3,4,5	200	200	200	200	200	200	ns
W11	t_{QVVL}	V_{PP} Hold from Valid SRD	3,4	0	0	0	0	0	0	ns
W12	t_{BHWH}/ t_{BHEH}	WP# Setup to WE# (CE#) Going High	3,4	0	0	0	0	0	0	ns
W13	t_{QVBL}	WP# Hold from Valid SRD	3,4	0	0	0	0	0	0	ns
W14	t_{WHGL}	WE# High to OE# Going Low	3,4	30	30	30	30	30	30	ns

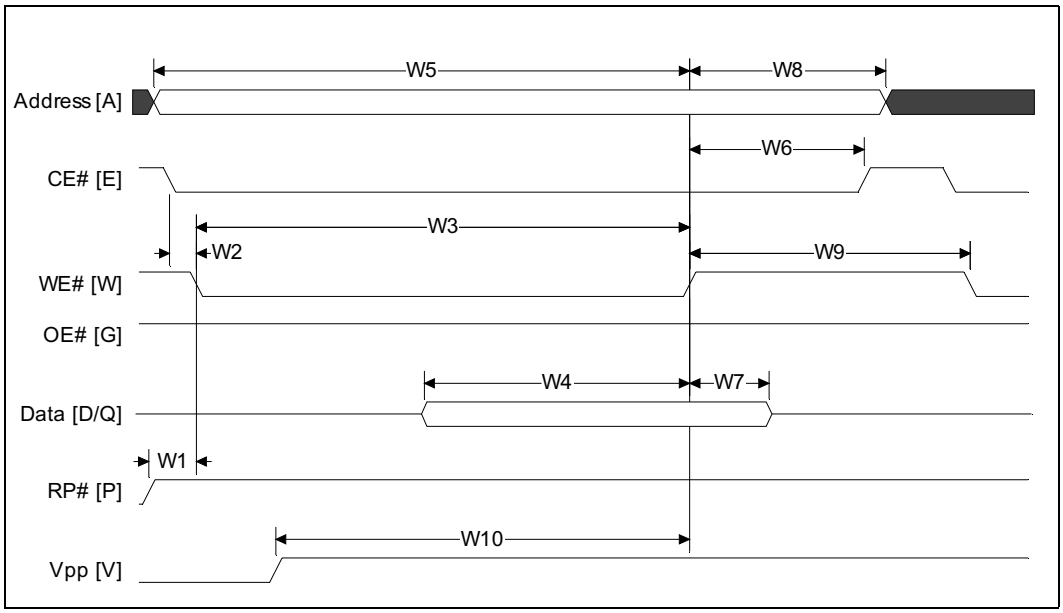
NOTES:
1. Write pulse width (t_{WP}) is defined from CE# or WE# going low (whichever goes low last) to CE# or WE# going high (whichever goes high first). Hence, $t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$. Similarly, write pulse width high (t_{WPH}) is defined from CE# or WE# going high (whichever goes high first) to CE# or WE# going low (whichever goes low last). Hence, $t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$.
2. Refer to Table 25, "Bus Operations[1]" on page 52 for valid A_{IN} or D_{IN}.
3. Sampled, but not 100% tested.
4. See Figure 12, "AC Input/Output Reference Waveform" on page 47 for timing measurements and maximum allowable input slew rate.
5. See Figure 11, "Write Operations Waveform" on page 46.
6. V_{CC}Max = 3.3 V for 32-Mbit 0.25 Micron product.

Table 20. Write Operations—64-Mbit Density

#	Symbol	Parameter	Density			64 Mbit	Unit
			Product			80 ns	
			V_{CC}	2.7 V – 3.6 V	Note	Min	
W1	t_{PHWL} / t_{PHEL}	RP# High Recovery to WE# (CE#) Going Low			4,5	150	ns
W2	t_{ELWL} / t_{WLEL}	CE# (WE#) Setup to WE# (CE#) Going Low			4,5	0	ns
W3	t_{WLWH} / t_{ELEH}	WE# (CE#) Pulse Width			1,4,5	60	ns
W4	t_{DVWH} / t_{DVEH}	Data Setup to WE# (CE#) Going High			2,4,5	40	ns
W5	t_{AVWH} / t_{AVEH}	Address Setup to WE# (CE#) Going High			2,4,5	60	ns
W6	t_{WHEH} / t_{EHWH}	CE# (WE#) Hold Time from WE# (CE#) High			4,5	0	ns
W7	t_{WHDX} / t_{EHDX}	Data Hold Time from WE# (CE#) High			2,4,5	0	ns
W8	t_{WHAX} / t_{EHAX}	Address Hold Time from WE# (CE#) High			2,4,5	0	ns
W9	t_{WHWL} / t_{EHEL}	WE# (CE#) Pulse Width High			1,4,5	30	ns
W10	t_{VPWH} / t_{VPEH}	V_{PP} Setup to WE# (CE#) Going High			3,4,5	200	ns
W11	t_{QVVL}	V_{PP} Hold from Valid SRD			3,4	0	ns
W12	t_{BHWH} / t_{BHEH}	WP# Setup to WE# (CE#) Going High			3,4	0	ns
W13	t_{QVBL}	WP# Hold from Valid SRD			3,4	0	ns
W14	t_{WHGL}	WE# High to OE# Going Low			3,4	30	ns

NOTES:
1. Write pulse width (t_{WP}) is defined from CE# or WE# going low (whichever goes low last) to CE# or WE# going high (whichever goes high first). Hence, $t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$. Similarly, write pulse width high (t_{WPH}) is defined from CE# or WE# going high (whichever goes high first) to CE# or WE# going low (whichever goes low last). Hence, $t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$.
2. Refer to Table 25, "Bus Operations[1]" on page 52 for valid A_{IN} or D_{IN}.
3. Sampled, but not 100% tested.
4. See Figure 12, "AC Input/Output Reference Waveform" on page 47 for timing measurements and maximum allowable input slew rate.
5. See Figure 11, "Write Operations Waveform" on page 46.

Figure 11. Write Operations Waveform



8.3 Erase and Program Timing

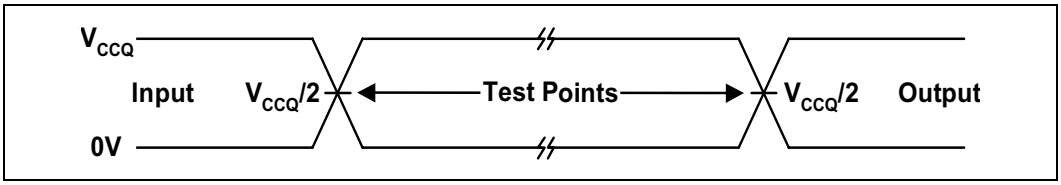
Table 21. Erase and Program Timing

Symbol	Parameter	V_{PP}	1.65 V–3.6 V		11.4 V–12.6 V		Unit
		Note	Typ	Max	Typ	Max	
t_{BWPB}	4-KW Parameter Block Word Program Time	1, 2, 3	0.10	0.30	0.03	0.12	s
t_{BWMB}	32-KW Main Block Word Program Time	1, 2, 3	0.8	2.4	0.24	1	s
t_{WHQV1} / t_{EHQV1}	Word Program Time for 0.13 and 0.18 Micron Product	1, 2, 3	12	200	8	185	µs
	Word Program Time for 0.25 Micron Product	1, 2, 3	22	200	8	185	µs
t_{WHQV2} / t_{EHQV2}	4-KW Parameter Block Erase Time	1, 2, 3	0.5	4	0.4	4	s
t_{WHQV3} / t_{EHQV3}	32-KW Main Block Erase Time	1, 2, 3	1	5	0.6	5	s
t_{WHRH1} / t_{EHRH1}	Program Suspend Latency	1,3	5	10	5	10	µs
t_{WHRH2} / t_{EHRH2}	Erase Suspend Latency	1,3	5	20	5	20	µs

NOTES:
1. Typical values measured at T_A= +25 °C and nominal voltages.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.

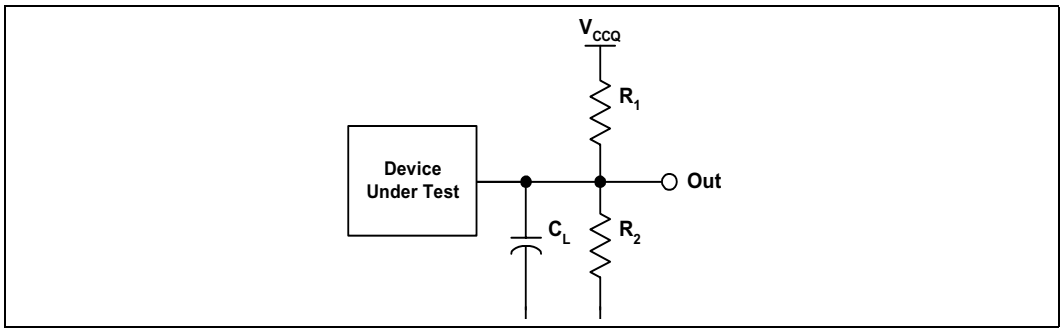
8.4 AC I/O Test Conditions

Figure 12. AC Input/Output Reference Waveform



NOTE: Input timing begins, and output timing ends, at V_{CCQ}/2. Input rise and fall times (10% to 90%) < 5 ns. Worst-case speed conditions are when V_{CC} = V_{CC}Min.

Figure 13. Transient Equivalent Testing Load Circuit



NOTE: See Table 22 for component values.

Table 22. Test Configuration Component Values for Worst Case Speed Conditions

Test Configuration	C_L (pF)	R_1 (kΩ)	R_2 (kΩ)
V_{CCQ}Min Standard Test	50	25	25

NOTE: C_L includes jig capacitance.

8.5 Device Capacitance

T_A = 25 °C, f = 1 MHz

Table 23. Device Capacitance

Symbol	Parameter[§]	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	6	8	pF	V_{IN} = 0.0 V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0.0 V

[§]Sampled, not 100% tested.

9.0 Power and Reset Specifications

9.1 Power-Up/Down Characteristics

To prevent any condition that may result in a spurious write or erase operation, Intel recommends that you power-up V_{CC} and V_{CCQ} together. Conversely, V_{CC} and V_{CCQ} must power-down together. Intel also recommends power-up V_{PP} with or slightly after V_{CC}. Conversely, V_{PP} must powerdown with or slightly before V_{CC}.

If V_{CCQ} and/or VPP are not connected to the V_{CC} supply, then V_{CC} must attain V_{CC}Min before applying VCCQ and VPP. Device inputs must not be driven before supply voltage = VCCMin. Power supply transitions must only occur when RP# is low.

9.1.1 RP# Connected to System Reset

The use of RP# during system reset is important with automated program/erase devices because the system expects to read from the flash memory when it exits reset. If a CPU reset occurs without a flash memory reset, proper CPU initialization will not occur because the flash memory may be providing status information instead of array data. Intel recommends connecting RP# to the system CPU RESET# signal to allow proper CPU/flash initialization following system reset.

System designers must guard against spurious writes when V_{CC} voltages are above V_{LKO}. Because both WE# and CE# must be low for a command write, driving either signal to V_{IH} will inhibit writes to the device. The CUI architecture provides additional protection since alteration of memory contents can occur only after successful completion of the two-step command sequences. The device is also disabled until RP# is brought to V_{IH}, regardless of the state of its control inputs. By holding the device in reset (RP# connected to system POWERGOOD) during power-up/down, invalid bus conditions during power-up can be masked, providing yet another level of memory protection.

9.1.2 V_{CC}, V_{PP}, and RP# Transitions

The CUI latches commands as issued by system software and is not altered by V_{PP} or CE# transitions or WSM actions. Its default state upon power-up, after exit from reset mode or after V_{CC} transitions above V_{LKO} (Lockout voltage), is read-array mode.

After any program or Block-Erase operation is complete (even after V_{PP} transitions down to V_{PPLK}), the CUI must be reset to read-array mode through the Read Array command if access to the flash-memory array is required.

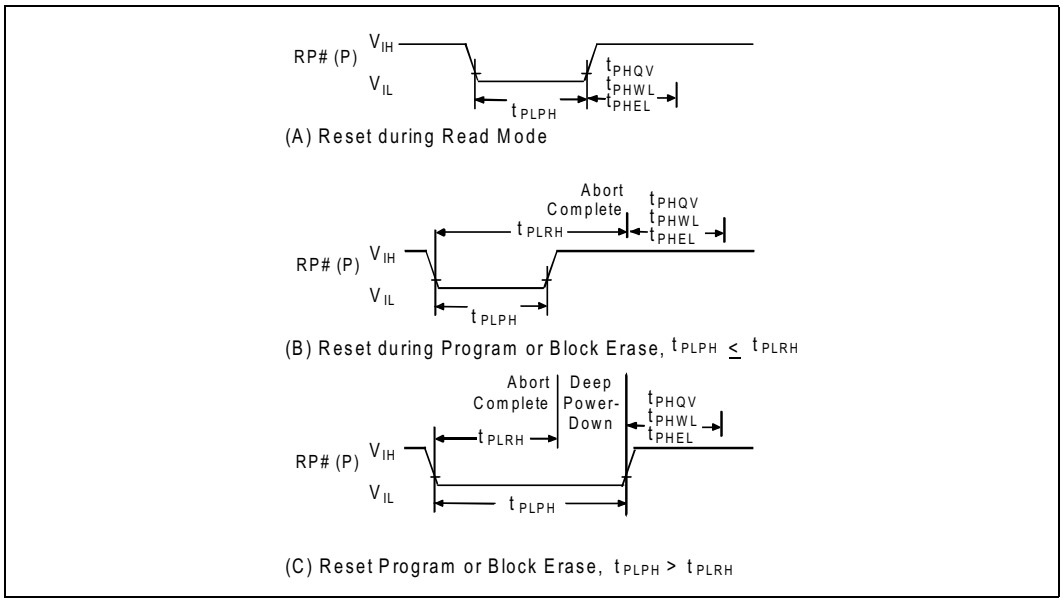
9.2 Reset Specifications

Table 24. Reset Specifications

Symbol	Parameter	V_{CC} 2.7 V – 3.6 V		Unit	Notes
		Min	Max		
t_{PLPH}	RP# Low to Reset during Read (If RP# is tied to V_{CC}, this specification is not applicable)	100		ns	1, 2
t_{PLRH1}	RP# Low to Reset during Block Erase		22	µs	3
t_{PLRH2}	RP# Low to Reset during Program		12	µs	3

NOTES:
1. If t_{PLPH} is < 100 ns the device can still reset but this is not guaranteed.
2. If RP# is asserted while a Block Erase or Word Program operation is not executing, the reset will complete within 100 ns.
3. Sampled, but not 100% tested.

Figure 14. Deep Power-Down/Reset Operations Waveforms



9.3 Power Supply Decoupling

Flash memory power-switching characteristics require careful device decoupling. System designers must consider the following three supply current issues:

1. Standby current levels (I_{CCS})
2. Read current levels (I_{CCR})
3. Transient peaks produced by falling and rising edges of CE#.

Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress these transient voltage peaks. Each flash device must have a 0.1 µF ceramic capacitor connected between each V_{CC} and GND, and between its V_{PP} and GND. These high-frequency, inherently low-inductance capacitors must be placed as close as possible to the package leads.

9.4 Power Consumption

Intel flash devices have a tiered approach to power savings that can significantly reduce overall system power consumption. The Automatic Power Savings (APS) feature reduces power consumption when the device is selected but idle. If the CE# is deasserted, the flash enters its standby mode, where current consumption is even lower. The combination of these features can minimize memory power consumption, and therefore, overall system power consumption.

9.4.1 Active Power

With CE# at a logic-low level and RP# at a logic-high level, the device is in the active mode. Refer to the DC Characteristic tables for I_{CC} current values. Active power is the largest contributor to overall system power consumption. Minimizing the active current could have a profound effect on system power consumption, especially for battery-operated devices.

9.4.2 Automatic Power Savings (APS)

Automatic Power Savings provides low-power operation during read mode. After data is read from the memory array and the address lines are quiescent, APS circuitry places the device in a mode where typical current is comparable to I_{CCS}. The flash stays in this static state with outputs valid until a new location is read.

9.4.3 Standby Power

With CE# at a logic-high level (V_{IH}) and the device in read mode, the flash memory is in standby mode, which disables much of the device circuitry, and substantially reduces power consumption. Outputs are placed in a high-impedance state independent of the status of the OE# signal. If CE# transitions to a logic-high level during Erase or Program operations, the device continues to perform the operation and consume corresponding active power until the operation is completed.

System engineers must analyze the breakdown of standby time versus active time and quantify the respective power consumption in each mode for their specific application. This approach provides a more accurate measure of application-specific power and energy requirements.

9.4.4 Deep Power-Down Mode

The deep power-down mode is activated when RP# = V_{IL} (GND ± 0.2 V). During read modes, RP# going low de-selects the memory and places the outputs in a high-impedance state. Recovery from deep power-down requires a minimum time of t_{PHQV} (See "AC Read Characteristics" on page 38.)

During program or erase modes, RP# transitioning low aborts the in-progress operation. The memory contents of the address being programmed or the block being erased are no longer valid as the data integrity has been compromised by the abort. During deep power-down, all internal circuits are switched to a low-power savings mode (RP# transitioning to V_{IL} or turning off power to the device clears the Status Register).

10.0 Operations Overview

Flash memory combines EEPROM functionality with in-circuit electrical program-and-erase capability. The B3 flash memory device family utilizes a Command User Interface (CUI) and automated algorithms to simplify Program and Erase operations. The CUI allows for 100% CMOS-level control inputs and fixed power supplies during erasure and programming.

When $V_{PP} < V_{PPLK}$, the device will execute only the following commands successfully: Read Array, Read Status Register, Clear Status Register, and Read Identifier. The device provides standard EEPROM read, standby, and Output-Disable operations. Manufacturer identification and device identification data can be accessed through the CUI. All functions associated with altering memory contents, namely program and erase, are accessible through the CUI. The internal Write State Machine (WSM) completely automates Program and Erase operations, while the CUI signals the start of an operation and the Status Register reports status. The CUI handles the WE# interface to the data and address latches, as well as system status requests during WSM operation.

10.1 Bus Operations

The B3 flash memory device performs read, program, and erase in-system through the local CPU or microcontroller. All bus cycles to or from the flash memory conform to standard microcontroller bus cycles. Four control pins dictate the data flow in and out of the flash component: CE#, OE#, WE#, and RP#. Table 25 summarizes these bus operations.

Table 25. Bus Operations(1)

Mode	Note	RP#	CE#	OE#	WE#	DQ_{0-7}	DQ_{8-15}
Read (Array, Status, or Identifier)	2–4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	D_{OUT}
Output Disable	2	V_{IH}	V_{IL}	V_{IH}	V_{IH}	High Z	High Z
Standby	2	V_{IH}	V_{IH}	X	X	High Z	High Z
Reset	2, 7	V_{IL}	X	X	X	High Z	High Z
Write	2, 5–7	V_{IH}	V_{IL}	V_{IH}	V_{IL}	D_{IN}	D_{IN}

NOTES:
1. 8-bit devices use only DQ[0:7], 16-bit devices use DQ[0:15].
2. X must be V_{IL}, V_{IH} for control pins and addresses.
3. See *DC Characteristics* for V_{PPLK}, V_{PP1}, V_{PP2}, V_{PP3}, V_{PP4} voltages.
4. Manufacturer and device codes can also be accessed in read identifier mode (A_1–A_{21} = 0). See Table 27.
5. Refer to Table 28 for valid D_{IN} during a Write operation.
6. To program or erase the lockable blocks, hold WP# at V_{IH}.
7. RP# must be at GND ± 0.2 V to meet the maximum deep power-down current specified.

10.1.1 Read

The flash memory has four read modes available: read array, read identifier, read status, and read query. These modes are accessible independent of the V_{PP} voltage. The appropriate Read Mode command must be issued to the CUI to enter the corresponding mode. Upon initial device power-up or after exit from reset, the device automatically defaults to read-array mode.

CE# and OE# must be driven active to obtain data at the outputs. CE# is the device selection control; when active, it enables the flash memory device. OE# is the data output control, and it drives the selected memory data onto the I/O bus. For all read modes, WE# and RP# must be at V_{IH}. Figure 10 illustrates a read cycle.

10.1.2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins are placed in a high-impedance state.

10.1.3 Standby

Deselecting the device by bringing CE# to a logic-high level (V_{IH}) places the device in standby mode, which substantially reduces device power consumption without any latency for subsequent read accesses. In standby, outputs are placed in a high-impedance state independent of OE#. If deselected during Program or Erase operation, the device continues to consume active power until the Program or Erase operation is complete.

10.1.4 Deep Power-Down / Reset

From read mode, RP# at V_{IL} for time t_{PLPH} deselects the memory, places output drivers in a high-impedance state, and turns off all internal circuits. After return from reset, a time t_{PHQV} is required until the initial read-access outputs are valid. A delay (t_{PHWL} or t_{PHEL}) is required after return from reset before a write can be initiated. After this wake-up interval, normal operation is restored. The CUI resets to read-array mode, and the Status Register is set to 80H. Figure 14, “Deep Power-Down/Reset Operations Waveforms” on page 50 (A) illustrates this case.

If RP# is taken low for time t_{PLPH} during a Program or Erase operation, the operation will be aborted and the memory contents at the aborted location (for a program) or block (for an erase) are no longer valid, since the data may be partially erased or written. The abort process goes through the following sequence:

1. When RP# goes low, the device shuts down the operation in progress, a process that takes time t_{PLRH} to complete.
2. After this time t_{PLRH}, the part will either reset to read-array mode (if RP# has gone high during t_{PLRH}, see Figure 14, “Deep Power-Down/Reset Operations Waveforms” on page 50 (B)), or enter reset mode (if RP# is still logic low after t_{PLRH}, see Figure 14, “Deep Power-Down/Reset Operations Waveforms” on page 50 (C)).
3. In both cases, after returning from an aborted operation, the relevant time t_{PHQV} or t_{PHWL}/t_{PHEL} must be waited before a Read or Write operation is initiated, as discussed in the previous paragraph. However, in this case, these delays are referenced to the end of t_{PLRH} rather than when RP# goes high.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, the processor expects to read from the flash memory. Automated flash memories provide status information when read during program or Block-Erase operations. If a CPU reset occurs with no flash memory reset, proper CPU initialization can not occur because the flash memory may be providing status information instead of array data. Intel® Flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

10.1.5 Write

A write occurs when both CE# and WE# are low and OE# is high. Commands are written to the Command User Interface (CUI) using standard microprocessor write timings to control Flash operations. The CUI does not occupy an addressable memory location. The address and data buses

are latched on the rising edge of the second WE# or CE# pulse, whichever occurs first. Table 28 shows the available commands, and Appendix A provides detailed information on moving between the different modes of operation using CUI commands.

Two commands modify array data: Program (40H), and Erase (20H). Writing either of these commands to the internal Command User Interface (CUI) initiates a sequence of internally timed functions that culminate in the completion of the requested task (unless that operation is aborted by either RP# being driven to V_{IL} for t_{PLRH} or an appropriate Suspend command).

11.0 Modes of Operation

The flash memory has four read modes (read array, read identifier, read status, and read query; see Figure 1, "B3 Architecture Block Diagram" on page 10), and two write modes (program and block erase). Three additional modes (erase suspend to program, erase suspend to read, and program suspend to read) are available only during suspended operations. Table 26, "Command Codes and Descriptions" on page 55 summarizes the commands used to reach these modes. Appendix A, "Write State Machine Current/Next States," is a comprehensive chart showing the state transitions.

11.1 Read Array

When RP# transitions from V_{IL} (reset) to V_{IH}, the device defaults to read-array mode and will respond to the read-control inputs (CE#, address inputs, and OE#) without any additional CUI commands.

When the device is in read-array mode, four control signals control data output.

- WE# must be logic high (V_{IH})
- CE# must be logic low (V_{IL})
- OE# must be logic low (V_{IL})
- RP# must be logic high (V_{IH})

In addition, the address of the preferred location must be applied to the address pins. If the device is not in read-array mode, as would be the case after a Program or Erase operation, the Read Array command (FFH) must be written to the CUI before array reads can occur.

Table 26. Command Codes and Descriptions (Sheet 1 of 2)

Code	Device Mode	Description
00, 01, 60, 2F, C0, 98	Invalid/ Reserved	Unassigned commands that must not be used. Intel reserves the right to redefine these codes for future functions.
FF	Read Array	Places the device in read-array mode, such that array data will be output on the data pins.
40	Program Set-Up	This is a two-cycle command. The first cycle prepares the CUI for a program operation. The second cycle latches addresses and data information and initiates the WSM to execute the program algorithm. The flash outputs Status Register data when CE# or OE# is toggled. A Read Array command is required after programming to read array data. See Section 11.4.
10	Alternate Program Set-Up	(See 40H/Program Set-Up)
20	Erase Set-Up	Prepares the CUI for the Erase Confirm command. If the next command is not an Erase Confirm command, then the CUI will (a) set both SR.4 and SR.5 of the Status Register to a "1," (b) place the device into the read-Status Register mode, and (c) wait for another command. See Section 11.5, "Erase Mode" on page 58.
D0	Erase Confirm	If the previous command was an Erase Set-Up command, then the CUI will close the address and data latches, and begin erasing the block indicated on the address pins. During erase, the device will only respond to the Read Status Register and Erase Suspend commands. The device will output Status Register data when CE# or OE# is toggled.
	Program / Erase Resume	If a Program or Erase operation was previously suspended, this command will resume that operation.

Table 26. Command Codes and Descriptions (Sheet 2 of 2)

Code	Device Mode	Description
B0	Program / Erase Suspend	Issuing this command will begin to suspend the currently executing Program/Erase operation. The Status Register will indicate when the operation has been successfully suspended by setting either the program suspend (SR.2) or erase suspend (SR.6), and the WSM status bit (SR.7) to a "1" (ready). The WSM will continue to idle in the SUSPEND state, regardless of the state of all input-control pins except RP#, which will immediately shut down the WSM and the remainder of the chip, if it is driven to V_{IL}. See Section 11.4.1, "Suspending and Resuming Program" on page 58 and Section 11.4.1, "Suspending and Resuming Program" on page 58.
70	Read Status Register	This command places the device into Read-Status Register mode. Reading the device will output the contents of the Status Register, regardless of the address presented to the device. The device automatically enters this mode after a Program or Erase operation has been initiated. See Section 11.3, "Read Status Register" on page 57.
50	Clear Status Register	The WSM can set the block-lock status (SR.1), V_{PP} status (SR.3), program status (SR.4), and erase status (SR.5) bits in the Status Register to "1," but it cannot clear them to "0." Issuing this command clears those bits to "0."
90	Read Identifier	Puts the device into the intelligent-identifier-read mode, so that reading the device will output the manufacturer and device codes (A_0 = 0 for manufacturer, A_0 = 1 for device, all other address inputs must be 0). See Section Section 11.2, "Read Identifier" on page 56.

NOTE: See Chapter 14.0, "Write State Machine Current/Next States," for mode transition information.

11.2 Read Identifier

To read the manufacturer and device codes, the device must be in read-identifier mode, which can be reached by writing the Read Identifier command (90H). Once in read-identifier mode, A_0 = 0 outputs the manufacturer's identification code, and A_0 = 1 outputs the device identifier (see Table 27) Note: A_1–A_{21} = 0. To return to read-array mode, write the Read-Array command (FFH).

Table 27. Read Identifier Table

Size	Mfr. ID	Device Identifier	
		-T (Top Boot)	-B (Bottom Boot)
28F004B3	0089H	D4H	D5H
28F400B3		8894H	8895H
28F008B3	0089H	D2H	D3H
28F800B3		8892H	8893H
28F016B3		D0H	D1H
28F160B3	0089H	8890H	8891H
28F320B3		8896H	8897H
28F640B3		8898H	8899H

11.3 Read Status Register

The device Status Register indicates when a Program or Erase operation is complete, and the success or failure of that operation. To read the Status Register, issue the Read Status Register (70H) command to the CUI. This causes all subsequent Read operations to output data from the Status Register until another command is written to the CUI. To return to reading from the array, issue the Read Array (FFH) command.

The Status Register bits are output on DQ_0–DQ_7. The upper byte, DQ_8–DQ_{15}, outputs 00H during a Read Status Register command.

The contents of the Status Register are latched on the falling edge of OE# or CE#, which prevents possible Bus errors that might occur if Status Register contents change while being read. CE# or OE# must be toggled with each subsequent status read, or the Status Register will not indicate completion of a Program or Erase operation.

When the WSM is active, SR.7 will indicate the status of the WSM; the remaining bits in the Status Register indicate whether or not the WSM was successful in performing the preferred operation (see Table 29 on page 60).

11.3.1 Clearing the Status Register

The WSM sets status bits 1 through 7 to "1," and clears bits 2, 6, and 7 to "0," but cannot clear status bits 1 or 3 through 5 to "0." Because bits 1, 3, 4, and 5 indicate various error conditions, these bits can be cleared only through the Clear Status Register (50H) command. By allowing the system software to control the resetting of these bits, several operations can be performed (such as cumulatively programming several addresses or erasing multiple blocks in sequence) before reading the Status Register to determine if an error occurred during that series. Clear the Status Register before beginning another command or sequence.

Note: The Read Array command must be issued before data can be read from the memory array.

11.4 Program Mode

Programming is executed using a two-write sequence. The Program Setup command (40H) is written to the CUI followed by a second write that specifies the address and data to be programmed. The WSM will execute a sequence of internally timed events to program preferred bits of the addressed location, then verify the bits are sufficiently programmed. Programming the memory results in specific bits within an address location being changed to a "0." If users attempt to program "1"s, the memory cell contents do not change and no error occurs.

The Status Register indicates programming status: while the program sequence executes, status bit 7 is "0." The Status Register can be polled by toggling either CE# or OE#. While programming, the only valid commands are Read Status Register, Program Suspend, and Program Resume.

When programming is complete, the program-status bits must be checked. If the programming operation was unsuccessful, SR.4 is set to indicate a program failure. If SR.3 is set, then V_{PP} was not within acceptable limits, and the WSM did not execute the program command. If SR.1 is set, a program operation was attempted on a locked block and the operation was aborted.

The Status Register must be cleared before attempting the next operation. Any CUI instruction can follow after programming is completed; however, to prevent inadvertent Status Register reads, be sure to reset the CUI to read-array mode.

11.4.1 Suspending and Resuming Program

The Program Suspend halts the in-progress program operation to read data from another location of memory. Once the programming process starts, writing the Program Suspend command to the CUI requests that the WSM suspend the program sequence (at predetermined points in the program algorithm). The device continues to output Status Register data after the Program Suspend command is written. Polling SR.7 and SR.2 will determine when the program operation has been suspended (both will be set to "1"). t_{WHRH1}/t_{EHRH1} specify the program- suspend latency.

A Read Array command can now be written to the CUI to read data from blocks other than that which is suspended. The only other valid commands while program is suspended are Read Status Register, Read Identifier, and Program Resume. After the Program Resume command is written to the flash memory, the WSM will continue with the program process and Status Register bits SR.2 and SR.7 will automatically be cleared. After the Program Resume command is written, the device automatically outputs Status Register data when read. See Appendix B, "Program and Erase Flowcharts." V_{PP} must remain at the same V_{PP} level used for program while in program- suspend mode. RP# must also remain at V_{IH}.

11.5 Erase Mode

To erase a block, write the Erase Set-up and Erase Confirm commands to the CUI, along with an address identifying the block to be erased. This address is latched internally when the Erase Confirm command is issued. Block erasure results in all bits within the block being set to "1." Only one block can be erased at a time. The WSM will execute a sequence of internally timed events to program all bits within the block to "0," erase all bits within the block to "1," then verify that all bits within the block are sufficiently erased. While the erase executes, status bit 7 is a "0."

When the Status Register indicates that erasure is complete, check the erase-status bit to verify that the Erase operation was successful. If the Erase operation was unsuccessful, SR.5 of the Status Register will be set to a "1," indicating an erase failure. If V_{PP} was not within acceptable limits after the Erase Confirm command was issued, the WSM will not execute the erase sequence; instead, SR.5 is set to indicate an Erase error, and SR.3 is set to a "1" to identify that V_{PP} supply voltage was not within acceptable limits.

After an Erase operation, clear the Status Register (50H) before attempting the next operation. Any CUI instruction can follow after erasure is completed; however, to prevent inadvertent status-register reads, it is advisable to place the flash in read-array mode after the erase is complete.

11.5.1 Suspending and Resuming Erase

Since an Erase operation requires on the order of seconds to complete, an Erase Suspend command is provided to allow erase-sequence interruption in order to read data from—or program data to—another block in memory. Once the erase sequence is started, writing the Erase Suspend command to the CUI requests that the WSM pause the erase sequence at a predetermined point in the erase algorithm. The Status Register will indicate if/when the Erase operation has been suspended.

A Read Array/Program command can now be written to the CUI in order to read data from/ program data to blocks other than the one currently suspended. The Program command can subsequently be suspended to read yet another array location. The only valid commands while Erase is suspended are Erase Resume, Program, Read Array, Read Status Register, or Read Identifier. During erase-suspend mode, the chip can be placed in a pseudo-standby mode by taking CE# to V_{IH}, which reduces active current consumption.

Erase Resume continues the erase sequence when CE# = V_{IL}. As with the end of a standard Erase operation, the Status Register must be read and cleared before the next instruction is issued.

Table 28. Command Bus Definitions (1,4)

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Array		Write	X	FFH			
Read Identifier	2	Write	X	90H	Read	IA	ID
Read Status Register		Write	X	70H	Read	X	SRD
Clear Status Register		Write	X	50H			
Program	3	Write	X	40H / 10H	Write	PA	PD
Block Erase/Confirm		Write	X	20H	Write	BA	D0H
Program/Erase Suspend		Write	X	B0H			
Program/Erase Resume		Write	X	D0H			

NOTES:

PA: Program Address **PD:** Program Data **BA:** Block Address
IA: Identifier Address **ID:** Identifier Data **SRD:** Status Register Data

1. Bus operations are defined in Table 25.
2. Following the Intelligent Identifier command, two Read operations access manufacturer and device codes. A_0 = 0 for manufacturer code, A_0 = 1 for device code. A_1–A_{21} = 0.
3. Either 40H or 10H command is valid although the standard is 40H.
4. When writing commands to the device, the upper data bus [DQ_8–DQ_{15}] must be either V_{IL} or V_{IH}, to minimize current draw.

Table 29. Status Register Bit Definition

WSMS	ESS	ES	PS	VPPS	PSS	BLS	R
7	6	5	4	3	2	1	0

	NOTES:
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Check Write State Machine bit first to determine word program or block-erase completion, before checking program or erase-status bits.
SR.6 = ERASE-SUSPEND STATUS (ESS) 1 = Erase Suspended 0 = Erase In Progress/Completed	When erase suspend is issued, WSM halts execution and sets both WSMS and ESS bits to “1.” ESS bit remains set at “1” until an Erase Resume command is issued.
SR.5 = ERASE STATUS (ES) 1 = Error In Block Erasure 0 = Successful Block Erase	When this bit is set to “1,” WSM has applied the max. number of erase pulses to the block and is still unable to verify successful block erasure.
SR.4 = PROGRAM STATUS (PS) 1 = Error in Word Program 0 = Successful Word Program	When this bit is set to “1,” WSM has attempted but failed to program a word.
SR.3 = V_{PP} STATUS (VPPS) 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK	The V_{PP} status bit does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP} level only after the Program or Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. The V_{PP} is also checked before the operation is verified by the WSM. The V_{PP} status bit is not guaranteed to report accurate feedback between V_{PPLK} max and V_{PP1} min or between V_{PP1} max and V_{PP4} min.
SR.2 = PROGRAM SUSPEND STATUS (PSS) 1 = Program Suspended 0 = Program in Progress/Completed	When program suspend is issued, WSM halts execution and sets both WSMS and PSS bits to “1.” PSS bit remains set to “1” until a Program Resume command is issued.
SR.1 = BLOCK LOCK STATUS 1 = Program/Erase attempted on locked block; Operation aborted 0 = No operation to locked blocks	If a Program or Erase operation is attempted to one of the locked blocks, this bit is set by the WSM. The operation specified is aborted and the device is returned to read status mode.
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	This bit is reserved for future use and must be masked out when polling the Status Register.

NOTE: A Command Sequence Error is indicated when SR.4, SR.5, and SR.7 are set.

12.0 Block Locking

The B3 flash memory device architecture features two hardware-lockable parameter blocks.

12.1 WP# = V_{IL} for Block Locking

The lockable blocks are locked when WP# = V_{IL}; any program or Erase operation to a locked block will result in an error, which will be reflected in the Status Register:

- For top configuration, the top two parameter blocks (blocks #133 and #134 for the 64 Mbit, #69 and #70 for the 32 Mbit, blocks #37 and #38 for the 16 Mbit, blocks #21 and #22 for the 8 Mbit, blocks #13 and #14 for the 4 Mbit) are lockable.

- For the bottom configuration, the bottom two parameter blocks (blocks #0 and #1 for 4 /8 /16 / 32/64 Mbit) are lockable. Unlocked blocks can be programmed or erased normally (unless V_{PP} is below V_{PPLK}).

12.2 WP# = V_{IH} for Block Unlocking

WP# = V_{IH} unlocks all lockable blocks. These blocks can now be programmed or erased.

Note that RP# does not override WP# locking as in previous Boot Block devices. WP# controls all block locking and V_{PP} provides protection against spurious writes. Table 30 defines the write-protection methods.

Table 30. Write-Protection Truth Table for the B3 Device Family

V_{PP}	WP#	RP#	Write Protection Provided
X	X	V_{IL}	All Blocks Locked
V_{IL}	X	V_{IH}	All Blocks Locked
≥ V_{PPLK}	V_{IL}	V_{IH}	Lockable Blocks Locked
≥ V_{PPLK}	V_{IH}	V_{IH}	All Blocks Unlocked

13.0 V_{PP} Program and Erase Voltages

TheB3 flash memory device products provide in-system programming and erase at 2.7 V. For customers requiring fast programming in their manufacturing environment, B3 flash memory device includes an additional low-cost 12-V programming feature.

The 12-V V_{PP} mode enhances programming performance during the short period of time typically found in manufacturing processes; however, it is not intended for extended use. 12 V can be applied to V_{PP} during program and Erase operations for a maximum of 1000 cycles on the main blocks, and 2500 cycles on the parameter blocks. V_{PP} can be connected to 12 V for a total of 80 hours maximum.

Warning: Stressing the device beyond these limits may cause permanent damage.

During Read operations or idle times, V_{PP} can be tied to a 5-V supply. For Program and Erase operations, a 5-V supply is not permitted. The V_{PP} must be supplied with either 2.7 V to 3.6 V or 11.4 V to 12.6 V during Program and Erase operations.

13.1 $V_{PP} = V_{IL}$ for Complete Protection

The V_{PP} programming voltage can be held low for complete write protection of all blocks in the flash device. When V_{PP} is below V_{PPLK}, any Program or Erase operation will result in a error, prompting the corresponding SR.3 to be set.

14.0 Additional Information

Order Number	Document/Tool
297948	*Intel® Advanced Boot Block Flash Memory Family Specification Update*
292199	*AP-641 Achieving Low Power with the 3 Volt Advanced Boot Block Flash Memory*
292200	*AP-642 Designing for Upgrade to the 3 Volt Advanced Boot Block Flash Memory*
Note 2	*3 Volt Advanced Boot Block Algorithms ('C' and assembly)* http://developer.intel.com/design/flash/swtools
Contact your Intel Representative	*Intel® Flash Data Integrator (IFDI) Software Developer's Kit*
297874	*IFDI Interactive: Play with Intel® Flash Data Integrator on Your PC*

NOTES:
1. Call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers must contact their local Intel or distribution sales office.
2. Visit the Intel home page at http://www.Intel.com or http://developer.intel.com for technical documentation and tools.
3. For the most current information on Intel® Advanced Boot Block Flash memory and Intel® Advanced+ Boot Block Flash memory, visit http://developer.intel.com/design/flash/

Appendix A Write State Machine Current/Next States

Current State	SR.7	Data When Read	Command Input (and Next State)								
			Read Array (FFH)	Program Setup (10/ 40H)	Erase Setup (20H)	Erase Confirm (D0H)	Prog/Ers Suspend (B0H)	Prog/Ers Resume (D0H)	Read Status (70H)	Clear Status (50H)	Read Identifier. (90H)
Read Array	"1"	Array	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Read Status	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Read Identifier	"1"	Identifier	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Prog. Setup	"1"	Status	Program (Command Input = Data to be Programmed)								
Program (continue)	"0"	Status	Program (continue)				Prog. Sysop. to Rd. Status	Program (continue)			
Program Suspend to Read Status	"1"	Status	Prog. Susp. to Read Array	Program Suspend to Read Array		Program (continue)	Program Susp. to Read Array	Program (continue)	Prog. Susp. to Read Status	Prog. Susp. to Read Array	Prog. Susp. to Read Identifier
Program Suspend to Read Array	"1"	Array	Prog. Susp. to Read Array	Program Suspend to Read Array		Program (continue)	Program Susp. to Read Array	Program (continue)	Prog. Susp. to Read Status	Prog. Sus. to Read Array	Prog. Susp. to Read Identifier
Prog. Susp. to Read Identifier	"1"	Identifier	Prog. Susp. to Read Array	Program Suspend to Read Array		Program (continue)	Program Susp. to Read Array	Program (continue)	Prog. Susp. to Read Status	Prog. Sus. to Read Array	Prog. Susp. to Read Identifier
Program (complete)	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Erase Setup	"1"	Status	Erase Command Error			Erase (continue)	Erase Cant. Error	Erase (continue)	Erase Command Error		
Erase Cant. Error	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Erase (continue)	"0"	Status	Erase (continue)				Erase Sus. to Read Status	Erase (continue)			
Erase Suspend to Status	"1"	Status	Erase Susp. to Read Array	Program Setup	Erase Susp. to Read Array	Erase	Erase Susp. to Read Array	Erase	Erase Susp. to Read Status	Erase Susp. to Read Array	Ers. Susp. to Read Identifier
Erase Susp. to Read Array	"1"	Array	Erase Susp. to Read Array	Program Setup	Erase Susp. to Read Array	Erase	Erase Susp. to Read Array	Erase	Erase Susp. to Read Status	Erase Susp. to Read Array	Ers. Susp. to Read Identifier
Erase Susp. to Read Identifier	"1"	Identifier	Erase Susp. to Read Array	Program Setup	Erase Susp. to Read Array	Erase	Erase Susp. to Read Array	Erase	Erase Susp. to Read Status	Erase Susp. to Read Array	Ers. Susp. to Read Identifier
Erase (complete)	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier

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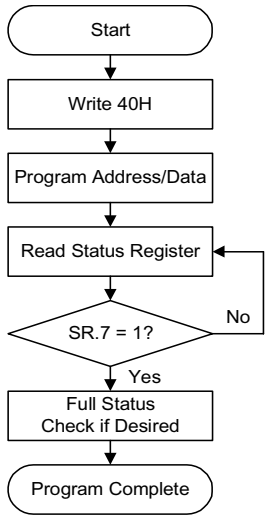
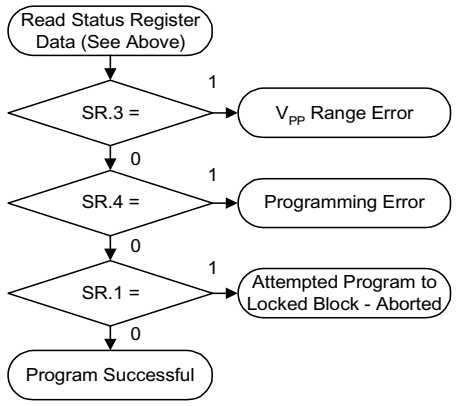
Appendix B Program and Erase Flowcharts

Figure 15. Program Flowchart



Bus Operation	Command	Comments
Write	Program Setup	Data = 40H
Write	Program	Data = Data to Program Addr = Location to Program
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent programming operations. SR Full Status Check can be done after each program or after a sequence of program operations. Write FFH after the last program operation to reset device to read array mode.		

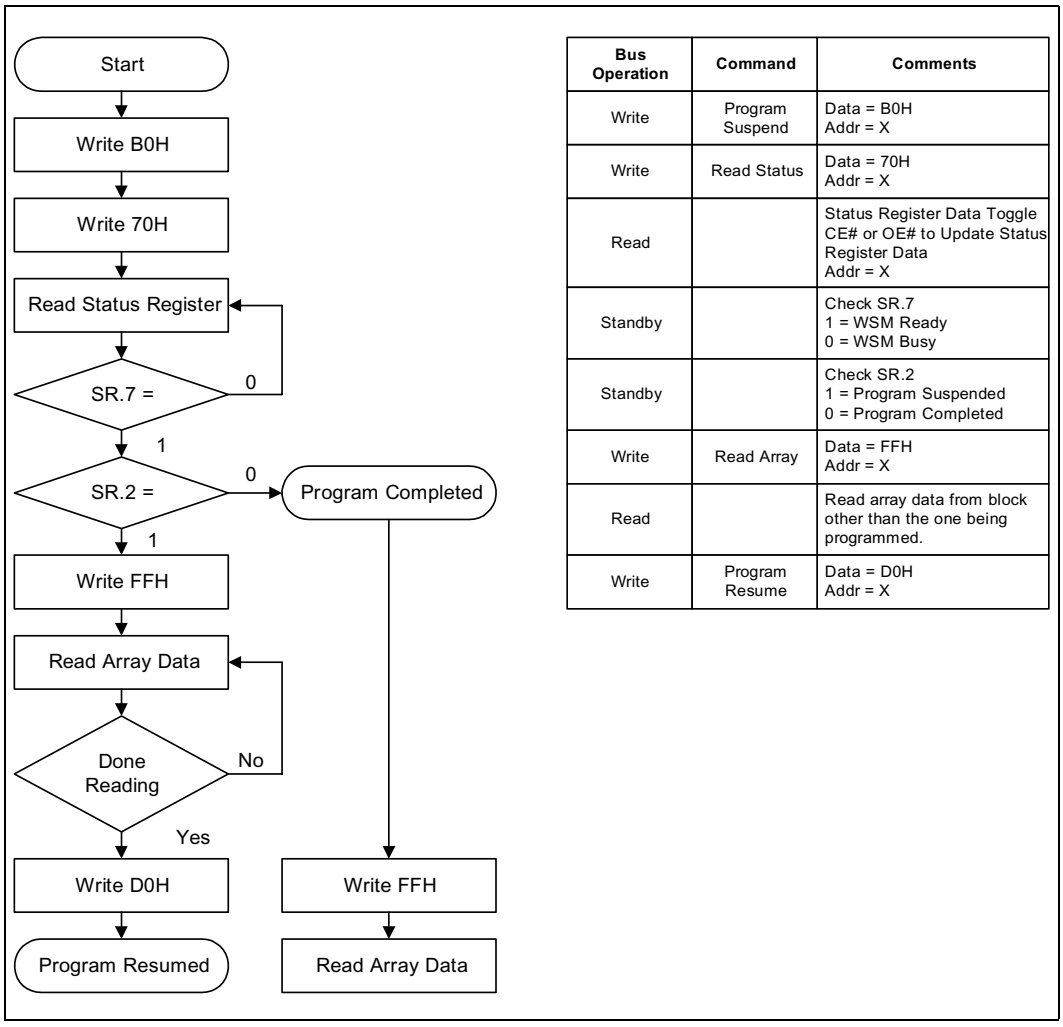
FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4 1 = V_{PP} Program Error
Standby		Check SR.1 1 = Attempted Program to Locked Block - Program Aborted
SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine. SR.1, SR.3 and SR.4 are only cleared by the Clear Staus Register Command, in cases where multiple bytes are programmed before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

0580_E1

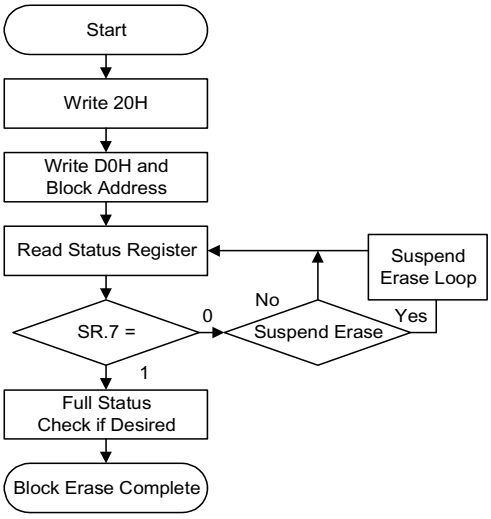
Figure 16. Program Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Program Suspend	Data = B0H Addr = X
Write	Read Status	Data = 70H Addr = X
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.2 1 = Program Suspended 0 = Program Completed
Write	Read Array	Data = FFH Addr = X
Read		Read array data from block other than the one being programmed.
Write	Program Resume	Data = D0H Addr = X

0580_E2

Figure 17. Block Erase Flowchart



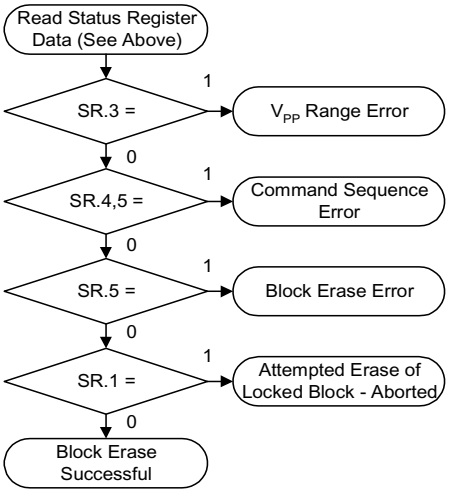
Bus Operation	Command	Comments
Write	Erase Setup	Data = 20H Addr = Within Block to Be Erased
Write	Erase Confirm	Data = D0H Addr = Within Block to Be Erased
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent block erasures.

Full Status Check can be done after each block erase or after a sequence of block erasures.

Write FFH after the last write operation to reset device to read array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4,5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block EraseError
Standby		Check SR.1 1 = Attempted Erase of Locked Block - Erase Aborted

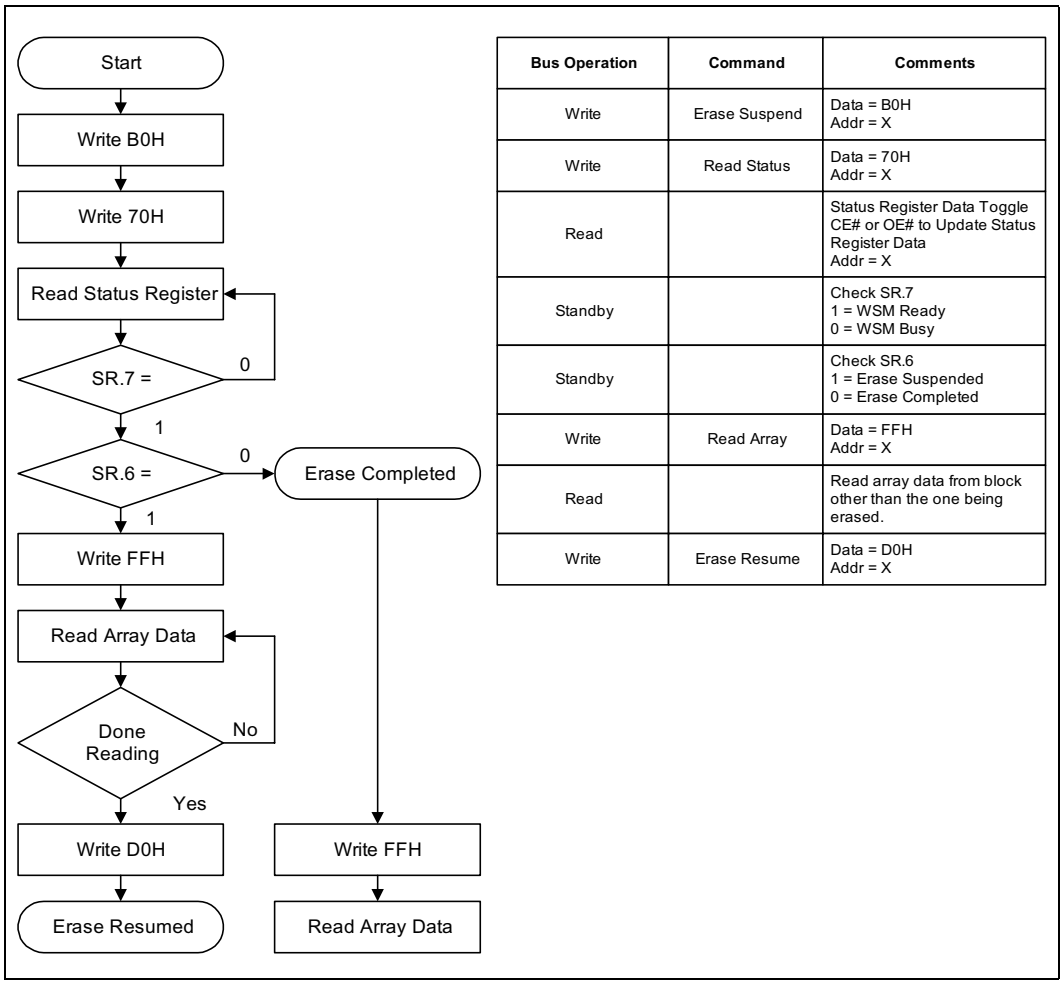
SR. 1 and 3 MUST be cleared, if set during an erase attempt, before further attempts are allowed by the Write State Machine.

SR.1, 3, 4, 5 are only cleared by the Clear Staus Register Command, in cases where multiple bytes are erased before full status is checked.

If an error is detected, clear the status register before attempting retry or other error recovery.

0580_E3

Figure 18. Erase Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H Addr = X
Write	Read Status	Data = 70H Addr = X
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Erase Suspended 0 = Erase Completed
Write	Read Array	Data = FFH Addr = X
Read		Read array data from block other than the one being erased.
Write	Erase Resume	Data = D0H Addr = X

0580_E4

Appendix C Ordering Information

Figure 19. Ordering Information

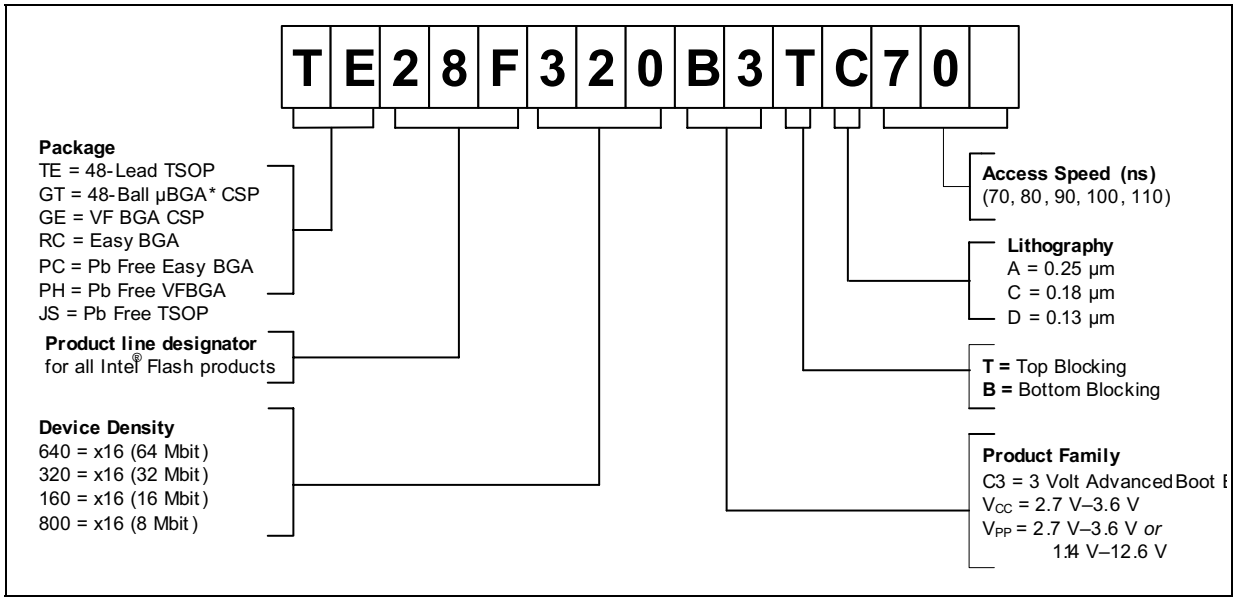


Table 31. Ordering Information: Valid Combinations (Sheet 1 of 2)

	40-Lead TSOP	48-Lead TSOP	48-Ball µBGA CSP(1,2)	48-Ball VF BGA
Ext. Temp. 64 Mbit		TE28F640B3TC80 TE28F640B3BC80		GE28F640B3TC80 GE28F640B3BC80
Ext. Temp. 32 Mbit		TE28F320B3TD70 TE28F320B3BD70 TE28F320B3TC70 TE28F320B3BC70 TE28F320B3TC90 TE28F320B3BC90 TE28F320B3TA100 TE28F320B3BA100 TE28F320B3TA110 TE28F320B3BA110 JS28F320B3TD70 JS28F320B3BD70		GE28F320B3TD70 GE28F320B3BD70 GE28F320B3TC70 GE28F320B3BC70 GE28F320B3TC90 GE28F320B3BC90 PH28F320B3BD70

Table 31. Ordering Information: Valid Combinations (Sheet 2 of 2)

	40-Lead TSOP	48-Lead TSOP	48-Ball µBGA CSP[1,2]	48-Ball VF BGA
Ext. Temp. 16 Mbit	TE28F016B3TA90 TE28F016B3BA90 TE28F016B3TA110 TE28F016B3BA110	TE28F160B3TD70 TE28F160B3BD70 TE28F160B3TC70 TE28F160B3BC70 TE28F160B3TC80 TE28F160B3BC80 TE28F160B3TC90 TE28F160B3BC90 TE28F160B3TA90 TE28F160B3BA90 TE28F160B3TA110 TE28F160B3BA110 JS28F160B3TA70 JS28F160B3BD70	GT28F160B3TA90[3] GT28F160B3BA90[3] GT28F160B3TA110[3] GT28F160B3BA110[3]	GE28F160B3TD70 GE28F160B3BD70 GE28F160B3TC70 GE28F160B3BC70 GE28F160B3TC80 GE28F160B3BC80 GE28F160B3TC90 GE28F160B3BC90 PH28F160B3TD70 PH28F160B3BD70
Ext. Temp. 8 Mbit	TE28F008B3TA90 TE28F008B3BA90 TE28F008B3TA110 TE28F008B3BA110	TE28F800B3TA90 TE28F800B3BA90 TE28F800B3TA110 TE28F800B3BA110		GE28F800B3TA70 GE28F800B3BA70 GE28F008B3TA70 GE28F008B3BA70 GE28F800B3TA90 GE28F800B3BA90 GE28F008B3TA90 GE28F008B3BA90

NOTES:
1. The 48-ball µBGA package top side mark reads F160B3. This mark is identical for both x8 and x16 products. All product shipping boxes or trays provide the correct information regarding bus architecture. However, once the devices are removed from the shipping media, it may be difficult to differentiate based on the top side mark. The device identifier (accessible through the Device ID command: see Section 11.2, “Read Identifier” on page 56 for further details) enables x8 and x16 µBGA package product differentiation.
2. The second line of the 48-ball µBGA package top side mark specifies assembly codes. For samples only, the first character signifies either “E” for engineering samples or “S” for silicon daisy-chain samples. All other assembly codes without an “E” or “S” as the first character are production units.
3. Intel recommends using.18 µm Intel® Advanced Boot Block Products.