SHARP

		Date	Jan. 16. 2003
PRELIMINARY DA	TASHEET		
	DATAS	HEE	<u>Т</u>
	64M (x16) Flash Memo	ory	
MODEL NO :	LH28F640BFHB-PT	TL60	
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- When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.
 - The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).
 - Office electronics
 - Instrumentation and measuring equipment
 - Machine tools
 - Audiovisual equipment
 - Home appliance
 - Communication equipment other than for trunk lines
 - (2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
 - Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
 - Mainframe computers
 - Traffic control systems
 - Gas leak detectors and automatic cutoff devices
 - Rescue and security equipment
 - Other safety devices and safety equipment, etc.
 - (3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
 - Aerospace equipment
 - Communications equipment for trunk lines
 - Control equipment for the nuclear power industry
 - Medical equipment related to life support, etc.
 - (4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.
- Please direct all queries regarding the products covered herein to a sales representative of the company.

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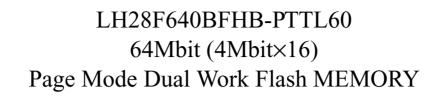
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2 Related Document Information

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■ 64M density with 16Bit I/O Interface

- High Performance Reads
 60/25ns 8-Word Page Mode
- Configurative 4-Plane Dual Work
 - Flexible Partitioning
 - Read operations during Block Erase or (Page Buffer) Program
 - Status Register for Each Partition

Low Power Operation

- 2.7V Read and Write Operations
- \bullet V_{CCO} for Input/Output Power Supply Isolation
- Automatic Power Savings Mode Reduces I_{CCR} in Static Mode
- Enhanced Code + Data Storage
 5µs Typical Erase/Program Suspends
- OTP (One Time Program) Block
 - 4-Word Factory-Programmed Area
 - 4-Word User-Programmable Area
- High Performance Program with Page Buffer
 - 16-Word Page Buffer
 - + 5µs/Word (Typ.) at 12V $V_{\ensuremath{PP}}$
- Operating Temperature -40°C to +85°C
- CMOS Process (P-type silicon substrate)

- Flexible Blocking Architecture
 - Eight 4K-word Parameter Blocks
 - One-hundred and twenty-seven 32K-word Main Blocks
 - Top Parameter Location
- Enhanced Data Protection Features
 - Individual Block Lock and Block Lock-Down with Zero-Latency
 - All blocks are locked at power-up or device reset.
 - Absolute Protection with $V_{PP} \leq V_{PPLK}$
 - Block Erase, Full Chip Erase, (Page Buffer) Word Program Lockout during Power Transitions
- Automated Erase/Program Algorithms
 - 3.0V Low-Power 11µs/Word (Typ.) Programming
 - 12V No Glue Logic 9µs/Word (Typ.) Production Programming and 0.5s Erase (Typ.)
- Cross-Compatible Command Support
 - Basic Command Set
 - Common Flash Interface (CFI)
- Extended Cycling Capability
 Minimum 100,000 Block Erase Cycles
- 0.8mm pitch 60-Ball CSP
- ETOX^{TM*} Flash Technology
- Not designed or rated as radiation hardened

The product, which is 4-Plane Page Mode Dual Work (Simultaneous Read while Erase/Program) Flash memory, is a low power, high density, low cost, nonvolatile read/write storage solution for a wide range of applications. The product can operate at V_{CC} =2.7V-3.6V and V_{PP} =1.65V-3.6V or 11.7V-12.3V. Its low voltage operation capability greatly extends battery life for portable applications.

The product provides high performance asynchronous page mode. It allows code execution directly from Flash, thus eliminating time consuming wait states. Furthermore, its newly configurative partitioning architecture allows flexible dual work operation.

The memory array block architecture utilizes Enhanced Data Protection features, and provides separate Parameter and Main Blocks that provide maximum flexibility for safe nonvolatile code and data storage.

Fast program capability is provided through the use of high speed Page Buffer Program.

Special OTP (One Time Program) block provides an area to store permanent code such as a unique number.

* ETOX is a trademark of Intel Corporation.

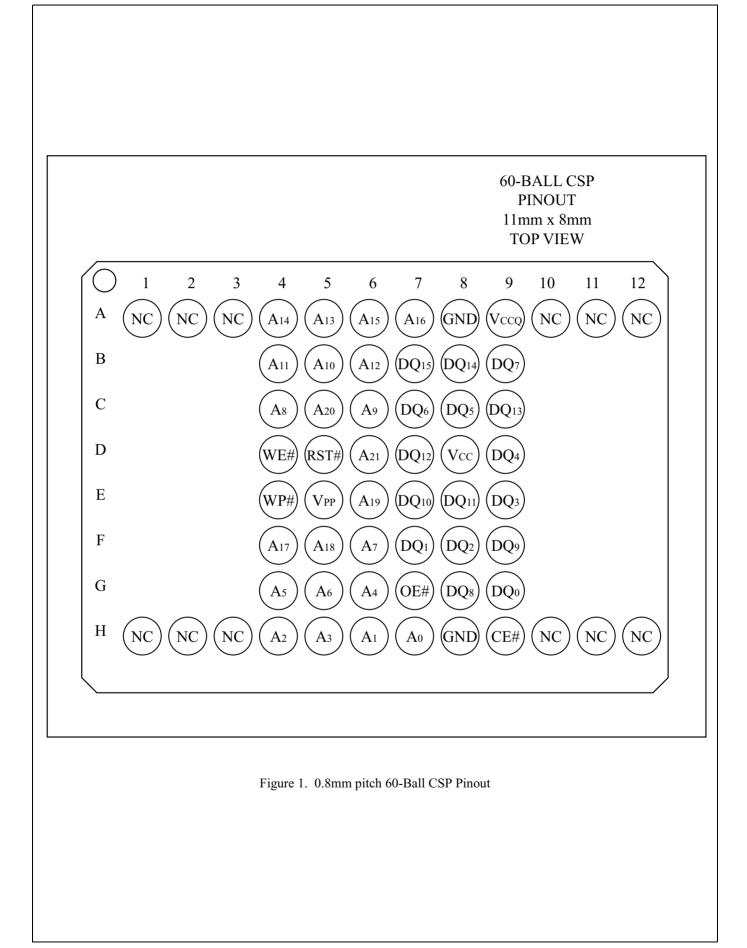


Table 1. Pin Descriptions

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Symbol	Туре	Name and Function
A ₀ -A ₂₁	INPUT	ADDRESS INPUTS: Inputs for addresses. 64M: A ₀ -A ₂₁
DQ ₀ -DQ ₁₅	INPUT/ OUTPUT	DATA INPUTS/OUTPUTS: Inputs data and commands during CUI (Command Use Interface) write cycles, outputs data during memory array, status register, query code identifier code and partition configuration register code reads. Data pins float to high impedance (High Z) when the chip or outputs are deselected. Data is internally latched during an erase or program cycle.
CE#	INPUT	CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sens amplifiers. CE#-high (V_{IH}) deselects the device and reduces power consumption t standby levels.
RST#	INPUT	RESET: When low (V_{IL}) , RST# resets internal automation and inhibits write operation which provides data protection. RST#-high (V_{IH}) enables normal operation. After power-up or reset mode, the device is automatically set to read array mode. RST# must be low during power-up/down.
OE#	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
WE#	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data ar latched on the rising edge of CE# or WE# (whichever goes high first).
WP#	INPUT	WRITE PROTECT: When WP# is V_{IL} , locked-down blocks cannot be unlocked. Eras or program operation can be executed to the blocks which are not locked and not locked down. When WP# is V_{IH} , lock-down is disabled.
V _{PP}	INPUT	MONITORING POWER SUPPLY VOLTAGE: V_{PP} is not used for power supply pinWith $V_{PP} \leq V_{PPLK}$, block erase, full chip erase, (page buffer) program or OTP programcannot be executed and should not be attempted.Applying $12V\pm0.3V$ to V_{PP} provides fast erasing or fast programming mode. In thmode, V_{PP} is power supply pin. Applying $12V\pm0.3V$ to V_{PP} during erase/program caonly be done for a maximum of 1,000 cycles on each block. V_{PP} may be connected t $12V\pm0.3V$ for a total of 80 hours maximum. Use of this pin at 12V beyond these limitmay reduce block cycling capability or cause permanent damage.
V _{CC}	SUPPLY	DEVICE POWER SUPPLY (2.7V-3.6V): With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see D Characteristics) produce spurious results and should not be attempted.
V _{CCQ}	SUPPLY	INPUT/OUTPUT POWER SUPPLY (2.7V-3.6V): Power supply for all input/output pins.
CND	SUPPLY	GROUND: Do not float any ground pins.
GND	SULLI	GROOND. Do not noat any ground pins.

	THEN THE MODES ALLOWED IN THE OTHER PARTITION IS:										
IF ONE PARTITION IS:	Read Array	Read ID/OTP	Read Status	Read Query	Word Program	Page Buffer Program	OTP Program	Block Erase	Full Chip Erase	Program Suspend	Hrace
Read Array	Х	X	Х	Х	Х	Х		Х		Х	Х
Read ID/OTP	Х	X	Х	Х	Х	Х		Х		Х	Х
Read Status	Х	Х	Х	Х	Х	Х	Х	Х	X	Х	Х
Read Query	Х	Х	Х	Х	Х	Х		Х		Х	Х
Word Program	Х	Х	Х	Х							Х
Page Buffer Program	Х	Х	Х	Х							Х
OTP Program			Х								
Block Erase	Х	Х	Х	Х							
Full Chip Erase			Х								
Program Suspend	Х	Х	Х	Х							Х
Block Erase Suspend	Х	Х	Х	Х	Х	Х				Х	

Table 2. Simultaneous Operation Modes Allowed with Four $Planes^{(1, 2)}$

NOTES:

"X" denotes the operation available.
 Configurative Partition Dual Work Restrictions:

Status register reflects partition state, not WSM (Write State Machine) state - this allows a status register for each partition. Only one partition can be erased or programmed at a time - no command queuing. Commands must be written to an address within the block targeted by that command.

	134	CK NUMBEF	R ADDRESS RANGE 3ff000h - 3fffffh
	134	4K-WORD	3FE000H - 3FEFFFH
	132	4K-WORD	3FD000H - 3FDFFFH
	131	4K-WORD	3FC000H - 3FCFFFH
	130	4K-WORD 4K-WORD	3FB000H - 3FBFFFH 3FA000H - 3FAFFFH
	129	4K-WORD	3F9000H - 3F9FFFH
	127	4K-WORD	3F8000H - 3F8FFFH
	126	32K-WORD	3F0000H - 3F7FFH
	125 124	32K-WORD 32K-WORD	3E8000H - 3EFFFFH 3E0000H - 3E7FFFH
臣	124	32K-WORD	3D8000H - 3DFFFFH
F	122	32K-WORD	3D0000H - 3D7FFFH
F	121	32K-WORD	3C8000H - 3CFFFFH
2	120 119	32K-WORD 32K-WORD	3C0000H - 3C7FFFH 3B8000H - 3BFFFFH
Ë	119	32K-WORD	3B0000H - 3B7FFFH
Ξ.	117	32K-WORD	3A8000H - 3AFFFFH
Σ	116	32K-WORD	3A0000H - 3A7FFFH
S.	115	32K-WORD	398000H - 39FFFFH
Z	114	32K-WORD 32K-WORD	390000H - 397FFFH 388000H - 38FFFFH
PLANE3 (PARAMETER PLANE)	112	32K-WORD	380000H - 387FFFH
E	111	32K-WORD	378000H - 37FFFFH
Z	110	32K-WORD	370000H - 377FFFH
Y.	109 108	32K-WORD 32K-WORD	368000H - 36FFFFH 360000H - 367FFFH
Б	108	32K-WORD	358000H - 35FFFFH
	106	32K-WORD	350000H - 357FFFH
	105	32K-WORD	348000H - 34FFFFH
	104	32K-WORD	340000H - 347FFFH
	103	32K-WORD 32K-WORD	338000H - 33FFFFH 330000H - 337FFFH
	102	32K-WORD	328000H - 32FFFH
	100	32K-WORD	320000H - 327FFFH
	99	32K-WORD	318000H - 31FFFFH
	<u>98</u> 97	32K-WORD 32K-WORD	310000H - 317FFFH 308000H - 30FFFFH
	96	32K-WORD	300000H - 307FFFH
	95	32K-WORD	2F8000H - 2FFFFFH
	94	32K-WORD	2F0000H - 2F7FFFH 2E8000H - 2EFFFFH
	93 92	32K-WORD 32K-WORD	2E0000H - 2E7FFFH
	91	32K-WORD	2D8000H - 2DFFFFH
	90	32K-WORD	2D0000H - 2D7FFFH
	89	32K-WORD	2C8000H - 2CFFFFH
	88 87	32K-WORD 32K-WORD	2C0000H - 2C7FFFH 2B8000H - 2BFFFFH
Ê	86	32K-WORD	2B0000H - 2B7FFFH
	85	32K-WORD	2A8000H - 2AFFFFH
LA	84	32K-WORD	2A0000H - 2A7FFFH
Б	83	32K-WORD	298000H - 29FFFFH 290000H - 297FFFH
Σ	82 81	32K-WORD 32K-WORD	288000H - 28FFFFH
	80	32K-WORD	280000H - 287FFFH
SR		32K-WORD	278000H - 27FFFFH
IFOR	79	32K-WORD	270000H - 277FFFH
INIFOR	78		2600011 2CEEEEII
(UNIFOR	78 77	32K-WORD	268000H - 26FFFFH 260000H - 267FFFH
E2 (UNIFOR	78 77 76	32K-WORD 32K-WORD	268000H - 26FFFFH 260000H - 267FFFH 258000H - 25FFFFH
NE2 (UNIFOR	78 77	32K-WORD	260000H - 267FFFH
ANE2 (UNIFOR	78 77 76 75 74 73	32K-WORD 32K-WORD 32K-WORD	260000H - 267FFFH 258000H - 25FFFFH 250000H - 257FFFH 248000H - 24FFFFH
PLANE2 (UNIFORM PLAN	78 77 76 75 74 73 72	32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD	260000H - 267FFFH 258000H - 25FFFFH 250000H - 257FFFH 248000H - 24FFFFH 240000H - 247FFFH
PLANE2 (UNIFOR	78 77 76 75 74 73 72 71	32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD	260000H - 267FFFH 258000H - 25FFFFH 250000H - 257FFFH 248000H - 247FFFH 2480000H - 247FFFH 238000H - 23FFFFH
PLANE2 (UNIFOR	78 77 76 75 74 73 72 71 70	32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD	260000H - 267FFFH 258000H - 25FFFFH 250000H - 257FFFH 248000H - 24FFFFH 240000H - 247FFFH
PLANE2 (UNIFOR	78 77 76 75 74 73 72 71	32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD	260000H - 267FFFH 258000H - 25FFFFH 250000H - 257FFFH 248000H - 24FFFFH 240000H - 24FFFFH 238000H - 23FFFFH 238000H - 237FFFH
PLANE2 (UNIFOR	78 77 76 75 74 73 72 71 70 69 68 67	32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD	260000H - 267FFFH 258000H - 25FFFFH 250000H - 257FFFH 248000H - 247FFFH 240000H - 247FFFH 238000H - 237FFFH 238000H - 237FFFH 228000H - 227FFFH 228000H - 227FFFH 218000H - 21FFFFH
PLANE2 (UNIFOR	78 77 76 75 74 73 72 71 70 69 68	32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD 32K-WORD	260000H - 267FFFH 258000H - 25FFFFH 250000H - 257FFFH 248000H - 24FFFFH 240000H - 247FFFH 238000H - 237FFFH 230000H - 237FFFH 228000H - 227FFFH 228000H - 227FFFH

BLOCK NUMBER ADDRESS RANGE 63 32K-WORD 1F8000H - 1FFFFH 61 32K-WORD 1F0000H - 1F7FFH 60 32K-WORD 1E8000H - 1E7FFH 59 32K-WORD 1D8000H - 1D7FFFH 57 32K-WORD 1D8000H - 1D7FFFH 58 32K-WORD 1C8000H - 1D7FFFH 53 32K-WORD 1C8000H - 1D7FFFH 54 32K-WORD 180000H - 1D7FFFH 53 32K-WORD 180000H - 1B7FFFH 54 32K-WORD 180000H - 187FFFH 50 32K-WORD 180000H - 187FFFH 50 32K-WORD 188000H - 187FFFH 40 32K-WORD 188000H - 187FFFH 41 32K-WORD 188000H - 187FFFH 42 32K-WORD 188000H - 187FFFH 43 32K-WORD 188000H - 187FFFH 44 32K-WORD 188000H - 187FFFH 43 32K-WORD 188000H - 187FFFH 38 32K-WORD 188000H - 187FFFH 30 32K-WORD				
63 32K-WORD IF8000H - IFFFFH 62 32K-WORD IE8000H - IEFFFH 61 32K-WORD IE8000H - IEFFFH 59 32K-WORD IE0000H - IEFFFH 59 32K-WORD IE0000H - IDFFFH 57 32K-WORD IC8000H - ICFFFH 56 32K-WORD IE8000H - IBFFFH 53 32K-WORD IB8000H - IBFFFH 53 32K-WORD IB8000H - IBFFFH 51 32K-WORD IB8000H - IBFFFH 50 32K-WORD IB8000H - IAFFFH 51 32K-WORD I88000H - IAFFFH 50 32K-WORD I88000H - IAFFFH 40 32K-WORD I88000H - IAFFFH 41 32K-WORD I88000H - ISFFFH 42 32K-WORD I58000H - ISFFFH 44 32K-WORD I38000H - ISFFFH 43 32K-WORD I38000H - ISFFFH 44 32K-WORD I38000H - ISFFFH 43 32K-WORD I38000H - ISFFFH 36 32K-WORD <		BL (CK NUMBER	ADDRESS RANGE
1 32k.WORD 1F0000H - 1F7FFH 60 32k.WORD 1E8000H - 1EFFFH 50 32k.WORD 1D0000H - 1D7FFFH 58 32k.WORD 1D0000H - 1D7FFFH 57 32k.WORD 1C8000H - 1D7FFFH 56 32k.WORD 1B8000H - 1B7FFFH 56 32k.WORD 1B8000H - 1B7FFFH 53 32k.WORD 1A8000H - 1A7FFFH 51 32k.WORD 180000H - 197FFFH 51 32k.WORD 180000H - 187FFFH 50 32k.WORD 180000H - 187FFFH 51 32k.WORD 180000H - 187FFFH 49 32k.WORD 180000H - 167FFFH 46 32k.WORD 168000H - 167FFFH 47 32k.WORD 158000H - 157FFFH 43 32k.WORD 158000H - 157FFFH 44 32k.WORD 138000H - 157FFFH 38 32k.WORD 138000H - 157FFFH 38 32k.WORD 128000H - 127FFFH 36 32k.WORD 128000H - 137FFFH 36 32k.WO		-		-
61 32K-WORD IE8000H - IEFFFH 59 32K-WORD IB0000H - IDFFFFH 58 32K-WORD ID8000H - IDFFFFH 57 32K-WORD IC0000H - IC7FFFH 56 32K-WORD IB8000H - IBFFFH 56 32K-WORD IB8000H - IA7FFFH 53 32K-WORD IA8000H - IA7FFFH 53 32K-WORD IA8000H - IA7FFFH 53 32K-WORD IA8000H - IA7FFFH 50 32K-WORD I88000H - IA7FFFH 50 32K-WORD I88000H - IA7FFFH 40 32K-WORD I88000H - IA7FFFH 47 32K-WORD I88000H - IA7FFFH 48 32K-WORD I88000H - IA7FFFH 41 32K-WORD I58000H - IA7FFFH 42 32K-WORD I58000H - IA7FFFH 33 32K-WORD I58000H - IA7FFFH 34 32K-WORD I58000H - IA7FFFH 35 32K-WORD I38000H - IA7FFFH 36 32K-WORD I38000H - IA7FFFH 37 32K-W				
59 32k.WORD 1D8000H - 1DFFFH 57 32k.WORD 1D0000H - 1D7FFFH 57 32k.WORD 1C8000H - 1C7FFFH 56 32k.WORD 1C8000H - 1C7FFFH 55 32k.WORD 1B8000H - 1BFFFFH 53 32k.WORD 1A8000H - 1BFFFFH 53 32k.WORD 1A8000H - 1AFFFFH 51 32k.WORD 180000H - 19FFFFH 50 32k.WORD 180000H - 18FFFFH 49 32k.WORD 180000H - 18FFFFH 49 32k.WORD 180000H - 18FFFFH 46 32k.WORD 180000H - 18FFFFH 46 32k.WORD 158000H - 15FFFH 42 32k.WORD 158000H - 15FFFH 43 32k.WORD 138000H - 13FFFFH 38 32k.WORD 138000H - 13FFFFH 38 32k.WORD 128000H - 12FFFH 36 32k.WORD 128000H - 12FFFH 37 32k.WORD 128000H - 12FFFH 36 32k.WORD 128000H - 0FFFFH 36 32k.WORD </td <td></td> <td></td> <td></td> <td></td>				
S8 32K-WORD 1D0000H - 1D7FFFH 57 32K-WORD IC8000H - IC7FFFH 56 32K-WORD IB8000H - IBFFFH 54 32K-WORD IB8000H - IBFFFH 53 32K-WORD IA8000H - IAFFFFH 53 32K-WORD IA8000H - IAFFFFH 50 32K-WORD I90000H - 197FFFH 50 32K-WORD I8000H - 18FFFFH 44 32K-WORD I8000H - 18FFFFH 45 32K-WORD I8000H - 18FFFFH 46 32K-WORD I68000H - 16FFFFH 46 32K-WORD I58000H - 15FFFFH 43 32K-WORD I58000H - 15FFFFH 43 32K-WORD I38000H - 13FFFFH 44 32K-WORD I28000H - 13FFFFH 36 32K-WORD I28000H - 13FFFFH 37 32K-WORD I28000H - 13FFFFH 38 32K-WORD I28000H - 117FFFH 36 32K-WORD I28000H - 0FFFFH 36 32K-WORD 068000H - 0FFFFH 30 32K-WORD </td <td></td> <td></td> <td></td> <td></td>				
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7 32K-WORD 030000H - 037FFFH 6 32K-WORD 030000H - 037FFFH 5 32K-WORD 028000H - 02FFFFH 4 32K-WORD 020000H - 027FFFH 3 32K-WORD 018000H - 017FFFH 2 32K-WORD 010000H - 017FFFH 1 32K-WORD 008000H - 00FFFFH	Ħ			
7 32K-WORD 030000H - 037FFFH 6 32K-WORD 030000H - 037FFFH 5 32K-WORD 028000H - 02FFFFH 4 32K-WORD 020000H - 027FFFH 3 32K-WORD 018000H - 017FFFH 2 32K-WORD 010000H - 017FFFH 1 32K-WORD 008000H - 00FFFFH	5			
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2 32K-WORD 010000H - 017FFFH 1 32K-WORD 008000H - 00FFFFH	1			
1 32K-WORD 008000H - 00FFFFH	1			
0 32K-WORD 000000H - 007FFFH	1			008000H - 00FFFFH
		0	32K-WORD	000000H - 007FFFH

Figure 2. Memory Map (Top Parameter)

	Code	Address [A ₁₅ -A ₀]	Data [DQ ₁₅ -DQ ₀]	Notes
Manufacturer Code	Manufacturer Code	0000H	00B0H	1
Device Code	Top Parameter Device Code	0001H	00B0H	1, 2
Block Lock Configuration	Block is Unlocked		$DQ_0 = 0$	3
Code	Block is Locked	Block	$DQ_0 = 1$	3
	Block is not Locked-Down	Address + 2	$DQ_1 = 0$	3
	Block is Locked-Down		$DQ_1 = 1$	3
Device Configuration Code	Partition Configuration Register	0006H	PCRC	1, 4
OTP	OTP Lock	0080H	OTP-LK	1, 5
	OTP	0081-0088H	OTP	1, 6

NOTES:

1. The address A₂₁-A₁₆ are shown in below table for reading the manufacturer code, device code, device configuration code and OTP data.

2. Top parameter device has its parameter blocks in the plane3 (The highest address).

- Block Address = The beginning location of a block address within the partition to which the Read Identifier Codes/OTP command (90H) has been written. DQ₁₅-DQ₂ are reserved for future implementation.
- 4. PCRC=Partition Configuration Register Code.
- 5. OTP-LK=OTP Block Lock configuration.

6. OTP=OTP Block data.

Partition C	Configuration I	Register ⁽²⁾	Address (64M-bit device)
PCR.10	PCR.9	PCR.8	[A ₂₁ -A ₁₆]
0	0	0	00H
0	0	1	00H or 10H
0	1	0	00H or 20H
1	0	0	00H or 30H
0	1	1	00H or 10H or 20H
1	1	0	00H or 20H or 30H
1	0	1	00H or 10H or 30H
1	1	1	00H or 10H or 20H or 30H

Table 4. Identifier Codes and OTP Address for Read Operation on Partition Configuration⁽¹⁾ (64M-bit device)

NOTES:

1. The address to read the identifier codes or OTP data is dependent on the partition which is selected when writing the Read Identifier Codes/OTP command (90H).

2. Refer to Table 12 for the partition configuration register.

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000088H	
	Customer Programmable Area
000085H	
000084H	
	Factory Programmed Area
000081H	
000080H	Reserved for Future Implementation (DQ15-DQ2)

Figure 3. OTP Block Address Map for OTP Program (The area outside 80H~88H cannot be used.)

Mode	Notes	RST#	CE#	OE#	WE#	Address	V _{PP}	DQ ₀₋₁₅	
Read Array	6	V _{IH}	V _{IL}	V _{IL}	V _{IH}	Х	Х	D _{OUT}	
Output Disable		V _{IH}	V _{IL}	V _{IH}	V _{IH}	Х	Х	High Z	
Standby		V _{IH}	V _{IH}	Х	Х	Х	Х	High Z	
Reset	3	V _{IL}	Х	Х	Х	Х	Х	High Z	
Read Identifier Codes/OTP	6	V _{IH}	V _{IL}	V _{IL}	V _{IH}	See Table 3 and Table 4	X	See Table 3 and Table 4	
Read Query	6,7	V _{IH}	V _{IL}	V _{IL}	V _{IH}	See Appendix	Х	See Appendix	
Write	4,5,6	V _{IH}	V _{IL}	V _{IH}	V _{IL}	Х	Х	D _{IN}	

Table 5. Bus $Operation^{(1,2)}$

NOTES:

Refer to DC Characteristics. When V_{PP}≤V_{PPLK}, memory contents can be read, but cannot be altered.
 X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or V_{PPH1/2} for V_{PP}. See DC Characteristics for V_{PPLK} and V_{PPH1/2} voltages.
 RST# at GND±0.2V ensures the lowest power consumption.

4. Command writes involving block erase, full chip erase, (page buffer) program or OTP program are reliably executed when V_{PP}=V_{PPH1/2} and V_{CC}=2.7V-3.6V.
5. Refer to Table 6 for valid D_{IN} during a write operation.
6. Never hold OE# low and WE# low at the same timing.

7. Refer to Appendix of LH28F640BF series for more information about query code.

	Т	able 6. C	Command	Definitions ⁽¹	1)			
	Bus		I	First Bus Cyc	le	Se	econd Bus C	ycle
Command	Cycles Req'd	Notes	Oper ⁽¹⁾	Addr ⁽²⁾	Data	Oper ⁽¹⁾	Addr ⁽²⁾	Data ⁽³⁾
Read Array	1		Write	PA	FFH			
Read Identifier Codes/OTP	≥2	4	Write	PA	90H	Read	IA or OA	ID or OD
Read Query	≥2	4	Write	PA	98H	Read	QA	QD
Read Status Register	2		Write	PA	70H	Read	PA	SRD
Clear Status Register	1		Write	PA	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Full Chip Erase	2	5,9	Write	Х	30H	Write	Х	D0H
Program	2	5,6	Write	WA	40H or 10H	Write	WA	WD
Page Buffer Program	≥4	5,7	Write	WA	E8H	Write	WA	N-1
Block Erase and (Page Buffer) Program Suspend	1	8,9	Write	PA	B0H			
Block Erase and (Page Buffer) Program Resume	1	8,9	Write	PA	D0H			
Set Block Lock Bit	2		Write	BA	60H	Write	BA	01H
Clear Block Lock Bit	2	10	Write	BA	60H	Write	BA	D0H
Set Block Lock-down Bit	2		Write	BA	60H	Write	BA	2FH
OTP Program	2	9	Write	OA	СОН	Write	OA	OD
Set Partition Configuration Register	2		Write	PCRC	60H	Write	PCRC	04H

NOTES:

1. Bus operations are defined in Table 5.

2. All addresses which are written at the first bus cycle should be the same as the addresses which are written at the second bus cvcle.

X=Any valid address within the device.

PA=Address within the selected partition.

IA=Identifier codes address (See Table 3 and Table 4).

QA=Query codes address. Refer to Appendix of LH28F640BF series for details.

BA=Address within the block being erased, set/cleared block lock bit or set block lock-down bit.

WA=Address of memory location for the Program command or the first address for the Page Buffer Program command. OA=Address of OTP block to be read or programmed (See Figure 3).

PCRC=Partition configuration register code presented on the address A₀-A₁₅.

3. ID=Data read from identifier codes. (See Table 3 and Table 4).

QD=Data read from query database. Refer to Appendix of LH28F640BF series for details.

SRD=Data read from status register. See Table 10 and Table 11 for a description of the status register bits.

WD=Data to be programmed at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first) during command write cycles.

OD=Data within OTP block. Data is latched on the rising edge of WE# or CE# (whichever goes high first) during command write cycles.

N-1=N is the number of the words to be loaded into a page buffer.

4. Following the Read Identifier Codes/OTP command, read operations access manufacturer code, device code, block lock configuration code, partition configuration register code and the data within OTP block (See Table 3 and Table 4). The Read Query command is available for reading CFI (Common Flash Interface) information.

5. Block erase, full chip erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when RST# is V_{IH}.

6. Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.

7. Following the third bus cycle, input the program sequential address and write data of "N" times. Finally, input the any valid address within the target block to be programmed and the confirm command (D0H). Refer to Appendix of LH28F640BF series for details.

- 8. If the program operation in one partition is suspended and the erase operation in other partition is also suspended, the suspended program operation should be resumed first, and then the suspended erase operation should be resumed next.
- 9. Full chip erase and OTP program operations can not be suspended. The OTP Program command can not be accepted while the block erase operation is being suspended.
- 10. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when WP# is V_{IL}. When WP# is V_{IH}, lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.
 11. Commands other than those shown above are reserved by SHARP for future device implementations and should not be
- used.

		Cu	rrent State				
State	WP#	DQ1 ⁽¹⁾	DQ ₀ ⁽¹⁾	State Name	Erase/Program Allowed ⁽²⁾		
[000]	0	0	0	Unlocked	Yes		
[001] ⁽³⁾	0	0	1	Locked	No		
[011]	0	1	1	Locked-down	No		
[100]	1	0	0	Unlocked	Yes		
[101] ⁽³⁾	1	0	1	Locked	No		
[110] ⁽⁴⁾	1	1	0	Lock-down Disable	Yes		
[111]	1	1	1	Lock-down Disable	No		

Table 7. Functions of Block Lock⁽⁵⁾ and Block Lock-Down

NOTES:

1. $DQ_0=1$: a block is locked; $DQ_0=0$: a block is unlocked.

 $DQ_1=1$: a block is locked-down; $DQ_1=0$: a block is not locked-down.

2. Erase and program are general terms, respectively, to express: block erase, full chip erase and (page buffer) program operations.

3. At power-up or device reset, all blocks default to locked state and are not locked-down, that is,

[001] (WP#=0) or [101] (WP#=1), regardless of the states before power-off or reset operation. 4. When WP# is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.

5. OTP (One Time Program) block has the lock function which is different from those described above.

	Curren	t State		Result after Lock Command Written (Next State)					
State	WP#	DQ ₁	DQ ₀	Set Lock ⁽¹⁾	Clear Lock ⁽¹⁾	Set Lock-down ⁽¹⁾			
[000]	0	0	0	[001]	No Change	[011] ⁽²⁾			
[001]	0	0	1	No Change ⁽³⁾	[000]	[011]			
[011]	0	1	1	No Change	No Change	No Change			
[100]	1	0	0	[101]	No Change	[111] ⁽²⁾			
[101]	1	0	1	No Change	[100]	[111]			
[110]	1	1	0	[111]	No Change	[111] ⁽²⁾			
[111]	1	1	1	No Change	[110]	No Change			

Table 8. Block Locking State Transitions upon Command Write⁽⁴⁾

NOTES:

1. "Set Lock" means Set Block Lock Bit command, "Clear Lock" means Clear Block Lock Bit command and "Set Lock-down" means Set Block Lock-Down Bit command.

2. When the Set Block Lock-Down Bit command is written to the unlocked block ($DQ_0=0$), the corresponding block is locked-down and automatically locked at the same time.

3. "No Change" means that the state remains unchanged after the command written.

4. In this state transitions table, assumes that WP# is not changed and fixed V_{IL} or V_{IH} .

Day is a first	(Current S	State		Result after WP# Transition (Next State)			
Previous State	State	WP#	DQ ₁	DQ ₀	WP#= $0 \rightarrow 1^{(1)}$	WP#= $1 \rightarrow 0^{(1)}$		
-	[000]	0	0	0	[100]	-		
-	[001]	0	0	1	[101]	-		
[110] ⁽²⁾	[011]	0	1	1	[110]	-		
Other than [110] ⁽²⁾	[011]	0	1	1	[111]	-		
-	[100]	1	0	0	-	[000]		
-	[101]	1	0	1	-	[001]		
-	[110]	1	1	0	-	[011] ⁽³⁾		
-	[111]	1	1	1	-	[011]		

Table 9. Block Locking State Transitions upon WP# Transition⁽⁴⁾

NOTES:

1. "WP#=0 \rightarrow 1" means that WP# is driven to V_{IH} and "WP#=1 \rightarrow 0" means that WP# is driven to V_{IL}.

2. State transition from the current state [011] to the next state depends on the previous state.

3. When WP# is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.

4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.

R	R	R	R	R	R	R	R				
15	14	13	12	11	10	9	8				
WSMS	BESS	BEFCES	PBPOPS	VPPS	PBPSS	DPS	R				
7	6	5	4	3	2	1	0				
ENHANCE R.7 = WRITI 1 = Ready 0 = Busy R.6 = BLOC 1 = Block 0 = Block R.5 = BLOC STAT 1 = Error i 0 = Succes R.4 = (PAGH OTP 1 = Error i 0 = Succes R.3 = V _{PP} S' 1 = V _{PP} L 0 = V _{PP} O R.2 = (PAGH STAT 1 = (Page	EMENTS (R) E STATE MAC E STATE MAC E STATE MAC Erase Suspende Erase in Progree E ERASE ANE CUS (BEFCES) n Block Erase Stul Block Erase Stul Block Erase E BUFFER) PR PROGRAM ST n (Page Buffer) Stul (Page Buffer) Stul (Page Buffer) OW Detect, Op K E BUFFER) PR CUS (PBPSS) Buffer) Program	ess/Completed D FULL CHIP H or Full Chip Era se or Full Chip H OGRAM AND FATUS (PBPOP) Program or OT fer) Program or OT fer) Program or OT	S (BESS) ERASE se Erase S) P Program OTP Program	(Write State M be occupied by 3 or 4 partition Check SR.7 to buffer) program invalid while S If both SR.5 a erase, (page to block lock-do attempt, an im SR.3 does not The WSM into Block Erase, F Program com report accurate SR.1 does not bit. The WSM Erase, Full C Program com depending on set. Reading th	NOT r indicates the sta lachine). Even if y the other partiti ns configuration. o determine bloc m or OTP progra SR.7="0". and SR.4 are "1" puffer) program, own bit, set pa proper command provide a contin errogates and ind full Chip Erase, (mand sequences e feedback when provide a contin interrogates the Chip Erase, (Pag mand sequences the attempted op ne block lock con ntifier Codes/OT	atus of the partit the SR.7 is "1", ion when the de k erase, full ch m completion. S s after a block of set/clear block ritition configu l sequence was of nuous indication licates the V _{PP} I (Page Buffer) Pro- s. SR.3 is not V _{PP} \neq V _{PPH1} , V _I nuous indication block lock bit of ge Buffer) Pro- es. It informs eration, if the b nfiguration code	the WSM m vice is set to ip erase, (pa SR.6 - SR.1 a erase, full ch c lock bit, s ration regis entered. n of V_{PP} lev evel only af rogram or O' guaranteed opH2 or V_{PPL} n of block lo nly after Blo gram or O' the syste lock lock bit es after writi				
		STATUS (DPS)		lock bit status.		reved for future	use and show				
	or Program Atte d Block, Opera ked			SR.15 - SR.8 and SR.0 are reserved for future use and sho be masked out when polling the status register.							

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		Table 1	1. Extended Sta	atus Register De	efinition			
R	R	R	R	R	R	R	R	
15	14	13	12	11	10	9	8	
SMS	R	R	R	R	R	R	R	
7	6	5	4	3	2	1	0	
XSR.15-8 = RESERVED FOR FUTURE ENHANCEMENTS (R) XSR.7 = STATE MACHINE STATUS (SMS) 1 = Page Buffer Program available 0 = Page Buffer Program not available				NOTES: After issue a Page Buffer Program command (E8H), XSR.7="1" indicates that the entered command is accepted. If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not.				
XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)							future use and extended status	

		Table 12.	Partition Config	uration R	Regist	ter Definition		
R	R	R	R	R		PC2	PC1	PC0
15	14	13	12	11		10	9	8
R	R	R	R	R		R	R	R
7	6	5	4	3		2	1	0
PCR.15-11 = 1PCR.10-8 = P $000 = No$ $001 = Pla$ $(defau)$ $010 = Pla$ $(defau)$ $011 = Pla$ $(defau)$ $011 = Pla$ $three$ $operal$ $101 = Pla$ $three$ $operal$ $101 = Pla$ $three$ $operal$ $0 = 0$ $0 = 0$ $0 = 0$ $0 = 0$ $0 = 0$ $0 = 0$ $0 = 0$ $0 = 0$ $0 = 0$ $0 = 0$ $0 = 0$ $0 = 0$ $0 = 0$ $0 = 0$ $0 = 0$ $0 = 0$	RESERVED FOR ENHANCEMI ARTITION COM- partitioning. Du me1-3 are merge alt in a bottom paran in e 0-1 and Pland on respectively. me 0-2 are merge partitions in the tion is available in e 0-1 are merge partitions in the tion is available me 1-2 are merge partitions in the tion is available PARTITION FUNCTI	R FUTURE ENTS (R) IFIGURATION al Work is not a d into one parti arameter device e2-3 are merged ed into one part heter device) ed into one part his configuration between any two ed into one part his configuration ed into one part his	I (PC2-0) allowed. tion. b) I into one ition. There are on. Dual work to partitions. ition. There are on. Dual work to partitions.	111 PCR.7-0 "001" in paramet See Figu PCR.15- should	Each tivel two p P = R power- n a p er de ure 4 -11 a be ration <u>1 PC0</u>	ere are four partit plane correspon- y. Dual work oper- partitions. ESERVED FOR I ENHANCEMEN NOT- oup or device resub- bottom parameter vice. for the detail on p and PCR.7-0 are masked out w n register. PARTITION PARTITION PARTITION2 PAR ENHANCE PARTITION2 PAR ENHANCE PARTITION2 PAR ENHANCE PARTITION2 PAR ENHANCE PARTITION2 PAR ENHANCE PARTITION2 PAR ENHANCE PARTITION2 PAR ENHANCE PARTITION2 PAR ENHANCE PARTITION2 PAR ENHANCE PARTITION2 PAR ENHANCE PARTITION3 PART	ions in this connots to each pration is availa FUTURE TS (R) TES: et, PCR10-8 (0) reserved for hen checking VING FOR DU N2 PARTITION ENTITION PAR TITION PAR ENTITION PAR EN	PC2-0) is set to "100" in a top uration. future use and the partition UAL WORK N1 PARTITIONO UAL WORK N1 PARTITIONO UAL WORK N1 PARTITIONO PARTITIONO UAL WORK
		I	Figure 4. Partiti	on Confi	gurat	ion		
								Rev 2/1/

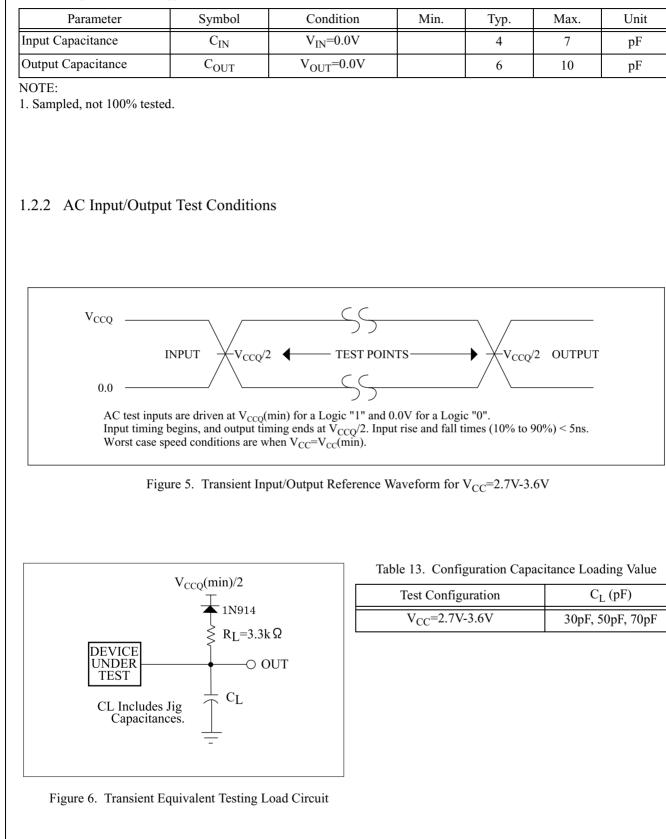
 Electrical Specifications Absolute Maximum Ratings[*] Operating Temperature During Read, Erase and Program40°C to +85°C ⁽¹⁾ 	*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.
	NOTES:
Storage Temperature During under Bias40°C to +85°C During non Bias65°C to +125°C	 Operating temperature is for extended temperature product defined by this specification. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC} and V_{PP} pins. During transitions,
Voltage On Any Pin (except V_{CC} and V_{PP})0.5V to V_{CC} +0.5V ⁽²⁾	this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is V_{CC} +0.5V which, during transitions, may overshoot to V_{CC} +2.0V for periods <20ns.
$\rm V_{CC}$ and $\rm V_{CCQ}$ Supply Voltage0.2V to +3.9V $^{(2)}$	 Maximum DC voltage on V_{PP} may overshoot to +13.0V for periods <20ns. V_{PP} erase/program voltage is normally 2.7V-3.6V. Applying 11.7V-12.3V to V_{PP} during erase/program
V_{PP} Supply Voltage0.2V to +12.6V ^(2, 3, 4)	can be done for a maximum of 1,000 cycles on the main blocks and 1,000 cycles on the parameter blocks. V_{PP} may be connected to 11.7V-12.3V for a total of 80
Output Short Circuit Current 100mA ⁽⁵⁾	hours maximum.5. Output shorted for no more than one second. No more than one output shorted at a time.

1.2 Operating Conditions

Parameter	Symbol	Min.	Тур.	Max.	Unit	Notes
Operating Temperature	T _A	-40	+25	+85	°C	
V _{CC} Supply Voltage	V _{CC}	2.7	3.0	3.6	V	1
I/O Supply Voltage	V _{CCQ}	2.7	3.0	3.6	V	1
V _{PP} Voltage when Used as a Logic Control	V _{PPH1}	1.65	3.0	3.6	V	1
V _{PP} Supply Voltage	V _{PPH2}	11.7	12	12.3	V	1, 2
Main Block Erase Cycling: V _{PP} =V _{PPH1}		100,000			Cycles	
Parameter Block Erase Cycling: V _{PP} =V _{PPH1}		100,000			Cycles	
Main Block Erase Cycling: V _{PP} =V _{PPH2} , 80 hrs.				1,000	Cycles	
Parameter Block Erase Cycling: $V_{PP}=V_{PPH2}$, 80 hrs.				1,000	Cycles	
Maximum V _{PP} hours at V _{PPH2}				80	Hours	

NOTES:

See DC Characteristics tables for voltage range-specific specification.
 Applying V_{PP}=11.7V-12.3V during a erase or program can be done for a maximum of 1,000 cycles on the main blocks and 1,000 cycles on the parameter blocks. A permanent connection to V_{PP}=11.7V-12.3V is not allowed and can cause damage to the device.



1.2.1 Capacitance⁽¹⁾ (T_A =+25°C, f=1MHz)

Rev. 2.44

1.2.3 DC Characteristics

V_{CC}=2.7V-3.6V

			cc					
Symbol	Paran	neter	Notes	Min.	Тур.	Max.	Unit	Test Conditions
I _{LI}	Input Load Current		1	-1.0		+1.0	μΑ	V _{CC} =V _{CC} Max.,
I _{LO}	Output Leakage Cur	rent	1	-1.0		+1.0	μΑ	V _{CCQ} =V _{CCQ} Max., V _{IN} /V _{OUT} =V _{CCQ} or GND
I _{CCS}	V _{CC} Standby Curren	V _{CC} Standby Current			4	20	μΑ	$V_{CC}=V_{CC}Max.,$ $CE\#=RST\#=$ $V_{CCQ}\pm0.2V,$ $WP\#=V_{CCQ} \text{ or GND}$
I _{CCAS}	V _{CC} Automatic Pow	V _{CC} Automatic Power Savings Current			4	20	μΑ	V _{CC} =V _{CC} Max., CE#=GND±0.2V, WP#=V _{CCQ} or GND
I _{CCD}	V _{CC} Reset Power-De	V _{CC} Reset Power-Down Current			4	20	μΑ	RST#=GND±0.2V
T	Average V _{CC} Read Current Normal Mode		1,7		15	25	mA	V _{CC} =V _{CC} Max., CE#=V _{IL} ,
I _{CCR}	Average V _{CC} Read Current Page Mode	8 Word Read	1,7		5	10	mA	OE#=V _{IH} , f=5MHz
т	V (De se Duffer) D	Comment	1,5,7		20	60	mA	V _{PP} =V _{PPH1}
I _{CCW}	V _{CC} (Page Buffer) P	Togram Current	1,5,7		10	20	mA	V _{PP} =V _{PPH2}
т	V _{CC} Block Erase, Fu	ıll Chip	1,5,7		10	30	mA	V _{PP} =V _{PPH1}
I _{CCE}	Erase Current		1,5,7		4	10	mA	V _{PP} =V _{PPH2}
I _{CCWS} I _{CCES}	V _{CC} (Page Buffer) P Block Erase Suspend	-	1,2,7		10	200	μA	CE#=V _{IH}
I _{PPS} I _{PPR}	V _{PP} Standby or Read	d Current	1,6,7		2	5	μΑ	V _{PP} ≤V _{CC}
т	V _{PP} (Page Buffer) P	rogram Current	1,5,6,7		2	5	μΑ	V _{PP} =V _{PPH1}
I _{PPW}	v pp (1 age Duilei) r		1,5,6,7		10	30	mA	V _{PP} =V _{PPH2}
T	V _{PP} Block Erase, Fu	ll Chip	1,5,6,7		2	5	μΑ	V _{PP} =V _{PPH1}
I _{PPE}	Erase Current		1,5,6,7		5	15	mA	V _{PP} =V _{PPH2}
I	V _{PP} (Page Buffer) P	rogram	1,6,7		2	5	μΑ	V _{PP} =V _{PPH1}
I _{PPWS}	Suspend Current		1,6,7		10	200	μΑ	V _{PP} =V _{PPH2}
Inne	V _{PP} Block Erase Sus	spend Current	1,6,7		2	5	μA	V _{PP} =V _{PPH1}
I _{PPES}	v pp block Elase Su	spena Current	1,6,7		10	200	μΑ	V _{PP} =V _{PPH2}

		V _{CC} =2	2.7V-3.6V	7			
Symbol	Parameter	Notes	Min.	Тур.	Max.	Unit	Test Conditions
V _{IL}	Input Low Voltage	5	-0.4		0.4	V	
V _{IH}	Input High Voltage	5	2.4		V _{CCQ} + 0.4	V	
V _{OL}	Output Low Voltage	5			0.2	V	V _{CC} =V _{CC} Min., V _{CCQ} =V _{CCQ} Min., I _{OL} =100µA
V _{OH}	Output High Voltage	5	V _{CCQ} -0.2			V	V _{CC} =V _{CC} Min., V _{CCQ} =V _{CCQ} Min., I _{OH} =-100µA
V _{PPLK}	V _{PP} Lockout during Normal Operations	3,5,6			0.4	V	
V _{PPH1}	V _{PP} during Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program Operations	6	1.65	3.0	3.6	V	
V _{PPH2}	V _{PP} during Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program Operations		11.7	12	12.3	V	
V _{LKO}	V _{CC} Lockout Voltage		1.5			V	

DC Characteristics (Continued)

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values are the reference values at V_{CC}=3.0V and T_A=+25°C unless V_{CC} is specified.

2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or (page buffer) program is executed while in block erase suspend mode, the device's current draw is the sum of I_{CCES} and I_{CCR} or I_{CCW}. If read is executed while in (page buffer) program suspend mode, the device's current draw is the sum of I_{CCWS} and I_{CCR} . 3. Block erase, full chip erase, (page buffer) program and OTP program are inhibited when $V_{PP} \leq V_{PPLK}$, and not guaranteed

in the range between V_{PPLK}(max.) and V_{PPH1}(min.), between V_{PPH1}(max.) and V_{PPH2}(min.) and above V_{PPH2}(max.).

4. The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings (t_{AVOV}) provide new data when addresses are changed.

5. Sampled, not 100% tested.

6. V_{PP} is not used for power supply pin. With V_{PP}≤V_{PPLK}, block erase, full chip erase, (page buffer) program and OTP program cannot be executed and should not be attempted.

Applying 12V±0.3V to V_{PP} provides fast erasing or fast programming mode. In this mode, V_{PP} is power supply pin and supplies the memory cell current for block erasing and (page buffer) programming. Use similar power supply trace widths and layout considerations given to the V_{CC} power bus.

Applying 12V±0.3V to V_{PP} during erase/program can only be done for a maximum of 1,000 cycles on each block. V_{PP} may be connected to $12V\pm0.3V$ for a total of 80 hours maximum.

7. The operating current in dual work is the sum of the operating current (read, erase, program) in each plane.

1.2.4 AC Characteristics - Read-Only Operations⁽¹⁾

Symbol	Parameter	Notes	Min.	Max.	Unit
t _{AVAV}	Read Cycle Time		60		ns
t _{AVQV}	Address to Output Delay			60	ns
t _{ELQV}	CE# to Output Delay	3		60	ns
t _{APA}	Page Address Access Time			25	ns
t _{GLQV}	OE# to Output Delay	3		20	ns
t _{PHQV}	RST# High to Output Delay			150	ns
t _{EHQZ} , t _{GHQZ}	CE# or OE# to Output in High Z, Whichever Occurs First	2		20	ns
t _{ELQX}	CE# to Output in Low Z	2	0		ns
t _{GLQX}	OE# to Output in Low Z	2	0		ns
t _{OH}	Output Hold from First Occurring Address, CE# or OE# change	2	0		ns
t _{AVEL} , t _{AVGL}	Address Setup to CE#, OE# Going Low for Reading Status Register	4, 6	10		ns
t _{ELAX} , t _{GLAX}	Address Hold from CE#, OE# Going Low for Reading Status Register	5, 6	30		ns
t _{EHEL} , t _{GHGL}	CE#, OE# Pulse Width High for Reading Status Register	6	15		ns

V_{CC} =2.7V-3.6V, T_{A} =-40°C to +85°C, C_{L} =30pF

NOTES: Refer to NOTE 1 through NOTE 6 on next page.

Symbol	Parameter	Notes	Min.	Max.	Unit
t _{AVAV}	Read Cycle Time		65		ns
t _{AVQV}	Address to Output Delay			65	ns
t _{ELQV}	CE# to Output Delay	3		65	ns
t _{APA}	Page Address Access Time			25	ns
t _{GLQV}	OE# to Output Delay	3		20	ns
t _{PHQV}	RST# High to Output Delay			150	ns
t _{EHQZ} , t _{GHQZ}	CE# or OE# to Output in High Z, Whichever Occurs First	2		20	ns
t _{ELQX}	CE# to Output in Low Z	2	0		ns
t _{GLQX}	OE# to Output in Low Z	2	0		ns
t _{OH}	Output Hold from First Occurring Address, CE# or OE# change	2	0		ns
t _{AVEL} , t _{AVGL}	Address Setup to CE#, OE# Going Low for Reading Status Register	4,6	10		ns
t _{ELAX} , t _{GLAX}	Address Hold from CE#, OE# Going Low for Reading Status Register	5, 6	30		ns
t _{EHEL} , t _{GHGL}	CE#, OE# Pulse Width High for Reading Status Register 6 15				ns

$V_{CC}\!\!=\!\!2.7V\!\!\cdot\!\!3.6V\!,\,T_{A}\!\!=\!\!-40^{\circ}C$ to $+85^{\circ}C,\,C_{L}\!\!=\!\!50pF$

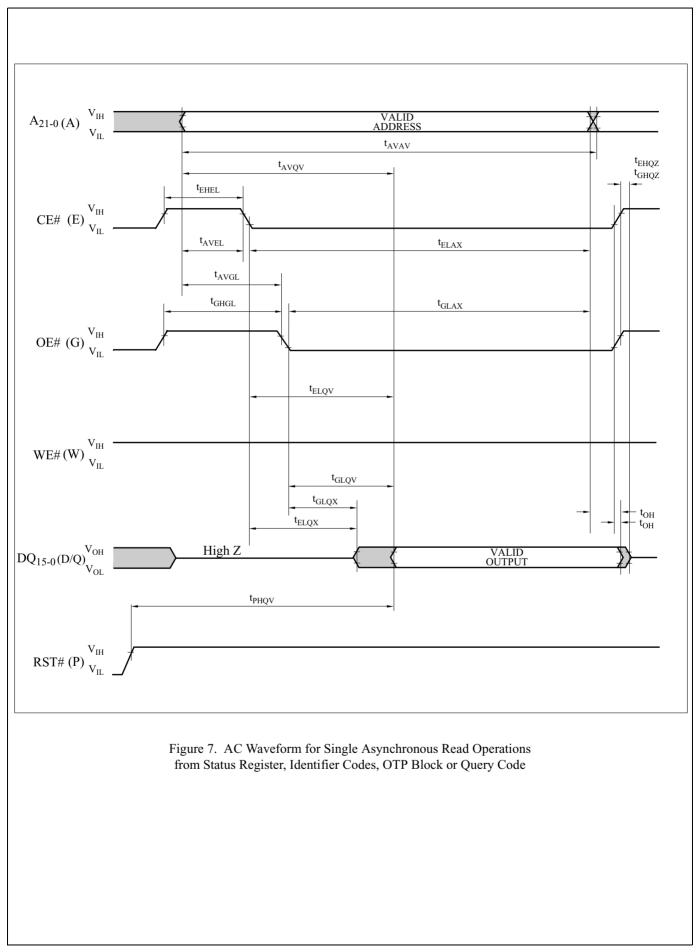
Symbol	Parameter	Notes	Min.	Max.	Unit
t _{AVAV}	Read Cycle Time 70		70		ns
t _{AVQV}	Address to Output Delay			70	ns
t _{ELQV}	CE# to Output Delay	3		70	ns
t _{APA}	Page Address Access Time			30	ns
t _{GLQV}	OE# to Output Delay	to Output Delay 3 2		25	ns
t _{PHQV}	RST# High to Output Delay			150	ns
t _{EHQZ} , t _{GHQZ}	CE# or OE# to Output in High Z, Whichever Occurs First	2		25	ns
t _{ELQX}	CE# to Output in Low Z	2	0		ns
t _{GLQX}	OE# to Output in Low Z	Z 2 0			ns
t _{OH}	Output Hold from First Occurring Address, CE# or OE# change	2	0		ns
t_{AVEL}, t_{AVGL}	Address Setup to CE#, OE# Going Low for Reading Status Register	4, 6	10		ns
$t_{\rm ELAX}, t_{\rm GLAX}$	Address Hold from CE#, OE# Going Low for Reading Status Register	5, 6	30		ns
t _{EHEL} , t _{GHGL}	CE#, OE# Pulse Width High for Reading Status Register	6	15		ns

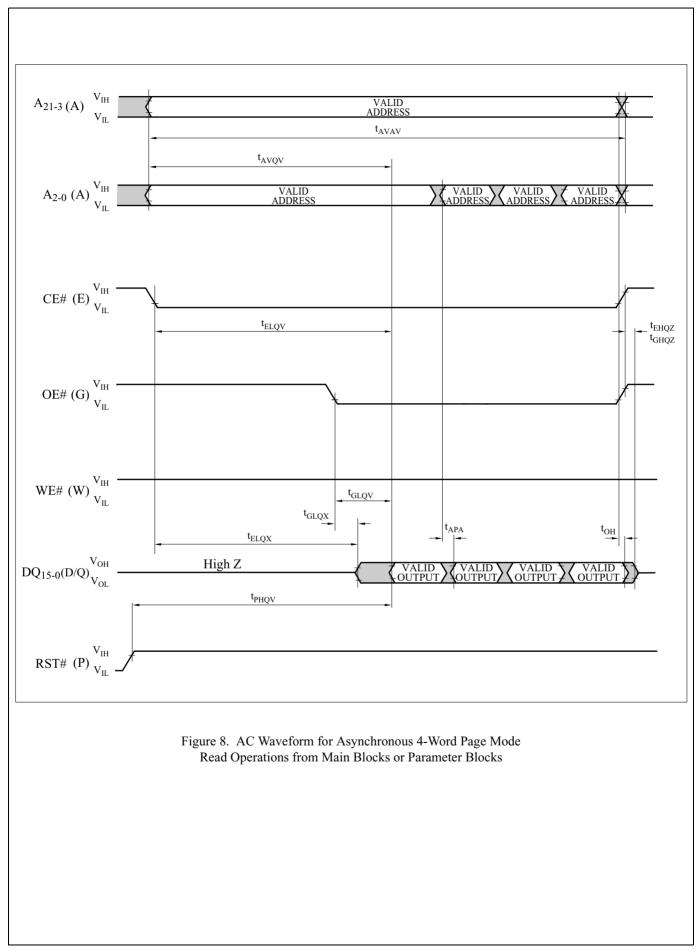
NOTES:

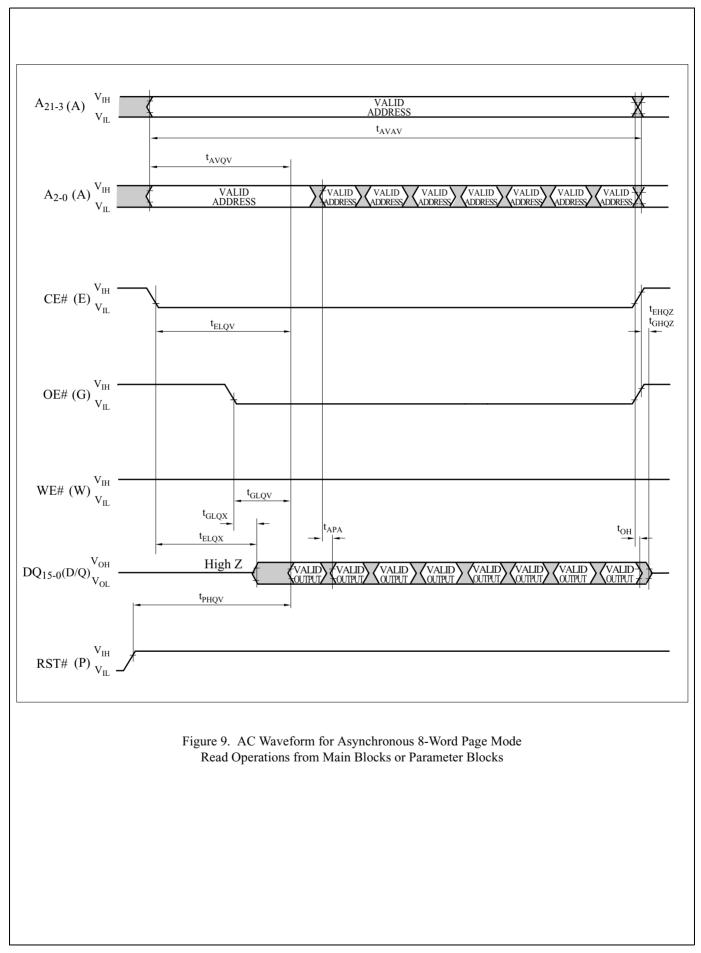
1. See AC input/output reference waveform for timing measurements and maximum allowable input slew rate.

2. Sampled, not 100% tested.

 3. OE# may be delayed up to t_{ELQV} — t_{GLQV} after the falling edge of CE# without impact to t_{ELQV}.
 4. Address setup time (t_{AVEL}, t_{AVGL}) is defined from the falling edge of CE# or OE# (whichever goes low last).
 5. Address hold time (t_{ELAX}, t_{GLAX}) is defined from the falling edge of CE# or OE# (whichever goes low last).
 6. Specifications t_{AVEL}, t_{AVGL}, t_{ELAX}, t_{GLAX} and t_{EHEL}, t_{GHGL} for read operations apply to only status register read operations. operations.







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1.2.5 AC Characteristics - Write Operations^{(1), (2)}

V _{CC} =2.7V-3.6V,	$T_A = -40^{\circ}C$ to $+85^{\circ}C$
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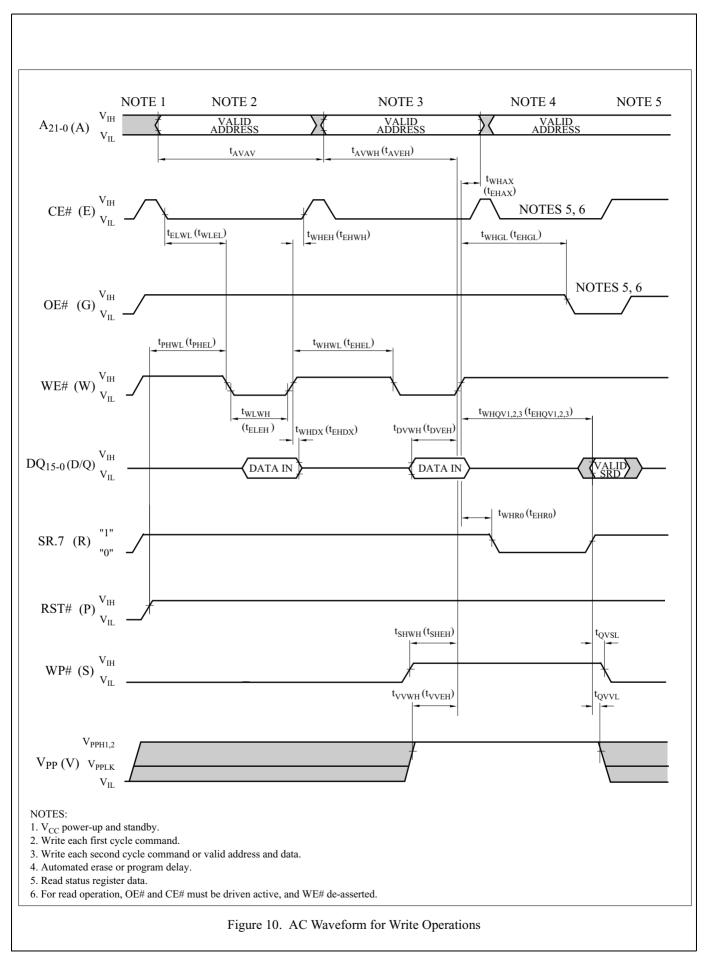
Symbol	Parameter		Notes	Min.	Max.	Unit
				60		ns
t _{AVAV}	Write Cycle Time			65		ns
				70		ns
$t_{PHWL} (t_{PHEL})$	RST# High Recovery to WE# (CE#) Goir	ig Low	3	150		ns
$t_{ELWL} (t_{WLEL})$	CE# (WE#) Setup to WE# (CE#) Going	Low		0		ns
		t _{AVAV} =60ns		45		ns
t _{WLWH} (t _{ELEH})	WE# (CE#) Pulse Width	t _{AVAV} =65ns	4, 9	50		ns
		t _{AVAV} =70ns		55		ns
t _{DVWH} (t _{DVEH})	Data Setup to WE# (CE#) Going High	•	8	40		ns
	Address Setup to WE# (CE#) Going High	t _{AVAV} =60ns		45		ns
t _{AVWH} (t _{AVEH})		t _{AVAV} =65ns	8, 9	50		ns
	mgn	t _{AVAV} =70ns		55		ns
$t_{\rm WHEH} \left(t_{\rm EHWH} \right)$	CE# (WE#) Hold from WE# (CE#) High		0		ns	
$t_{WHDX} (t_{EHDX})$	Data Hold from WE# (CE#) High			0		ns
$t_{WHAX} (t_{EHAX})$	Address Hold from WE# (CE#) High			0		ns
$t_{WHWL} (t_{EHEL})$	WE# (CE#) Pulse Width High		5	15		ns
$t_{\rm SHWH} \left(t_{\rm SHEH} \right)$	WP# High Setup to WE# (CE#) Going H	igh	3	0		ns
t _{VVWH} (t _{VVEH})	V _{PP} Setup to WE# (CE#) Going High	3	200		ns	
t _{WHGL} (t _{EHGL})	Write Recovery before Read		30		ns	
t _{QVSL}	WP# High Hold from Valid SRD	3,6	0		ns	
t _{QVVL}	V _{PP} Hold from Valid SRD	3,6	0		ns	
t _{WHR0} (t _{EHR0})	WE# (CE#) High to SR.7 Going "0"	3, 7		t_{AVQV}^+ 50	ns	

NOTES:

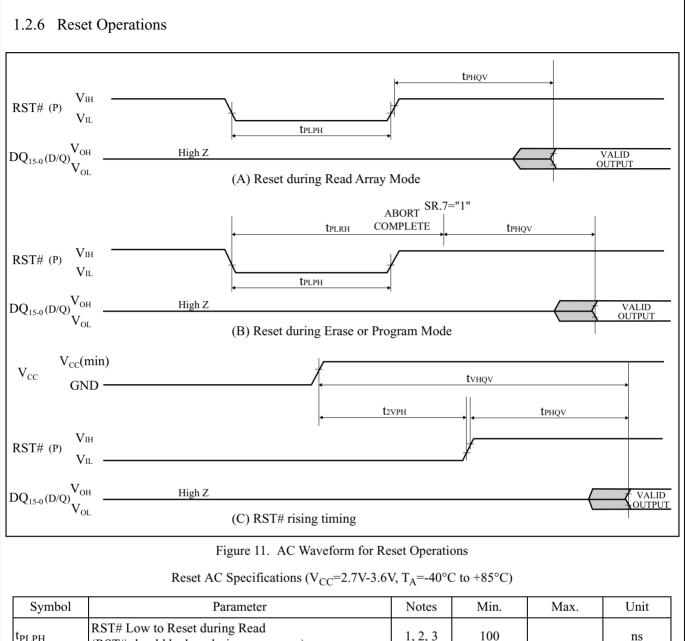
- 1. The timing characteristics for reading the status register during block erase, full chip erase, (page buffer) program and OTP program operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
- 2. A write operation can be initiated and terminated with either CE# or WE#.

3. Sampled. not 100% tested.

- 4. Write pulse width (t_{WP}) is defined from the falling edge of CE# or WE# (whichever goes low last) to the rising edge of CE# or WE# (whichever goes high first). Hence, $t_{WP}=t_{WLWH}=t_{ELEH}=t_{WLEH}=t_{ELWH}$. 5. Write pulse width high (t_{WPH}) is defined from the rising edge of CE# or WE# (whichever goes high first) to the falling
- edge of CE# or WE# (whichever goes low last). Hence, t_{WPH}=t_{WHWL}=t_{EHEL}=t_{WHEL}=t_{EHWL}.
 V_{PP} should be held at V_{PP}=V_{PPH1/2} until determination of block erase, full chip erase, (page buffer) program or OTP program success (SR.1/3/4/5=0).
- 7. t_{WHR0} (t_{EHR0}) after the Read Query or Read Identifier Codes/OTP command= t_{AVQV} +100ns.
- 8. Refer to Table 6 for valid address and data for block erase, full chip erase, (page buffer) program, OTP program or lock bit configuration.
- 9. t_{WLWH} (t_{ELEH}) and t_{AVWH} (t_{AVEH}) values vary depending on the write cycle time (t_{AVAV}).



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Symbol	Parameter	notes	IVIIII.	Iviax.	Unit
t _{PLPH}	RST# Low to Reset during Read (RST# should be low during power-up.)		100		ns
t _{PLRH}	RST# Low to Reset during Erase or Program	1, 3, 4		22	μs
t _{2VPH} V _{CC} 2.7V to RST# High		1, 3, 5	100		ns
t _{VHQV} V _{CC} 2.7V to Output Delay		3		1	ms
NOTES					

NOTES:

1. A reset time, t_{PHQV}, is required from the later of SR.7 going "1" or RST# going high until outputs are valid. Refer to AC Characteristics - Read-Only Operations for t_{PHQV}.

2. t_{PLPH} is <100ns the device may still reset but this is not guaranteed.

3. Sampled, not 100% tested.

4. If RST# asserted while a block erase, full chip erase, (page buffer) program or OTP program operation is not executing, the reset will complete within 100ns.

5. When the device power-up, holding RST# low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

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1.2.7 Block Erase, Full Chip Erase, (Page Buffer) Program and OTP Program Performa	$nce^{(3)}$)
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V _{CC} -2.7V-5.6V, 1 _A 40 C to +85 C										
Symbol	Parameter	Notes	Page Buffer Command is Used or not		PP=VPPI n Systen			PP=VPPI /lanufactu		Unit
			Used	Min.	Тур. ⁽¹⁾	Max. ⁽²⁾	Min.	Тур. ⁽¹⁾	Max. ⁽²⁾	
tum	4K-Word Parameter Block	2	Not Used		0.05	0.3		0.04	0.12	S
t _{WPB}	Program Time	2	Used		0.03	0.12		0.02	0.06	S
tun m	32K-Word Main Block	2	Not Used		0.38	2.4		0.31	1.0	S
t _{WMB}	Program Time	2	Used		0.24	1.0		0.17	0.5	S
t _{WHQV1} /	Word Program Time	2	Not Used		11	200		9	185	μs
t _{EHQV1}		2	Used		7	100		5	90	μs
t _{WHOV1} / t _{EHOV1}	OTP Program Time	2	Not Used		36	400		27	185	μs
t _{WHQV2} / t _{EHQV2}	4K-Word Parameter Block Erase Time	2	-		0.3	4		0.2	4	s
t _{WHQV3} / t _{EHQV3}	32K-Word Main Block Erase Time	2	-		0.6	5		0.5	5	s
	Full Chip Erase Time	2			80	700		65	700	s
t _{WHRH1} / t _{EHRH1}	(Page Buffer) Program Suspend Latency Time to Read	4	-		5	10		5	10	μs
t _{WHRH2} / t _{EHRH2}	Block Erase Suspend Latency Time to Read	4	-		5	20		5	20	μs
t _{ERES}	Latency Time from Block Erase Resume Command to Block Erase Suspend Command	5	-	500			500			μs

 $V_{CC}=2.7V-3.6V$, $T_{A}=-40^{\circ}C$ to $+85^{\circ}C$

NOTES:

1. Typical values measured at V_{CC} =3.0V, V_{PP} =3.0V or 12V, and T_A =+25°C. Assumes corresponding lock bits are not set. Subject to change based on device characterization.

2. Excludes external system-level overhead.

3. Sampled, but not 100% tested.

4. A latency time is required from writing suspend command (WE# or CE# going high) until SR.7 going "1".

5. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than t_{ERES} and its sequence is repeated, the block erase operation may not be finished.

2 Related Document Information⁽¹⁾

Document No.	Document Name
FUM00701	LH28F640BF series Appendix

NOTE:

1. International customers should contact their local SHARP or distribution sales offices.

LH28F640BFXX-XXXXXX Flash MEMORY ERRATA

1. AC Characteristics

PROBLEM

The table below summarizes the AC characteristics.

AC Characteristics - Write Operations

Page	Symbol	Parameter		Min.	Max.	Unit
				75		ns
26	t _{AVAV}	Write Cycle Time	Write Cycle Time			ns
				75		ns
			t _{AVAV} =75ns	50		ns
26	$t_{WLWH}(t_{ELEH})$	WE# (CE#) Pulse Width	t _{AVAV} =75ns	50		ns
			t _{AVAV} =75ns	50		ns
26	t_{WHWL} (t_{EHEL})	WE# (CE#) Pulse Width High		25		ns

V_{CC}=2.7V-3.6V

WORKAROUND

System designers should consider these specifications.

STATUS

This is intended to be fixed in future devices.

A-1 RECOMMENDED OPERATING CONDITIONS

A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

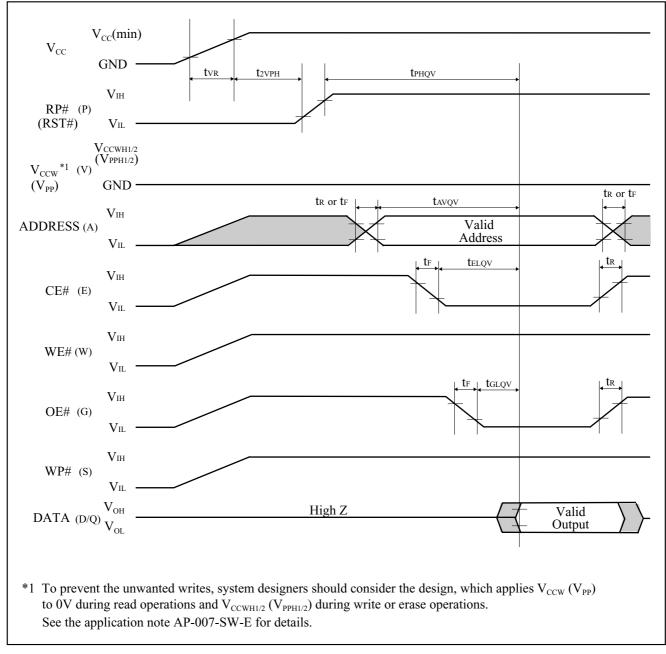


Figure A-1. AC Timing at Device Power-Up

For the AC specifications t_{VR} , t_R , t_F in the figure, refer to the next page. See the "ELECTRICAL SPECIFICATIONS" described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

A-1.1.1 Rise and Fall Time

Symbol	Parameter		Min.	Max.	Unit
t _{VR}	V _{CC} Rise Time		0.5	30000	μs/V
t _R	Input Signal Rise Time			1	μs/V
t _F	Input Signal Fall Time			1	μs/V

NOTES:

1. Sampled, not 100% tested.

2. This specification is applied for not only the device power-up but also the normal operations.

A-1.2 Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

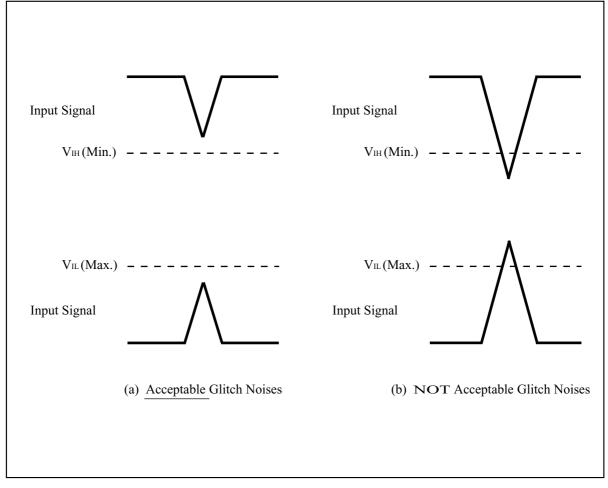


Figure A-2. Waveform for Glitch Noises

See the "DC CHARACTERISTICS" described in specifications for V_{IH} (Min.) and V_{IL} (Max.).

A-2 RELATED DOCUMENT INFORMATION⁽¹⁾

Document No.	Document Name	
AP-001-SD-E	Flash Memory Family Software Drivers	
АР-006-РТ-Е	Data Protection Method of SHARP Flash Memory	
AP-007-SW-E	RP#, V _{PP} Electric Potential Switching Circuit	

NOTE:

1. International customers should contact their local SHARP or distribution sales office.

A-3 STATUS REGISTER READ OPERATIONS

If AC timing for reading the status register described in specifications is not satisfied, a system processor can check the status register bit SR.15 instead of SR.7 to determine when the erase or program operation has been completed.

	NOTES:
SR.15 = WRITE STATE MACHINE STATUS: (DQ ₁₅) 1 = Ready in All Partitions 0 = Busy in Any Partition	SR.15 indicates the status of WSM (Write State Machine). If SR.15="0", erase or program operation is in progress in any partition.
 SR.7 = WRITE STATE MACHINE STATUS FOR EACH PARTITION: (DQ₇) 1 = Ready in the Addressed Partition 0 = Busy in the Addressed Partition 	SR.7 indicates the status of the partition. If SR.7="0", erase or program operation is in progress in the addressed partition. Even if the SR.7 is "1", the WSM may be occupied by the other partition.

Table A-3-1. Status Register Definition (SR.15 and SR.7)

