PRELIMINARY PRODUCT SPECIFICATIONS

SHARP®

Integrated Circuits Group

LH28F320BFN-PTTLZJ

Flash Memory

32M (2M × 16)

(Model No.: LHF32FDH)

Spec No.: FM024004

Issue Date: April 1, 2002

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- Please direct all queries regarding the products covered herein to a sales representative of the company.

CONTENTS

LH28F320BFN-PTTLZJ
32Mbit (2Mbit×16)
Page Mode Flash MEMORY

- 32M density with 16Bit I/O Interface
- High Performance Reads
  - 70/25ns 8-Word Page Mode
- Low Power Operation
  - 2.7V Read and Write Operations
  - Automatic Power Savings Mode Reduces I_{CCR} in Static Mode
- Enhanced Code + Data Storage
  - 5µs Typical Erase/Program Suspends
- OTP (One Time Program) Block
  - 4-Word Factory-Programmed Area
  - 4-Word User-Programmable Area
- High Performance Program with Page Buffer
  - 16-Word Page Buffer
- Operating Temperature 0°C to +70°C
- Flexible Blocking Architecture
  - Eight 4K-word Parameter Blocks
  - Sixty-three 32K-word Main Blocks
  - Top Parameter Location
- CMOS Process (P-type silicon substrate)
- Enhanced Data Protection Features
  - Individual Block Lock and Block Lock-Down with Zero-Latency
  - All blocks are locked at power-up or device reset.
  - Block Erase, Full Chip Erase, (Page Buffer) Word Program Lockout during Power Transitions
- Automated Erase/Program Algorithms
  - 3.0V Low-Power 11µs/Word (Typ.) Programming
- Cross-Compatible Command Support
  - Basic Command Set
  - Common Flash Interface (CFI)
- Extended Cycling Capability
  - Minimum 100,000 Block Erase Cycles
- 44-Lead SOP
- ETOX™* Flash Technology
- Not designed or rated as radiation hardened

The product, which is Page Mode Flash memory, is a low power, high density, low cost, nonvolatile read/write storage solution for a wide range of applications. The product can operate at V_{CC}=2.7V-3.6V. Its low voltage operation capability greatly extends battery life for portable applications.

The product provides high performance asynchronous page mode. It allows code execution directly from Flash, thus eliminating time consuming wait states.

The memory array block architecture utilizes Enhanced Data Protection features, and provides separate Parameter and Main Blocks that provide maximum flexibility for safe nonvolatile code and data storage.

Fast program capability is provided through the use of high speed Page Buffer Program.

Special OTP (One Time Program) block provides an area to store permanent code such as a unique number.

* ETOX is a trademark of Intel Corporation.

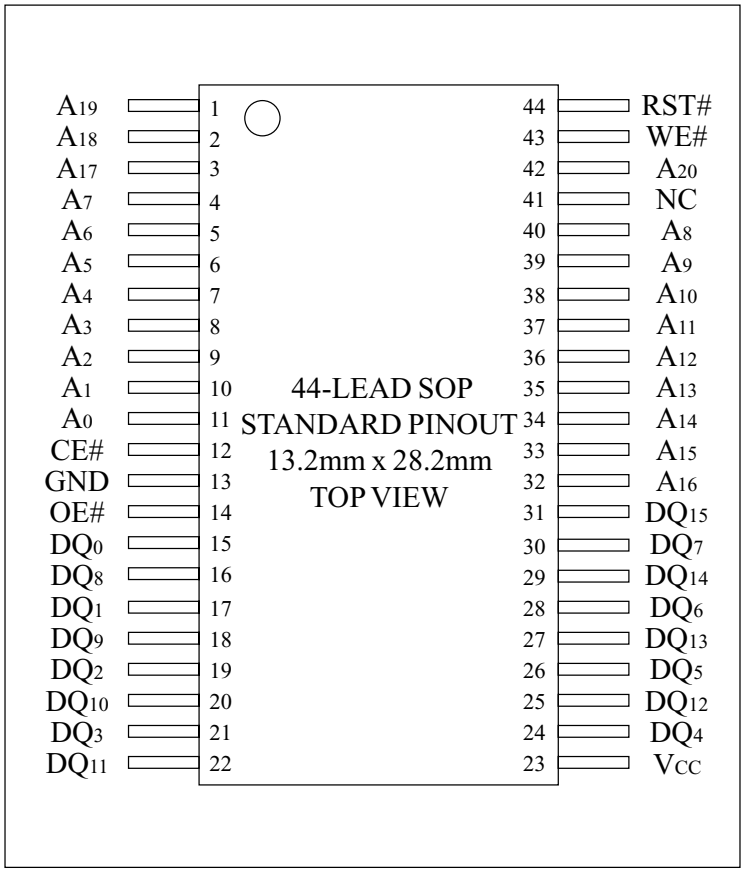


Figure 1. 44-Lead SOP Pinout

Table 1. Pin Descriptions

Symbol	Type	Name and Function
A_0-A_{20}	INPUT	ADDRESS INPUTS: Inputs for addresses. 32M: A_0-A_{20}
DQ_0-DQ_{15}	INPUT/ OUTPUT	DATA INPUTS/OUTPUTS: Inputs data and commands during CUI (Command User Interface) write cycles, outputs data during memory array, status register, query code and identifier code reads. Data pins float to high-impedance (High Z) when the chip or outputs are deselected. Data is internally latched during an erase or program cycle.
CE#	INPUT	CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. CE#-high (V_{IH}) deselects the device and reduces power consumption to standby levels.
RST#	INPUT	RESET: When low (V_{IL}), RST# resets internal automation and inhibits write operations which provides data protection. RST#-high (V_{IH}) enables normal operation. After power-up or reset mode, the device is automatically set to read array mode. RST# must be low during power-up/down.
OE#	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
WE#	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of CE# or WE# (whichever goes high first).
V_{CC}	SUPPLY	DEVICE POWER SUPPLY (2.7V-3.6V): With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see DC Characteristics) produce spurious results and should not be attempted.
GND	SUPPLY	GROUND: Do not float any ground pins.
NC		NO CONNECT: Lead is not internally connected; it may be driven or floated.

BLOCK NUMBER		ADDRESS RANGE
70	4K-WORD	1FF000H - 1FFFFFH
69	4K-WORD	1FE000H - 1FEFFFH
68	4K-WORD	1FD000H - 1FDFFFH
67	4K-WORD	1FC000H - 1FCFFFH
66	4K-WORD	1FB000H - 1FBFFFH
65	4K-WORD	1FA000H - 1FAFFFH
64	4K-WORD	1F9000H - 1F9FFFH
63	4K-WORD	1F8000H - 1F8FFFH
62	32K-WORD	1F0000H - 1F7FFFH
61	32K-WORD	1E8000H - 1EFFFFH
60	32K-WORD	1E0000H - 1E7FFFH
59	32K-WORD	1D8000H - 1DFFFFH
58	32K-WORD	1D0000H - 1D7FFFH
57	32K-WORD	1C8000H - 1CFFFFH
56	32K-WORD	1C0000H - 1C7FFFH
55	32K-WORD	1B8000H - 1BFFFFH
54	32K-WORD	1B0000H - 1B7FFFH
53	32K-WORD	1A8000H - 1AFFFFH
52	32K-WORD	1A0000H - 1A7FFFH
51	32K-WORD	198000H - 19FFFFH
50	32K-WORD	190000H - 197FFFH
49	32K-WORD	188000H - 18FFFFH
48	32K-WORD	180000H - 187FFFH
47	32K-WORD	178000H - 17FFFFH
46	32K-WORD	170000H - 177FFFH
45	32K-WORD	168000H - 16FFFFH
44	32K-WORD	160000H - 167FFFH
43	32K-WORD	158000H - 15FFFFH
42	32K-WORD	150000H - 157FFFH
41	32K-WORD	148000H - 14FFFFH
40	32K-WORD	140000H - 147FFFH
39	32K-WORD	138000H - 13FFFFH
38	32K-WORD	130000H - 137FFFH
37	32K-WORD	128000H - 12FFFFH
36	32K-WORD	120000H - 127FFFH
35	32K-WORD	118000H - 11FFFFH
34	32K-WORD	110000H - 117FFFH
33	32K-WORD	108000H - 10FFFFH
32	32K-WORD	100000H - 107FFFH

BLOCK NUMBER		ADDRESS RANGE
31	32K-WORD	0F8000H - 0FFFFFH
30	32K-WORD	0F0000H - 0F7FFFH
29	32K-WORD	0E8000H - 0EFFFFH
28	32K-WORD	0E0000H - 0E7FFFH
27	32K-WORD	0D8000H - 0DFFFFH
26	32K-WORD	0D0000H - 0D7FFFH
25	32K-WORD	0C8000H - 0CFFFFH
24	32K-WORD	0C0000H - 0C7FFFH
23	32K-WORD	0B8000H - 0BFFFFH
22	32K-WORD	0B0000H - 0B7FFFH
21	32K-WORD	0A8000H - 0AFFFFH
20	32K-WORD	0A0000H - 0A7FFFH
19	32K-WORD	098000H - 09FFFFH
18	32K-WORD	090000H - 097FFFH
17	32K-WORD	088000H - 08FFFFH
16	32K-WORD	080000H - 087FFFH
15	32K-WORD	078000H - 07FFFFH
14	32K-WORD	070000H - 077FFFH
13	32K-WORD	068000H - 06FFFFH
12	32K-WORD	060000H - 067FFFH
11	32K-WORD	058000H - 05FFFFH
10	32K-WORD	050000H - 057FFFH
9	32K-WORD	048000H - 04FFFFH
8	32K-WORD	040000H - 047FFFH
7	32K-WORD	038000H - 03FFFFH
6	32K-WORD	030000H - 037FFFH
5	32K-WORD	028000H - 02FFFFH
4	32K-WORD	020000H - 027FFFH
3	32K-WORD	018000H - 01FFFFH
2	32K-WORD	010000H - 017FFFH
1	32K-WORD	008000H - 00FFFFH
0	32K-WORD	000000H - 007FFFH

Figure 2. Memory Map (Top Parameter)

Table 2. Identifier Codes and OTP Address for Read Operation

	Code	Address [A_{20}-A_0]	Data [DQ_{15}-DQ_0]	Notes
Manufacturer Code	Manufacturer Code	000000H	00B0H	
Device Code	Top Parameter Device Code	000001H	00B4H	1
Block Lock Configuration Code	Block is Unlocked	Block Address + 2	DQ_0 = 0	2
	Block is Locked		DQ_0 = 1	2
	Block is not Locked-Down	Block Address + 2	DQ_1 = 0	2
	Block is Locked-Down		DQ_1 = 1	2
OTP	OTP Lock	000080H	OTP-LK	3
	OTP	000081-000088H	OTP	4

NOTES:
1. Top parameter device has its parameter blocks at the highest address.
2. DQ_{15}-DQ_2 are reserved for future implementation.
3. OTP-LK=OTP Block Lock configuration.
4. OTP=OTP Block data.

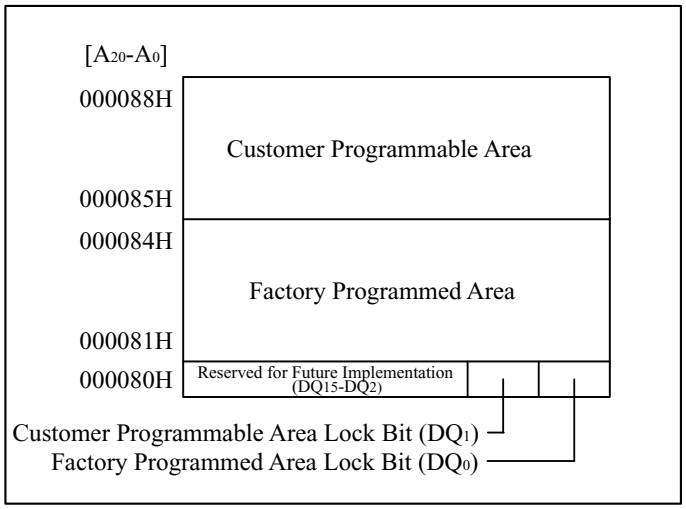


Figure 3. OTP Block Address Map for OTP Program
(The area outside 80H~88H cannot be used.)

Table 3. Bus Operation[1, 2]

Mode	Notes	RST#	CE#	OE#	WE#	Address	DQ_{0-15}
Read Array	6	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	High Z
Standby		V_{IH}	V_{IH}	X	X	X	High Z
Reset	3	V_{IL}	X	X	X	X	High Z
Read Identifier Codes/OTP	6	V_{IH}	V_{IL}	V_{IL}	V_{IH}	See Table 2	See Table 2
Read Query	6,7	V_{IH}	V_{IL}	V_{IL}	V_{IH}	See Appendix	See Appendix
Write	4,5,6	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}

NOTES:
1. See DC Characteristics for V_{IL} or V_{IH} voltages.
2. X can be V_{IL} or V_{IH} for control pins and addresses.
3. RST# at GND±0.2V ensures the lowest power consumption.
4. Command writes involving block erase, full chip erase, (page buffer) program or OTP program are reliably executed when V_{CC}=2.7V-3.6V.
5. Refer to Table 4 for valid D_{IN} during a write operation.
6. Never hold OE# low and WE# low at the same timing.
7. Refer to Appendix of LH28F320BF series for more information about query code.

Table 4. Command Definitions(10)

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Oper(1)	Addr(2)	Data(3)	Oper(1)	Addr(2)	Data(3)
Read Array	1	2	Write	X	FFH			
Read Identifier Codes/OTP	≥ 2	2,3,4	Write	X	90H	Read	IA or OA	ID or OD
Read Query	≥ 2	2,3,4	Write	X	98H	Read	QA	QD
Read Status Register	2	2,3,11	Write	BA or WA	70H	Read	BA or WA	SRD
Clear Status Register	1	2	Write	X	50H			
Block Erase	2	2,3,5	Write	BA	20H	Write	BA	D0H
Full Chip Erase	2	2,5,8	Write	X	30H	Write	X	D0H
Program	2	2,3,5,6	Write	WA	40H or 10H	Write	WA	WD
Page Buffer Program	≥ 4	2,3,5,7	Write	WA	E8H	Write	WA	N-1
Block Erase and (Page Buffer) Program Suspend	1	2,8	Write	BA or WA	B0H			
Block Erase and (Page Buffer) Program Resume	1	2,8	Write	BA or WA	D0H			
Set Block Lock Bit	2	2	Write	BA	60H	Write	BA	01H
Clear Block Lock Bit	2	2,9	Write	BA	60H	Write	BA	D0H
Set Block Lock-down Bit	2	2	Write	BA	60H	Write	BA	2FH
OTP Program	2	2,3,8	Write	OA	C0H	Write	OA	OD

NOTES:

1. Bus operations are defined in Table 3.
2. The address which is written at the first bus cycle should be the same as the address which is written at the second bus cycle.
   X=Any valid address within the device.
   IA=Identifier codes address (See Table 2).
   QA=Query codes address. Refer to Appendix of LH28F320BF series for details.
   BA=Address within the block being erased, set/cleared block lock bit or set block lock-down bit.
   WA=Address of memory location for the Program command or the first address for the Page Buffer Program command.
   OA=Address of OTP block to be read or programmed (See Figure 3).
3. ID=Data read from identifier codes. (See Table 2).
   QD=Data read from query database. Refer to Appendix of LH28F320BF series for details.
   SRD=Data read from status register. See Table 7 and Table 8 for a description of the status register bits.
   WD=Data to be programmed at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).
   OD=Data to be programmed at location OA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).
   N-1=N is the number of the words to be loaded into a page buffer.
4. Following the Read Identifier Codes/OTP command, read operations access manufacturer code, device code, block lock configuration code, and the data within OTP block (See Table 2).
   The Read Query command is available for reading CFI (Common Flash Interface) information.
5. Block erase, full chip erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when RST# is V_{IH}.
6. Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.
7. Following the third bus cycle, inputs the program sequential address and write data of "N" times. Finally, input the any valid address within the target block to be programmed and the confirm command (D0H). Refer to Appendix of LH28F320BF series for details.
8. Full chip erase and OTP program operations can not be suspended. The OTP Program command can not be accepted

while the block erase operation is being suspended.
9. Following the Clear Block Lock Bit command, the selected block is unlocked regardless of lock-down configuration.
10. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.
11. When the status register data is read, input the address to which the erase or program operation is executed.

Table 5. Functions of Block Lock[4] and Block Lock-Down

Current State				Erase/Program Allowed [2]
State	DQ_1[1]	DQ_0[1]	State Name	
[00]	0	0	Unlocked	Yes
[01][3]	0	1	Locked	No
[10]	1	0	Unlocked	Yes
[11]	1	1	Locked	No

NOTES:
1. DQ_0=1: a block is locked; DQ_0=0: a block is unlocked.
   DQ_1=1: a block is locked-down; DQ_1=0: a block is not locked-down.
2. Erase and program are general terms, respectively, to express: block erase, full chip erase and (page buffer) program operations.
3. At power-up or device reset, all blocks default to locked state and are not locked-down, that is, [01] regardless of the states before power-off or reset operation.
4. OTP (One Time Program) block has the lock function which is different from those described above.

Table 6. Block Locking State Transitions upon Command Write

Current State			Result after Lock Command Written (Next State)		
State	DQ_1	DQ_0	Set Lock[1]	Clear Lock[1]	Set Lock-down[1]
[00]	0	0	[01]	No Change[3]	[11][2]
[01]	0	1	No Change	[00]	[11]
[10]	1	0	[11]	No Change	[11][2]
[11]	1	1	No Change	[10]	No Change

NOTES:
1. "Set Lock" means Set Block Lock Bit command, "Clear Lock" means Clear Block Lock Bit command and "Set Lock-down" means Set Block Lock-Down Bit command.
2. When the Set Block Lock-Down Bit command is written to the unlocked block (DQ_0=0), the corresponding block is locked-down and automatically locked at the same time.
3. "No Change" means that the state remains unchanged after the command written.

Table 7. Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
WSMS	BESS	BEFCES	PBPOPS	R	PBPSS	DPS	R
7	6	5	4	3	2	1	0

SR.15 - SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R)

SR.7 = WRITE STATE MACHINE STATUS (WSMS)
1 = Ready
0 = Busy

SR.6 = BLOCK ERASE SUSPEND STATUS (BESS)
1 = Block Erase Suspended
0 = Block Erase in Progress/Completed

SR.5 = BLOCK ERASE AND FULL CHIP ERASE STATUS (BEFCES)
1 = Error in Block Erase or Full Chip Erase
0 = Successful Block Erase or Full Chip Erase

SR.4 = (PAGE BUFFER) PROGRAM AND OTP PROGRAM STATUS (PBPOPS)
1 = Error in (Page Buffer) Program or OTP Program
0 = Successful (Page Buffer) Program or OTP Program

SR.3 = RESERVED FOR FUTURE ENHANCEMENTS (R)

SR.2 = (PAGE BUFFER) PROGRAM SUSPEND STATUS (PBPSS)
1 = (Page Buffer) Program Suspended
0 = (Page Buffer) Program in Progress/Completed

SR.1 = DEVICE PROTECT STATUS (DPS)
1 = Erase or Program Attempted on a Locked Block, Operation Abort
0 = Unlocked

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

NOTES:

Check SR.7 to determine block erase, full chip erase, (page buffer) program or OTP program completion. SR.6 - SR.1 are invalid while SR.7="0".

If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, page buffer program, set/clear block lock bit, set block lock-down bit, attempt, an improper command sequence was entered.

SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes/OTP command indicates block lock bit status.

SR.15 - SR.8, SR.3 and SR.0 are reserved for future use and should be masked out when polling the status register.

Table 8. Extended Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

XSR.15-8 = RESERVED FOR FUTURE ENHANCEMENTS (R)

XSR.7 = STATE MACHINE STATUS (SMS)
1 = Page Buffer Program available
0 = Page Buffer Program not available

XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

NOTES:

After issue a Page Buffer Program command (E8H), XSR.7="1" indicates that the entered command is accepted. If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not.

XSR.15-8 and XSR.6-0 are reserved for future use and should be masked out when polling the extended status register.

1 Electrical Specifications

1.1 Absolute Maximum Ratings*

Operating Temperature

During Read, Erase and Program ..... 0°C to +70°C (1)

Storage Temperature

During under Bias..... -10°C to +80°C

During non Bias..... -65°C to +125°C

Voltage On Any Pin

(except V_{CC})..... -0.5V to V_{CC}+0.5V (2)

V_{CC} Supply Voltage ..... -0.2V to +3.9V (2)

Output Short Circuit Current..... 100mA (3)

**WARNING:* Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTES:

1. Operating temperature is for commercial temperature product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC} pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins and V_{CC} is V_{CC}+0.5V which, during transitions, may overshoot to V_{CC} +2.0V for periods <20ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

1.2 Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Temperature	T_A	0	+25	+70	°C	
V_{CC} Supply Voltage	V_{CC}	2.7	3.0	3.6	V	1
Main Block Erase Cycling		100,000			Cycles	
Parameter Block Erase Cycling		100,000			Cycles	

NOTES:

1. See DC Characteristics tables for voltage range-specific specification.

1.2.1 Capacitance(1) (T_A=+25°C, f=1MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0.0V		4	7	pF
RST# Input Capacitance	C_{IN}	V_{IN}=0.0V		20	28	pF
Output Capacitance	C_{OUT}	V_{OUT}=0.0V		6	10	pF

NOTE:
1. Sampled, not 100% tested.

1.2.2 AC Input/Output Test Conditions

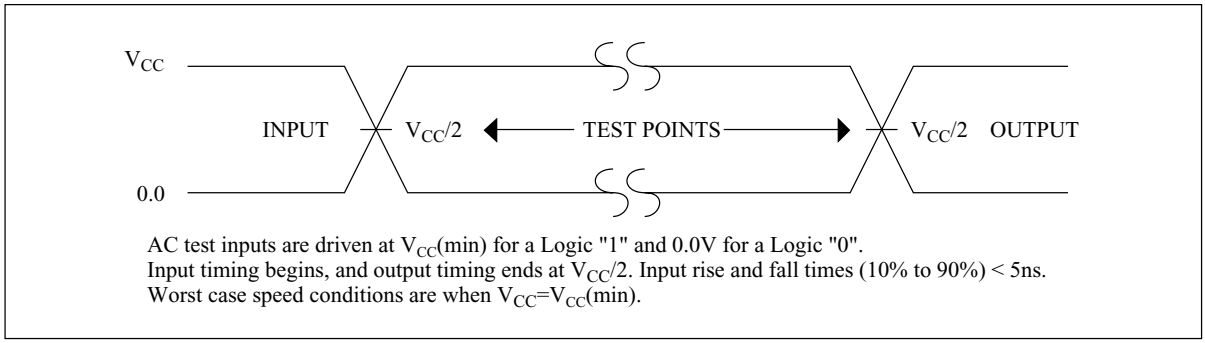


Figure 4. Transient Input/Output Reference Waveform for V_{CC}=2.7V-3.6V

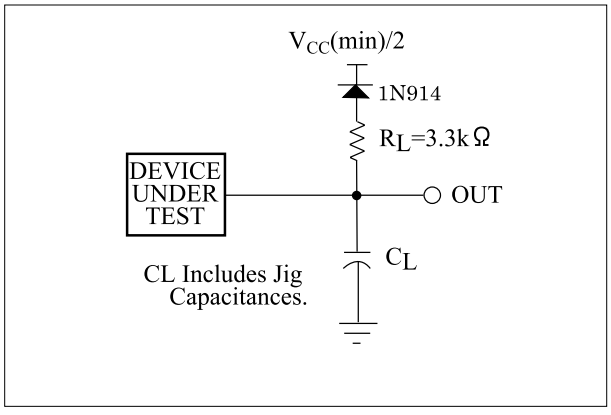


Figure 5. Transient Equivalent Testing Load Circuit

Table 9. Configuration Capacitance Loading Value

Test Configuration	C_L (pF)
V_{CC}=2.7V-3.6V	50

1.2.3 DC Characteristics

V_{CC}=2.7V-3.6V

Symbol	Parameter		Notes	Min.	Typ.	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	-1.0		+1.0	µA	V_{CC}=V_{CC}Max., V_{IN}/V_{OUT}=V_{CC} or GND
I_{LO}	Output Leakage Current		1	-1.0		+1.0	µA	
I_{CCS}	V_{CC} Standby Current		1		6	25	µA	V_{CC}=V_{CC}Max., CE#=RST#= V_{CC}±0.2V
I_{CCAS}	V_{CC} Automatic Power Savings Current		1,4		4	20	µA	V_{CC}=V_{CC}Max., CE#=GND±0.2V
I_{CCD}	V_{CC} Reset Power-Down Current		1		4	20	µA	RST#=GND±0.2V
I_{CCR}	Average V_{CC} Read Current Normal Mode		1		15	25	mA	V_{CC}=V_{CC}Max., CE#=V_{IL}, OE#=V_{IH}, f=5MHz
	Average V_{CC} Read Current Page Mode	8 Word Read	1		5	10	mA	
I_{CCW}	V_{CC} (Page Buffer) Program Current		1,5		20	60	mA	
I_{CCE}	V_{CC} Block Erase, Full Chip Erase Current		1,5		10	30	mA	
I_{CCWS} I_{CCES}	V_{CC} (Page Buffer) Program or Block Erase Suspend Current		1,2		15	210	µA	CE#=V_{IH}
V_{IL}	Input Low Voltage		5	-0.4		0.4	V	
V_{IH}	Input High Voltage		5	V_{CC} -0.4		V_{CC} + 0.4	V	
V_{OL}	Output Low Voltage		5			0.2	V	V_{CC}=V_{CC}Min., I_{OL}=100µA
V_{OH}	Output High Voltage		5	V_{CC} -0.2			V	V_{CC}=V_{CC}Min., I_{OH}=-100µA
V_{LKO}	V_{CC} Lockout Voltage		3	1.5			V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values are the reference values at V_{CC}=3.0V and T_A=+25°C unless V_{CC} is specified.
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or (page buffer) program while in block erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
3. Block erase, full chip erase, (page buffer) program and OTP program are inhibited when V_{CC}≤V_{LKO}, and not guaranteed outside the specified voltage.
4. The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings (t_{AVQV}) provide new data when addresses are changed.
5. Sampled, not 100% tested.

1.2.4 AC Characteristics - Read-Only Operations[1]

V_{CC}=2.7V-3.6V, T_A=0°C to +70°C

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Read Cycle Time		70		ns
t_{AVQV}	Address to Output Delay			70	ns
t_{ELQV}	CE# to Output Delay	3		70	ns
t_{APA}	Page Address Access Time			25	ns
t_{GLQV}	OE# to Output Delay	3		20	ns
t_{PHQV}	RST# High to Output Delay			150	ns
t_{EHQZ}, t_{GHQZ}	CE# or OE# to Output in High Z, Whichever Occurs First	2		20	ns
t_{ELQX}	CE# to Output in Low Z	2	0		ns
t_{GLQX}	OE# to Output in Low Z	2	0		ns
t_{OH}	Output Hold from First Occurring Address, CE# or OE# change	2	0		ns

NOTES:
1. See AC input/output reference waveform for timing measurements and maximum allowable input slew rate.
2. Sampled, not 100% tested.
3. OE# may be delayed up to $t_{ELQV} - t_{GLQV}$ after the falling edge of CE# without impact to t_{ELQV}.

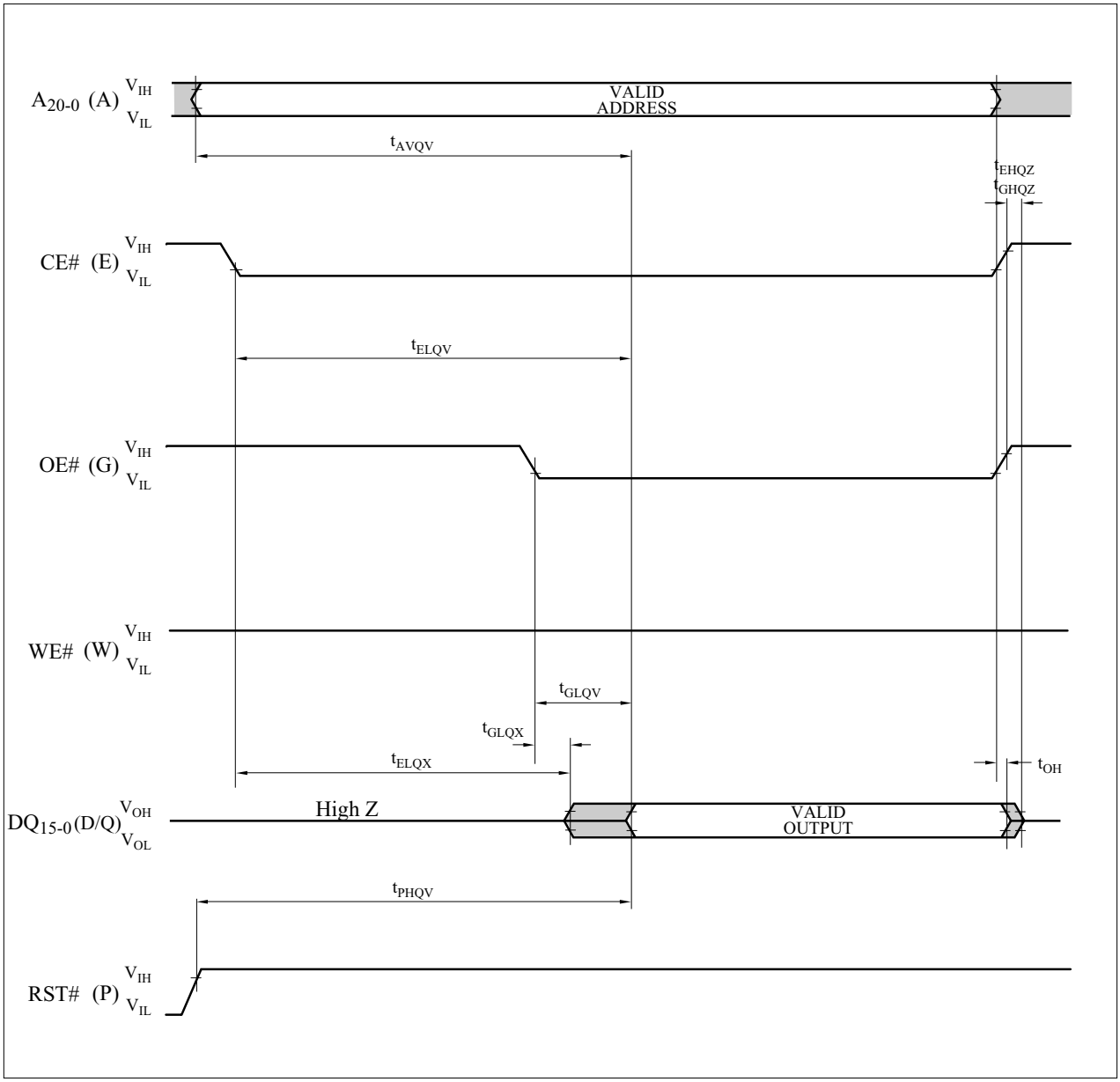


Figure 6. AC Waveform for Single Asynchronous Read Operations
from Status Register, Identifier Codes, OTP Block or Query Code

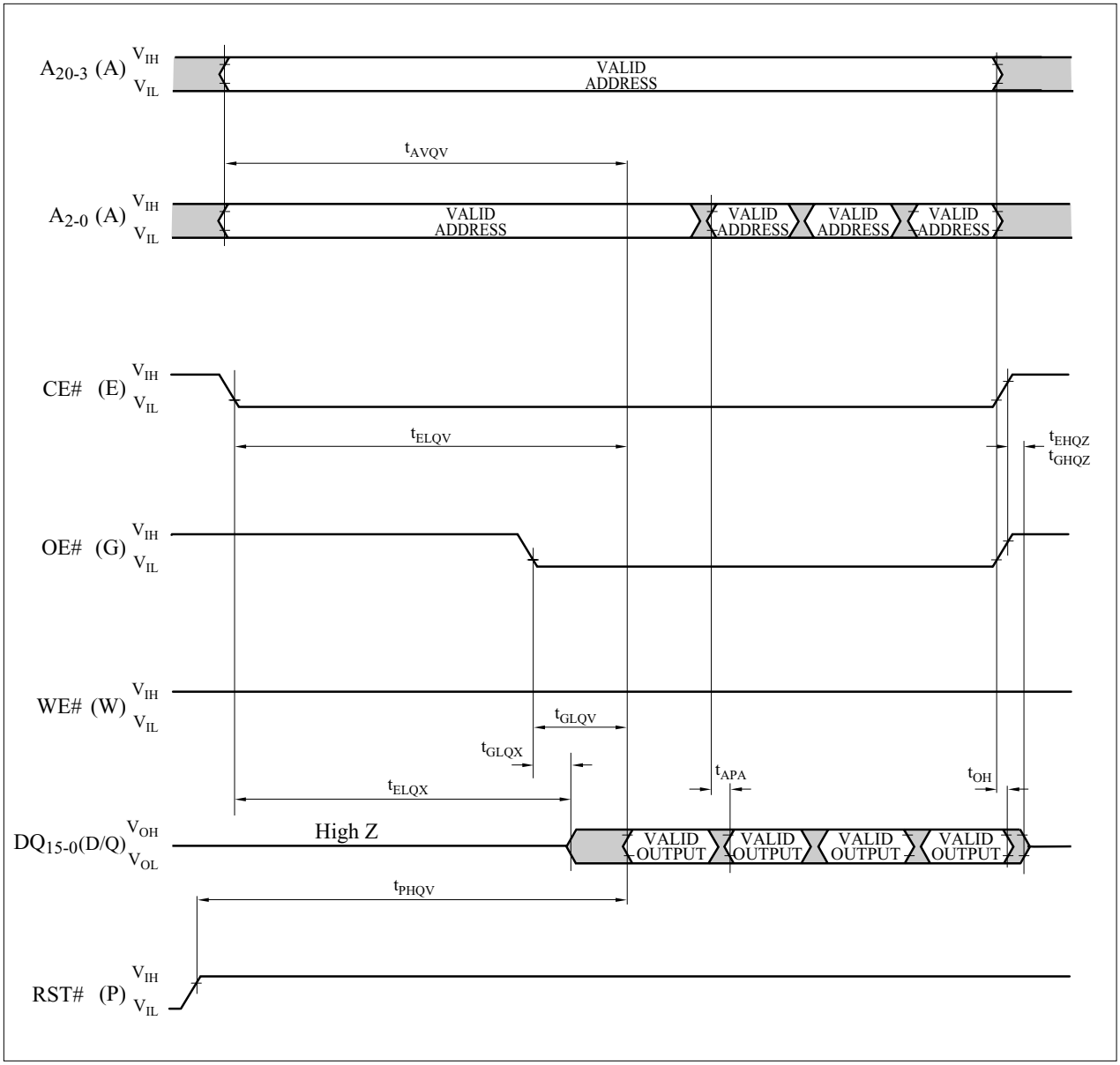


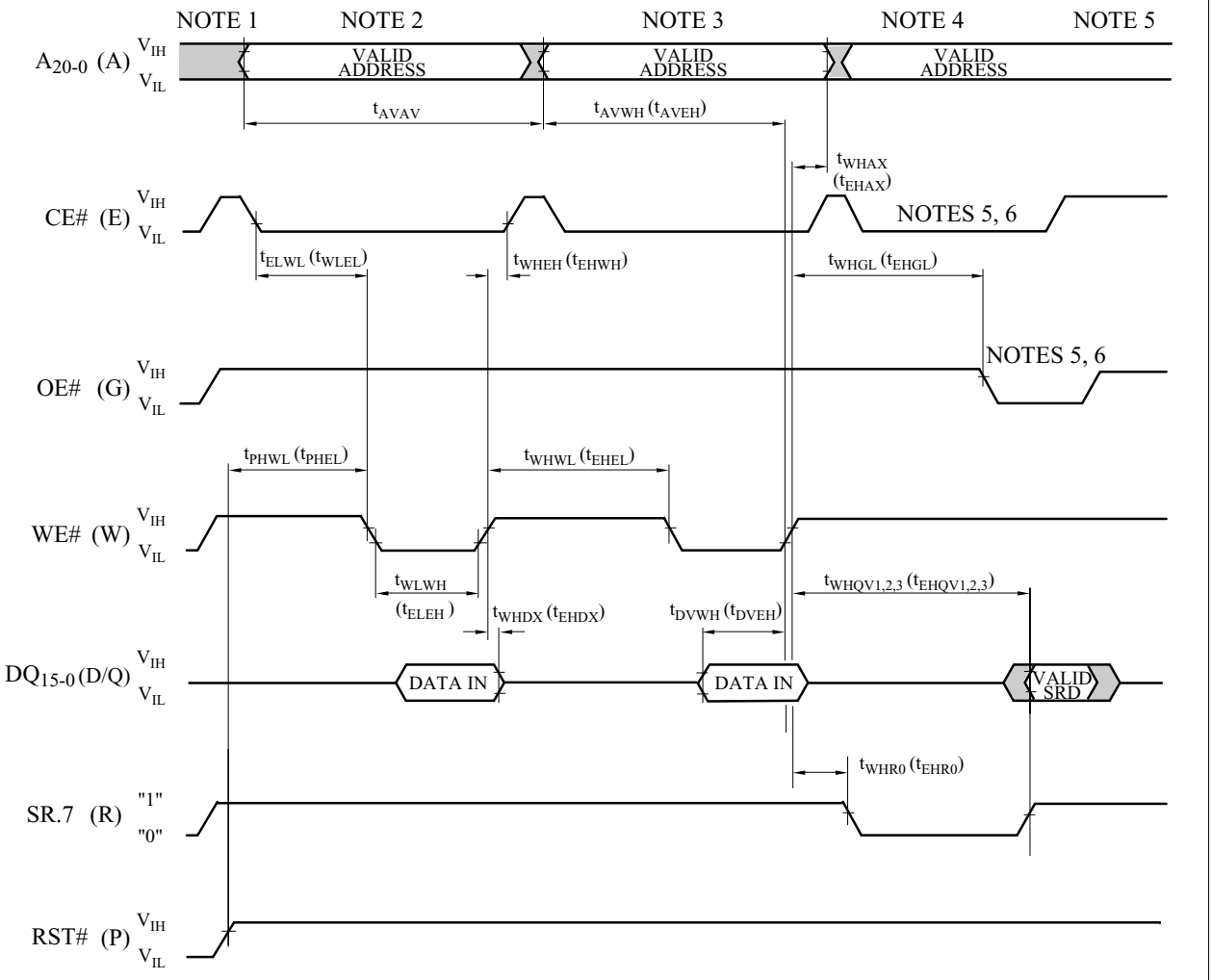
Figure 7. AC Waveform for Asynchronous Page Mode Read Operations
from Main Blocks or Parameter Blocks

1.2.5 AC Characteristics - Write Operations[1, 2]

V_{CC}=2.7V-3.6V, T_A=0°C to +70°C

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		70		ns
t_{PHWL} (t_{PHEL})	RST# High Recovery to WE# (CE#) Going Low	3	150		ns
t_{ELWL} (t_{WLEL})	CE# (WE#) Setup to WE# (CE#) Going Low	4	0		ns
t_{WLWH} (t_{ELEH})	WE# (CE#) Pulse Width	4	50		ns
t_{DVWH} (t_{DVEH})	Data Setup to WE# (CE#) Going High	7	40		ns
t_{AVWH} (t_{AVEH})	Address Setup to WE# (CE#) Going High	7	50		ns
t_{WHEH} (t_{EHWH})	CE# (WE#) Hold from WE# (CE#) High		0		ns
t_{WHDX} (t_{EHDX})	Data Hold from WE# (CE#) High		0		ns
t_{WHAX} (t_{EHAX})	Address Hold from WE# (CE#) High		0		ns
t_{WHWL} (t_{EHEL})	WE# (CE#) Pulse Width High	5	20		ns
t_{WHGL} (t_{EHGL})	Write Recovery before Read		30		ns
t_{WHR0} (t_{EHR0})	WE# (CE#) High to SR.7 Going "0"	3, 6		t_{AVQV}+ 40	ns

NOTES:
1. The timing characteristics for reading the status register during block erase, full chip erase, (page buffer) program and OTP program operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. A write operation can be initiated and terminated with either CE# or WE#.
3. Sampled, not 100% tested.
4. Write pulse width (t_{WP}) is defined from the falling edge of CE# or WE# (whichever goes low last) to the rising edge of CE# or WE# (whichever goes high first). Hence, $t_{WP}=t_{WLWH}=t_{ELEH}=t_{WLEH}=t_{ELWH}$.
5. Write pulse width high (t_{WPH}) is defined from the rising edge of CE# or WE# (whichever goes high first) to the falling edge of CE# or WE# (whichever goes low last). Hence, $t_{WPH}=t_{WHWL}=t_{EHEL}=t_{WHEL}=t_{EHWL}$.
6. t_{WHR0} (t_{EHR0}) after the Read Query or Read Identifier Codes/OTP command=t_{AVQV}+100ns.
7. Refer to Table 4 for valid address and data for block erase, full chip erase, (page buffer) program, OTP program or lock bit configuration.



NOTES:
1. V_{CC} power-up and standby.
2. Write each first cycle command.
3. Write each second cycle command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. For read operation, OE# and CE# must be driven active, and WE# de-asserted.

Figure 8. AC Waveform for Write Operations

1.2.6 Reset Operations

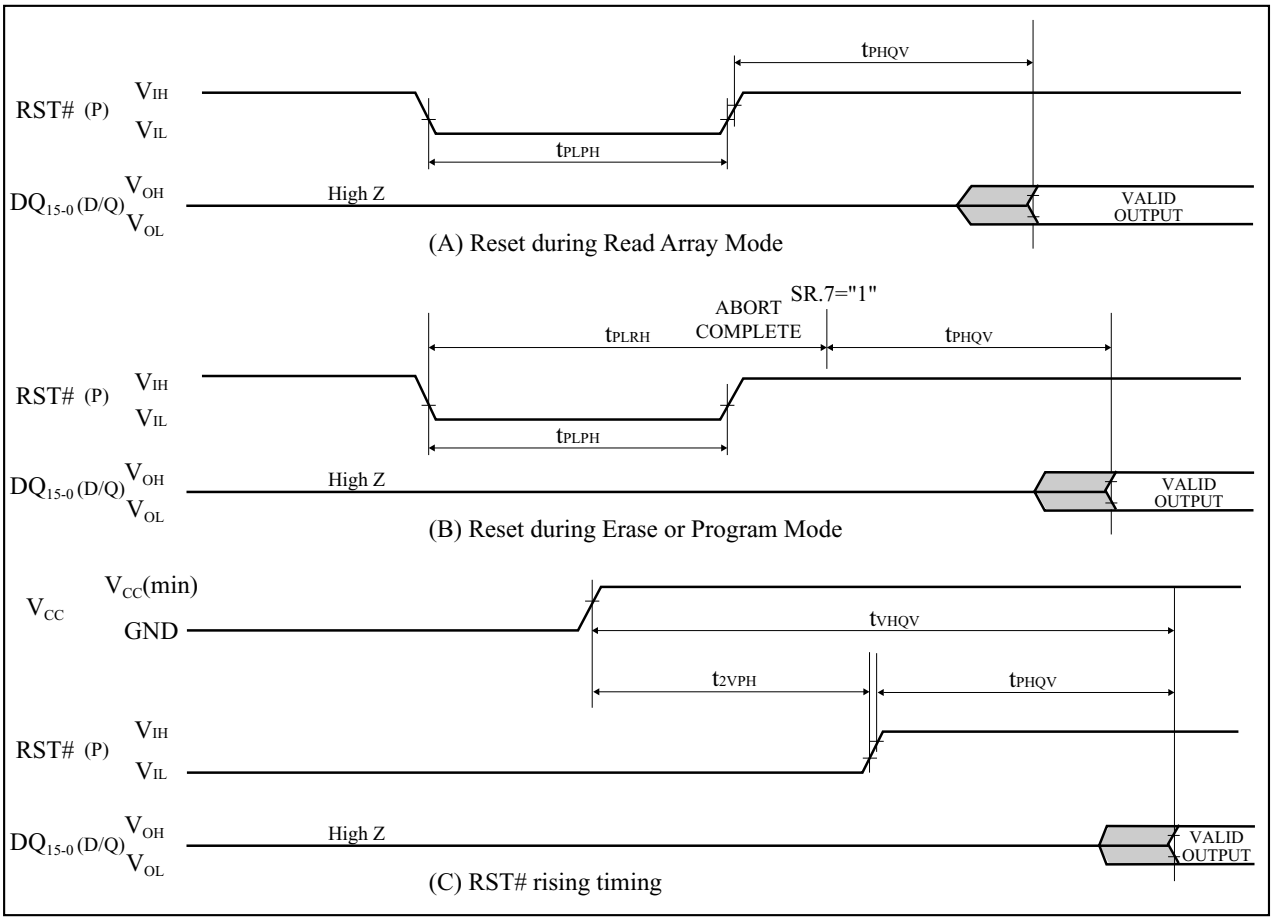


Figure 9. AC Waveform for Reset Operations

Reset AC Specifications (V_{CC}=2.7V-3.6V, T_A=0°C to +70°C)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{PLPH}	RST# Low to Reset during Read (RST# should be low during power-up.)	1, 2, 3	100		ns
t_{PLRH}	RST# Low to Reset during Erase or Program	1, 3, 4		22	µs
t_{2VPH}	V_{CC} 2.7V to RST# High	1, 3, 5	100		ns
t_{VHQV}	V_{CC} 2.7V to Output Delay	3		1	ms

NOTES:
1. A reset time, t_{PHQV}, is required from the later of SR.7 going "1" or RST# going high until outputs are valid. Refer to AC Characteristics - Read-Only Operations for t_{PHQV}.
2. t_{PLPH} is <100ns the device may still reset but this is not guaranteed.
3. Sampled, not 100% tested.
4. If RST# asserted while a block erase, full chip erase, (page buffer) program or OTP program operation is not executing, the reset will complete within 100ns.
5. When the device power-up, holding RST# low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

1.2.7 Block Erase, Full Chip Erase, (Page Buffer) Program and OTP Program Performance[3]

V_{CC}=2.7V-3.6V, T_A=0°C to +70°C

Symbol	Parameter	Notes	Page Buffer Command is Used or not Used	Min.	Typ.[1]	Max.[2]	Unit
t_{WPB}	4K-Word Parameter Block Program Time	2	Not Used		0.05	0.3	s
		2	Used		0.03	0.12	s
t_{WMB}	32K-Word Main Block Program Time	2	Not Used		0.38	2.4	s
		2	Used		0.24	1.0	s
t_{WHQV1}/ t_{EHQV1}	Word Program Time	2	Not Used		11	200	µs
		2	Used		7	100	µs
t_{WHOV1}/ t_{EHOV1}	OTP Program Time	2	Not Used		36	400	µs
t_{WHQV2}/ t_{EHQV2}	4K-Word Parameter Block Erase Time	2	-		0.3	4	s
t_{WHQV3}/ t_{EHQV3}	32K-Word Main Block Erase Time	2	-		0.6	5	s
	Full Chip Erase Time	2			40	350	s
t_{WHRH1}/ t_{EHRH1}	(Page Buffer) Program Suspend Latency Time to Read	4	-		5	10	µs
t_{WHRH2}/ t_{EHRH2}	Block Erase Suspend Latency Time to Read	4	-		5	20	µs
t_{ERES}	Latency Time from Block Erase Resume Command to Block Erase Suspend Command	5	-	500			µs

NOTES:
1. Typical values measured at V_{CC}=3.0V and T_A=+25°C. Assumes corresponding lock bits are not set. Subject to change based on device characterization.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.
4. A latency time is required from writing suspend command (WE# or CE# going high) until SR.7 going "1".
5. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than t_{ERES} and its sequence is repeated, the block erase operation may not be finished.

2 Related Document Information(1)

Document No.	Document Name
FUM00701	LH28F320BF series Appendix

NOTE:

1. International customers should contact their local SHARP or distribution sales offices.

A-1 RECOMMENDED OPERATING CONDITIONS

A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

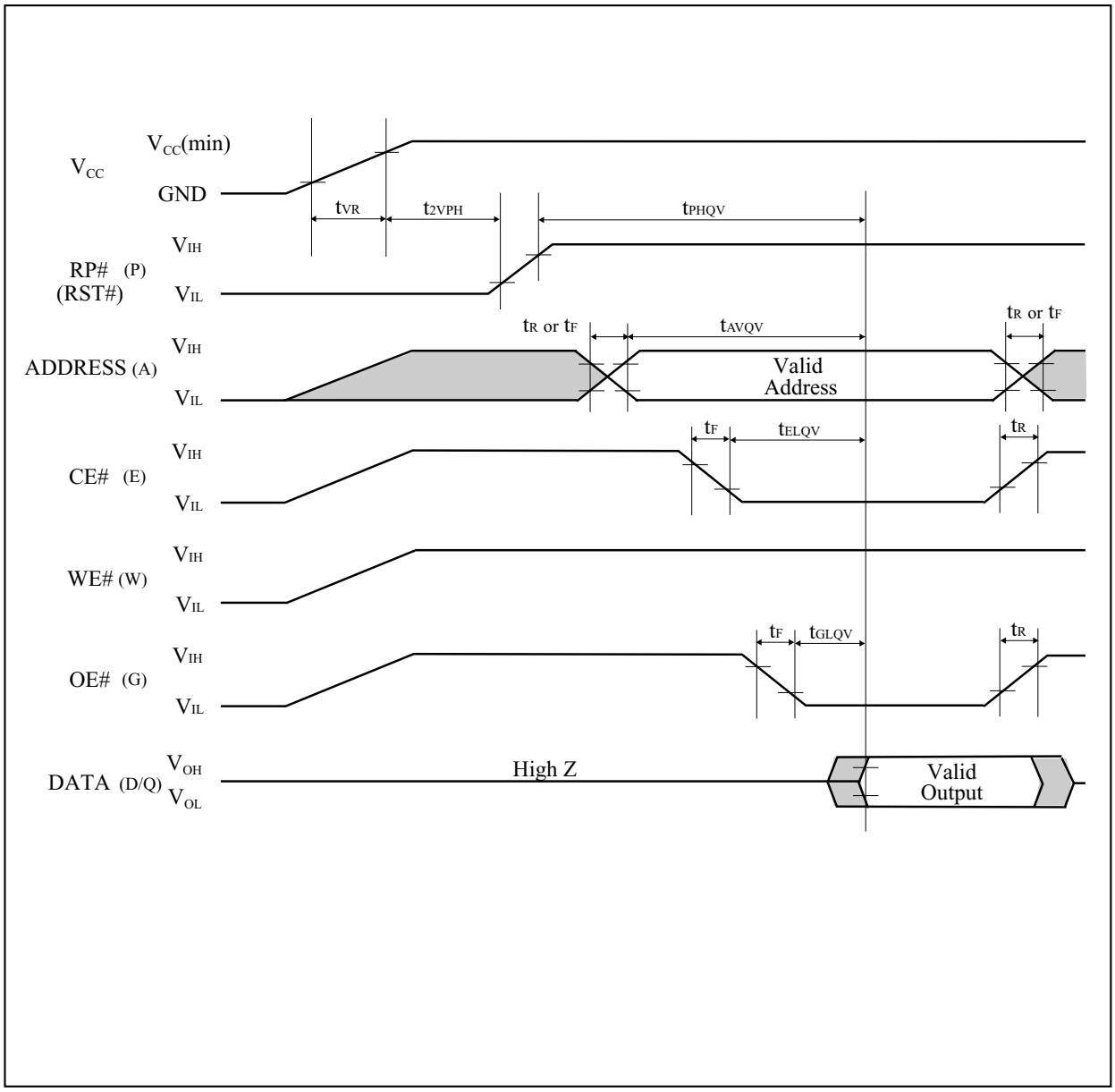


Figure A-1. AC Timing at Device Power-Up

For the AC specifications t_{VR}, t_R, t_F in the figure, refer to the next page. See the "ELECTRICAL SPECIFICATIONS" described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

A-1.1.1 Rise and Fall Time

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{VR}	V_{CC} Rise Time	1	0.5	30000	µs/V
t_R	Input Signal Rise Time	1, 2		1	µs/V
t_F	Input Signal Fall Time	1, 2		1	µs/V

NOTES:
1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.

A-1.2 Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

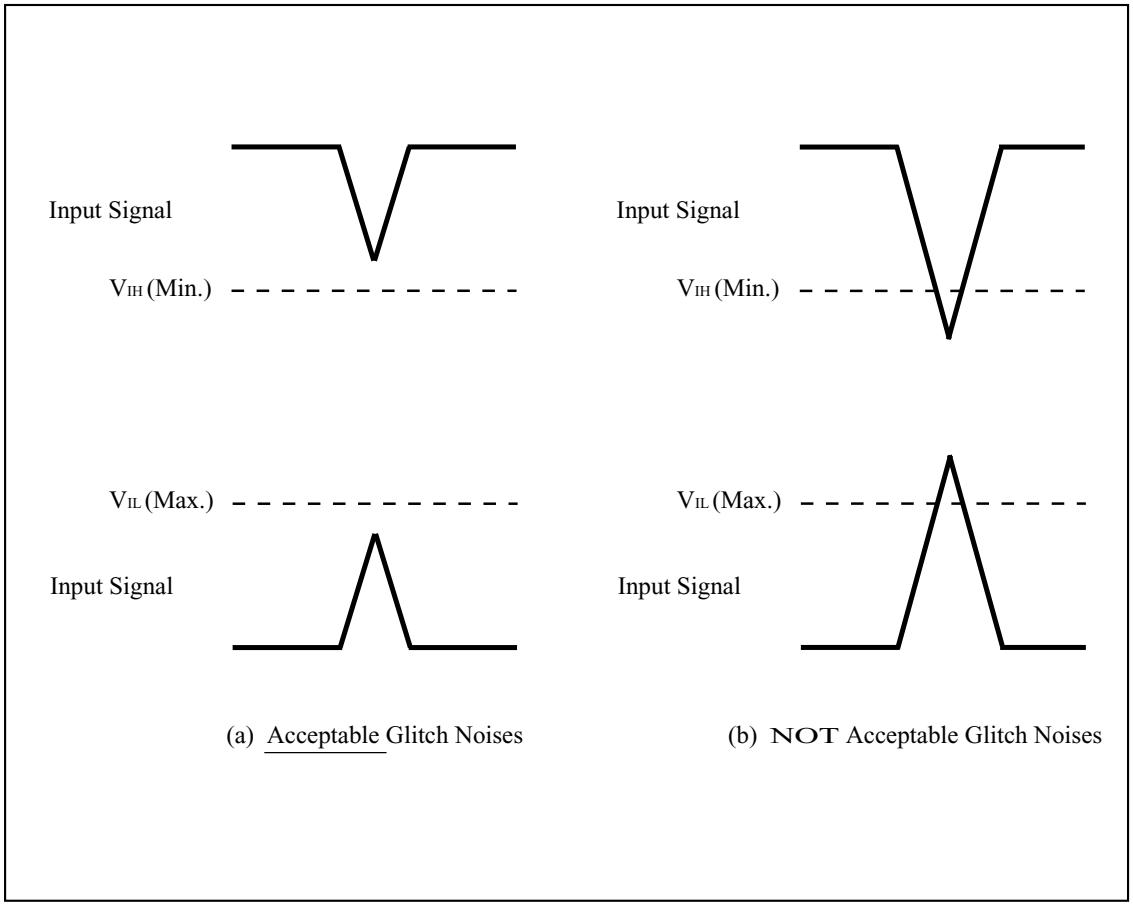


Figure A-2. Waveform for Glitch Noises

See the "DC CHARACTERISTICS" described in specifications for V_{IH} (Min.) and V_{IL} (Max.).

A-2 RELATED DOCUMENT INFORMATION(1)

Document No.	Document Name
AP-001-SD-E	Flash Memory Family Software Drivers
AP-006-PT-E	Data Protection Method of SHARP Flash Memory
AP-007-SW-E	RP#, V_{PP} Electric Potential Switching Circuit

NOTE:
1. International customers should contact their local SHARP or distribution sales office.

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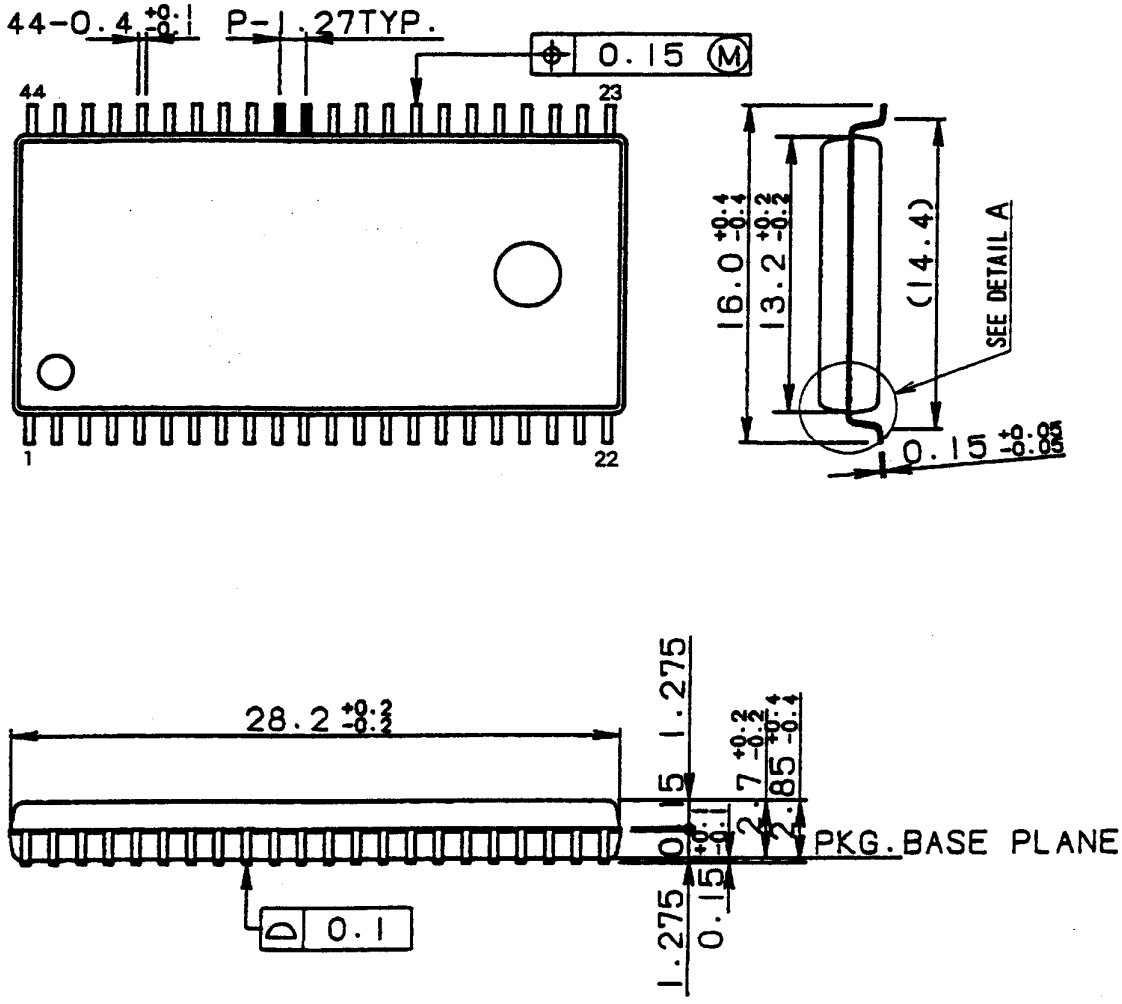

名称 NAME	SOP44-P-600	リード仕上 LEAD FINISH	TIN-LEAD PLATING	備考 NOTE プラスチックパッケージ外形寸法は、バリを含まないものとする。 Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA1050	単位 UNIT	mm	

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SHARP®

NORTH AMERICA

SHARP Microelectronics of the Americas
5700 NW Pacific Rim Blvd.
Camas, WA 98607, U.S.A.
Phone: (1) 360-834-2500
Fax: (1) 360-834-8903
Fast Info: (1) 800-833-9437
www.sharpsma.com

EUROPE

SHARP Microelectronics Europe
Division of Sharp Electronics (Europe) GmbH
Sonninstrasse 3
20097 Hamburg, Germany
Phone: (49) 40-2376-2286
Fax: (49) 40-2376-2232
www.sharpsme.com

JAPAN

SHARP Corporation
Electronic Components & Devices
22-22 Nagaike-cho, Abeno-Ku
Osaka 545-8522, Japan
Phone: (81) 6-6621-1221
Fax: (81) 6117-725300/6117-725301
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TAIWAN

SHARP Electronic Components
(Taiwan) Corporation
8F-A, No. 16, Sec. 4, Nanking E. Rd.
Taipei, Taiwan, Republic of China
Phone: (886) 2-2577-7341
Fax: (886) 2-2577-7326/2-2577-7328

SINGAPORE

SHARP Electronics (Singapore) PTE., Ltd.
438A, Alexandra Road, #05-01/02
Alexandra Technopark,
Singapore 119967
Phone: (65) 271-3566
Fax: (65) 271-3855

KOREA

SHARP Electronic Components
(Korea) Corporation
RM 501 Geosung B/D, 541
Dohwa-dong, Mapo-ku
Seoul 121-701, Korea
Phone: (82) 2-711-5813 ~ 8
Fax: (82) 2-711-5819

CHINA

SHARP Microelectronics of China
(Shanghai) Co., Ltd.
28 Xin Jin Qiao Road King Tower 16F
Pudong Shanghai, 201206 P.R. China
Phone: (86) 21-5854-7710/21-5834-6056
Fax: (86) 21-5854-4340/21-5834-6057
Head Office:
No. 360, Bashen Road,
Xin Development Bldg. 22
Waigaoqiao Free Trade Zone Shanghai
200131 P.R. China
Email: smc@china.global.sharp.co.jp

HONG KONG

SHARP-ROXY (Hong Kong) Ltd.
3rd Business Division,
17/F, Admiralty Centre, Tower 1
18 Harcourt Road, Hong Kong
Phone: (852) 28229311
Fax: (852) 28660779
www.sharp.com.hk
Shenzhen Representative Office:
Room 13B1, Tower C,
Electronics Science & Technology Building
Shen Nan Zhong Road
Shenzhen, P.R. China
Phone: (86) 755-3273731
Fax: (86) 755-3273735