

LH28F016SA

16M (1M × 16/2M × 8) Flash Memory

FEATURES

- User-Selectable 3.3 V or 5 V V_{CC}
- User-Configurable ×8 or ×16 Operation
- Access Times:
 - For 3.3 V Read: 120/150 ns
 - For 5 V Read: 70/100 ns
- 0.43 MB/sec Write Transfer Rate
- 1 Million Erase Cycles per Block
- 56-Lead, 1.2 mm × 14 mm × 20 mm TSOP Package
- Revolutionary Architecture
 - Pipelined Command Execution
 - Write During Erase
 - Command Superset of SHARP's LH28F008SA
- 1 mA Typical I_{CC} in Static Mode
- 1 μ A Typical Deep Power-Down
- 32 Independently Lockable Blocks
- State-of-the-Art 0.6 μ m ETOX™¹ Flash Technology

DESCRIPTION

SHARP's LH28F016SA 16M Flash Memory is a revolutionary architecture which enables the design of truly mobile, high-performance, personal computing and communication products. With innovative capabilities, low power operation and very high read/write performance, the LH28F016SA is also the ideal choice for designing embedded mass storage flash memory systems.

The LH28F016SA is a very high density, highest performance non-volatile read/write solution for solid-state storage applications. Its symmetrically blocked architecture (100% compatible with the LH28F008SA 8M Flash memory), extended cycling, low power 3.3 V operation, very fast write and read performance and selective block locking provide a highly flexible memory component suitable for high-density memory cards, Resident Flash Arrays and PCMCIA-ATA Flash Drives. The LH28F016SA's dual read voltage enables the design of memory cards which can interchangeably be read/written in 3.3 V and 5.0 V systems. Its ×8/×16 architecture allows the optimization of memory to processor interface. The flexible block locking option enables bundling of executable application software in a Resident Flash Array or memory card. Manufactured on SHARP's 0.6 μ m ETOX™¹ process technology, the LH28F016SA is the most cost-effective, high-density 3.3 V flash memory.

¹ ETOX is a trademark of Intel Corporation.

1.0 INTRODUCTION

The documentation of the SHARPLH28F016SA memory device includes this data sheet, a detailed user's manual, and a number of application notes, all of which are referenced at the end of this data sheet.

The data sheet is intended to give an overview of the chip feature-set and of the operating AC/DC specifications. The LH28F016SA User's Manual provides complete descriptions of the user modes, system interface examples, and detailed descriptions of all principles of operation. It also contains the full list of software algorithm flowcharts, and a brief section on compatibility with SHARP LH28F008SA.

1.1 Product Overview

The LH28F016SA is a high-performance 16M (16,777,216 bit) block erasable non-volatile random access memory organized as either 1 Mword × 16 or 2 Mbyte × 8. The LH28F016SA includes thirty-two 64KB (65,536) blocks or thirty-two 32-KW (32,768) blocks. A chip memory map is shown in Figure 3.

The implementation of a new architecture, with many enhanced features, will improve the device operating characteristics and results in greater product reliability and ease of use.

Some significant enhancements of the LH28F016SA include:

- 3.3 V Low Power Capability
- Improved Write Performance
- Dedicated Block Write/Erase Protection

A 3/5# input pin reconfigures the device internally for optimized 3.3 V or 5.0 V read/write operation.

The LH28F016SA will be available in a 56-lead, 1.2 mm thick, 14 mm × 20 mm TSOP type 1 package. This form factor and pinout allow for very high board layout densities.

A Command User Interface (CUI) serves as the system interface between the microprocessor or microcontroller and the internal memory operation.

Internal Algorithm Automation allows Byte/Word Writes and Block Erase operations to be executed using a Two-Write command sequence to the CUI in the same way as the LH28F008SA 8M Flash memory.

A Superset of commands have been added to the basic LH28F008SA command-set to achieve higher write performance and provide additional capabilities. These new commands and features include:

- Page Buffer Writes to Flash
- Command Queuing Capability
- Automatic Data Writes During Erase
- Software Locking of Memory Blocks
- Two-Byte Successive Writes in 8-bit Systems
- Erase All Unlocked Blocks

Writing of memory data is performed in either byte or word increments typically within 6 μsec, a 33% improvement over the LH28F008SA. A Block Erase operation erases one of the 32 blocks in typically 0.6 sec, independent of the other blocks, which is about 65% improvement over the LH28F008SA.

Each block can be written and erased a minimum of 100,000 cycles. Systems can achieve 1 million Block Erase Cycles by providing wear-leveling algorithms and graceful block retirement. These techniques have already been employed in many flash file systems and Hard Disk Drive designs.

The LH28F016SA incorporates two Page Buffers of 256 Bytes (128 Words) each to allow page data writes. This feature can improve a system write performance by up to 4.8 times over previous flash memory devices.

All operations are started by a sequence of Write commands to the device. Three Status Registers (described in detail later) and a RY/BY# output pin provide information on the progress of the requested operation.

While the LH28F008SA requires an operation to complete before the next operation can be requested, the LH28F016SA allows queuing of the next operation while the memory executes the current operation. This eliminates system overhead when writing several bytes in a row to the array or erasing several blocks at the same time. The LH28F016SA can also perform write operations to one block of memory while performing erase of another block.

The LH28F016SA provides user-selectable block locking to protect code or data such as Device Drivers, PCMCIA card information, ROM Executable O/S or Application Code. Each block has an associated non-volatile lock-bit which determines the lock status of the block. In addition, the LH28F016SA has a master Write Protect pin (WP#) which prevents any modifications to memory blocks whose lock-bits are set.

The LH28F016SA contains three types of Status Registers to accomplish various functions:

- A Compatible Status Register (CSR) which is 100% compatible with the LH28F008SA Flash memory's Status Register. This register, when used alone, provides a straightforward upgrade capability to the LH28F016SA from a LH28F008SA-based design.
- A Global Status Register (GSR) which informs the system of command Queue status, Page Buffer status, and overall Write Status Machine (WSM) status.
- 32 Block Status Registers (BSRs) which provide block-specific status information such as the block lock-bit status.

The GSR and BSR memory maps for Byte-Wide and Word-Wide modes are shown in Figures 4.1 and 4.2.

The LH28F016SA incorporates an open drain RY/BY# output pin. This feature allows the user to OR-tie many RY/BY# pins together in a multiple memory configuration such as a Resident Flash Array.

Other configurations of the RY/BY# pin are enabled via special CUI commands and are described in detail in the LH28F016SA User's Manual.

The LH28F016SA also incorporates a dual chip-enable function with two input pins, CE₀# and CE₁#. These pins have exactly the same functionality as the regular chip-enable pin CE# on the LH28F008SA. For minimum chip designs, CE₁# may be tied to ground and use CE₀# as the chip enable input. The LH28F016SA uses the logical combination of these two signals to enable or disable the entire chip. Both CE₀# and CE₁# must be active low to enable the device and if either one becomes inactive, the chip will be disabled. This feature, along with the open drain RY/BY# pin, allows the system designer to reduce the number of control pins used in a large array of 16M devices.

The BYTE# pin allows either ×8 or ×16 read/writes to the LH28F016SA. BYTE# at logic low selects 8-bit

mode with address A₀ selecting between low byte and high byte. On the other hand, BYTE# at logic high enables 16-bit operation with address A₁ becoming the lowest order address and address A₀ is not used (don't care). A device diagram is shown in Figure 1.

The LH28F016SA is specified for a maximum access time of 70 ns (t_{ACC}) at 5.0 V operation (4.75 V to 5.25 V) over the commercial temperature range (0°C to +70°C). A corresponding maximum access time of 120 ns at 3.3 V (3.0 V to 3.6 V and 0°C to +70°C) is achieved for reduced power consumption applications.

The LH28F016SA incorporates an Automatic Power Saving (APS) feature which substantially reduces the active current when the device is in static mode of operation (addresses not switching).

In APS mode, the typical I_{CC} current is 1 mA at 5.0 V (0.8 mA at 3.3 V).

A Deep Power-Down mode of operation is invoked when the RP# (called PWD on the LH28F008SA) pin transitions low. This mode brings the device power consumption to less than 1.0 μA, typically, and provides additional write protection by acting as a device reset pin during power transitions. A reset time of 400 ns is required from RP# switching high until outputs are again valid. In the Deep Power-Down state, the WSM is reset (any current operation will abort) and the CSR, GSR, and BSR registers are cleared.

A CMOS Standby mode of operation is enabled when either CE₀# or CE₁# transitions high and RP# stays high with all input control pins at CMOS levels. In this mode, the device typically draws an I_{CC} standby current of 50 μA.

2.0 DEVICE PINOUT

The LH28F016SA 56L-TSOP Type I pinout configuration is shown in Figure 2.

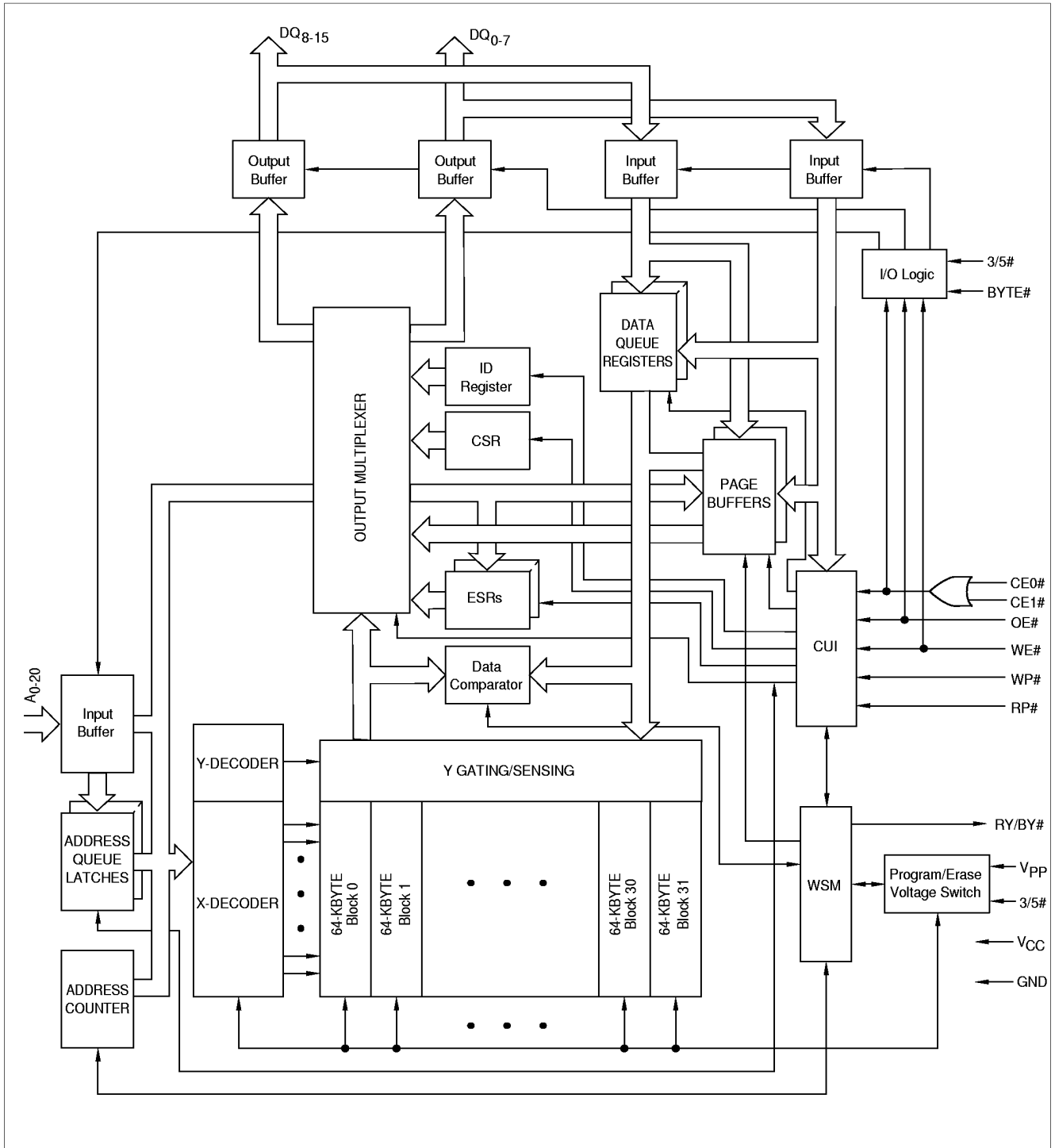


Figure 1. LH28F016SA Block Diagram
Architectural Evolution Includes Page Buffers, Queue Registers, and Extended Status Registers

2.1 Lead Descriptions

Symbol	Type	Name and Function
A ₀	INPUT	BYTE-SELECT ADDRESS: Selects between high and low byte when device is in x8 mode. This address is latched in x8 Data Writes. Not used in x16 mode (i.e., the A ₀ input buffer is turned off when BYTE# is high).
A ₁ -A ₁₅	INPUT	WORD-SELECT ADDRESSES: Select a word within one 64-Kbyte block. A ₆₋₁₅ selects 1 of 1024 rows, and A ₁₋₅ selects 16 of 512 columns. These addresses are latched during Data Writes.
A ₁₆ -A ₂₀	INPUT	BLOCK-SELECT ADDRESSES: Select 1 of 32 Erase blocks. These addresses are latched during Data Writes, Erase and Lock-Block operations.
DQ ₀ -DQ ₇	INPUT/OUTPUT	LOW-BYTE DATA BUS: Inputs data and commands during CUI write cycles. Outputs array, buffer, identifier or status data in the appropriate Read mode. Floated when the chip is de-selected or the outputs are disabled.
DQ ₈ -DQ ₁₅	INPUT/OUTPUT	HIGH-BYTE DATA BUS: Inputs data during x16 Data-Write operations. Outputs array, buffer or identifier data in the appropriate Read mode; not used for Status register reads. Floated when the chip is de-selected or the outputs are disabled.
CE ₀ #, CE ₁ #	INPUT	CHIP ENABLE INPUTS: Activate the device's control logic, input buffers, decoders and sense amplifiers. With either CE ₀ # or CE ₁ # high, the device is de-selected and power consumption reduces to Standby levels upon completion of any current Data-Write or Erase operations. Both CE ₀ #, CE ₁ # must be low to select the device. All timing specifications are the same for both signals. Device Selection occurs with the latter falling edge of CE ₀ # or CE ₁ #. The first rising edge of CE ₀ # or CE ₁ # disables the device.
RP#	INPUT	RESET/POWER-DOWN: RP# low places the device in a Deep Power-Down state. All circuits that burn static power, even those circuits enabled in standby mode, are turned off. When returning from Deep Power-Down, a recovery time of 400 ns is required to allow these circuits to power-up. When RP# goes low, any current or pending WSM operation(s) are terminated, and the device is reset. All Status registers return to ready (with all status flags cleared).
OE#	INPUT	OUTPUT ENABLE: Gates device data through the output buffers when low. The outputs float to tri-state off when OE# is high. NOTE: CE _x # overrides OE#, and OE# overrides WE#.
WE#	INPUT	WRITE ENABLE: Controls access to the CUI, Page Buffers, Data Queue Registers and Address Queue Latches. WE# is active low, and latches both address and data (command or array) on its rising edge.
RY/BY#	OPEN DRAIN OUTPUT	READY/BUSY: Indicates status of the internal WSM. When low, it indicates that the WSM is busy performing an operation. RY/BY# high indicates that the WSM is ready for new operations (or WSM has completed all pending operations), or Erase is Suspended, or the device is in deep power-down mode. This output is always active (i.e., not floated to tri-state off when OE# or CE ₀ #, CE ₁ # are high), except if a RY/BY# Pin Disable command is issued.

2.1 Lead Descriptions (Continued)

Symbol	Type	Name and Function
WP#	INPUT	WRITE PROTECT: Erase blocks can be locked by writing a non-volatile lock-bit for each block. When WP# is low, those locked blocks as reflected by the Block-Lock Status bits (BSR.6), are protected from inadvertent Data Writes or Erases. When WP# is high, all blocks can be Written or Erased regardless of the state of the lock-bits. The WP# input buffer is disabled when RP# transitions low (deep power-down mode).
BYTE#	INPUT	BYTE ENABLE: BYTE# low places device in x8 mode. All data is then input or output on DQ ₀₋₇ , and DQ ₈₋₁₅ float. Address A ₀ selects between the high and low byte. BYTE# high places the device in x16 mode, and turns off the A ₀ input buffer. Address A ₁ , then becomes the lowest order address.
3/5#	INPUT	3.3/5.0 VOLT SELECT: 3/5# high configures internal circuits for 3.3V operation. 3/5# low configures internal circuits for 5.0V operation. NOTES: Reading the array with 3/5# high in a 5.0V system could damage the device. There is a significant delay from 3/5# switching to valid data.
V _{PP}	SUPPLY	ERASE/WRITE POWER SUPPLY: For erasing memory array blocks or writing words/bytes/pages into the flash array.
V _{CC}	SUPPLY	DEVICE POWER SUPPLY (3.3V ± 0.3V, 5.0V ± 0.5V): Do not leave any power pins floating.
GND	SUPPLY	GROUND FOR ALL INTERNAL CIRCUITRY: Do not leave any ground pins floating.
NC		NO CONNECT: No internal connection to die, lead may be driven or left floating.

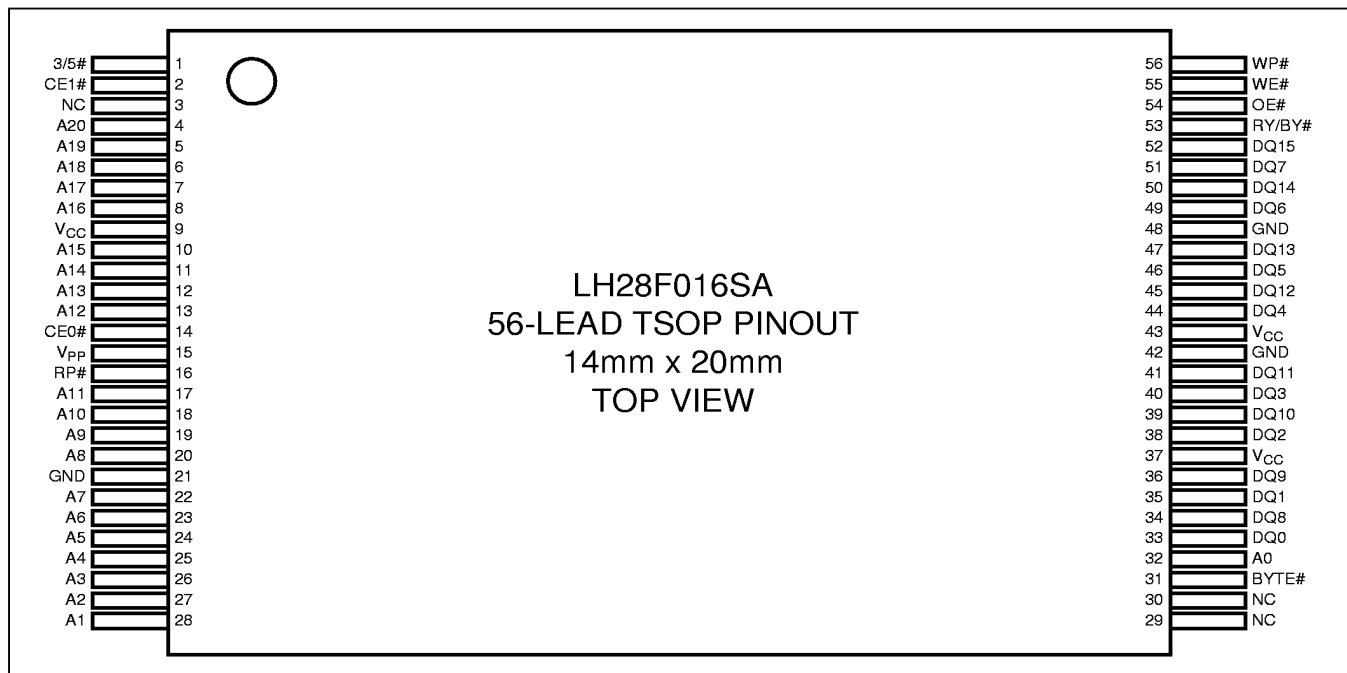


Figure 2. TSOP Configuration

NOTE:

56-LEAD TSOP Mechanical Diagrams and Dimensions are shown at the end of this specification

3.0 MEMORY MAPS

1FFFFF	64 KByte Block	31
1F0000		
1EFFFF	64 KByte Block	30
1E0000		
1DFFFF	64 KByte Block	29
1D0000		
1CFFFF	64 KByte Block	28
1C0000		
1BFFFF	64 KByte Block	27
1B0000		
1AFFFF	64 KByte Block	26
1A0000		
19FFFF	64 KByte Block	25
190000		
18FFFF	64 KByte Block	24
180000		
17FFFF	64 KByte Block	23
170000		
16FFFF	64 KByte Block	22
160000		
15FFFF	64 KByte Block	21
150000		
14FFFF	64 KByte Block	20
140000		
13FFFF	64 KByte Block	19
130000		
12FFFF	64 KByte Block	18
120000		
11FFFF	64 KByte Block	17
110000		
10FFFF	64 KByte Block	16
100000		
0FFFFF	64 KByte Block	15
0F0000		
0EFFFF	64 KByte Block	14
0E0000		
0DFFFF	64 KByte Block	13
0D0000		
0CFFFF	64 KByte Block	12
0C0000		
0BFFFF	64 KByte Block	11
0B0000		
0AFFFF	64 KByte Block	10
0A0000		
09FFFF	64 KByte Block	9
090000		
08FFFF	64 KByte Block	8
080000		
07FFFF	64 KByte Block	7
070000		
06FFFF	64 KByte Block	6
060000		
05FFFF	64 KByte Block	5
050000		
04FFFF	64 KByte Block	4
040000		
03FFFF	64 KByte Block	3
030000		
02FFFF	64 KByte Block	2
020000		
01FFFF	64 KByte Block	1
010000		
00FFFF	64 KByte Block	0
000000		

Figure 3. LH28F016SA Memory Map (Byte-Wide Mode)

3.1 Extended Status Registers Memory Map

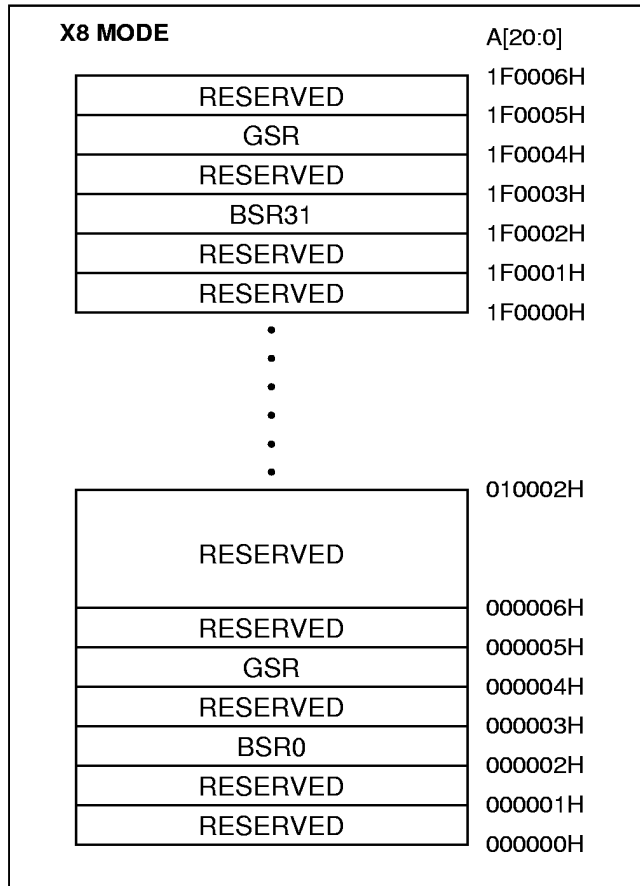


Figure 4.1. Extended Status Register Memory Map (Byte-Wide Mode)

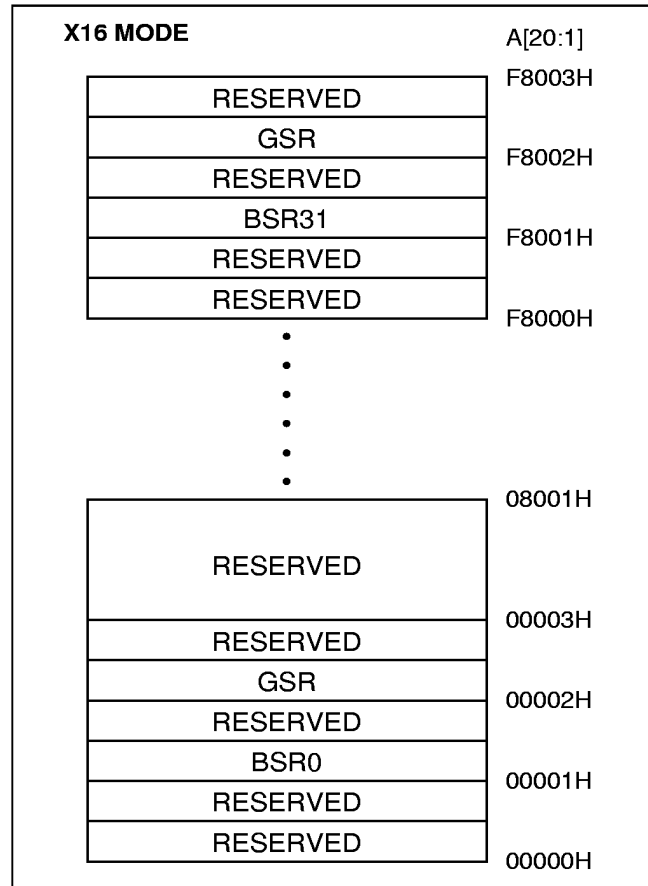


Figure 4.2. Extended Status Register Memory Map (Word-Wide Mode)

4.0 BUS OPERATIONS, COMMANDS AND STATUS REGISTER DEFINITIONS

4.1 Bus Operations for Word-Wide Mode (BYTE# = V_{IH})

Mode	Notes	RP#	CE ₁ #	CE ₀ #	OE#	WE#	A ₁	DQ ₀₋₁₅	RY/BY#
Read	1,2,7	V _{IH}	V _{IL}	V _{IL}	V _{IL}	V _{IH}	X	D _{OUT}	X
Output Disable	1,6,7	V _{IH}	V _{IL}	V _{IL}	V _{IH}	V _{IH}	X	High Z	X
Standby	1,6,7	V _{IH}	V _{IL} V _{IH} V _{IH}	V _{IH} V _{IL} V _{IH}	X	X	X	High Z	X
Deep Power-Down	1,3	V _{IL}	X	X	X	X	X	High Z	V _{OH}
Manufacturer ID	4	V _{IH}	V _{IL}	V _{IL}	V _{IL}	V _{IH}	V _{IL}	0089H	V _{OH}
Device ID	4	V _{IH}	V _{IL}	V _{IL}	V _{IL}	V _{IH}	V _{IH}	66A0H	V _{OH}
Write	1,5,6	V _{IH}	V _{IL}	V _{IL}	V _{IH}	V _{IL}	X	D _{IN}	X

4.2 Bus Operations For Byte-Wide Mode (BYTE# = V_{IL})

Mode	Notes	RP#	CE ₁ #	CE ₀ #	OE#	WE#	A ₀	DQ ₀₋₇	RY/BY#
Read	1,2,7	V _{IH}	V _{IL}	V _{IL}	V _{IL}	V _{IH}	X	D _{OUT}	X
Output Disable	1,6,7	V _{IH}	V _{IL}	V _{IL}	V _{IH}	V _{IH}	X	High Z	X
Standby	1,6,7	V _{IH}	V _{IL} V _{IH} V _{IH}	V _{IH} V _{IL} V _{IH}	X	X	X	High Z	X
Deep Power-Down	1,3	V _{IL}	X	X	X	X	X	High Z	V _{OH}
Manufacturer ID	4	V _{IH}	V _{IL}	V _{IL}	V _{IL}	V _{IH}	V _{IL}	89H	V _{OH}
Device ID	4	V _{IH}	V _{IL}	V _{IL}	V _{IL}	V _{IH}	V _{IH}	A0H	V _{OH}
Write	1,5,6	V _{IH}	V _{IL}	V _{IL}	V _{IH}	V _{IL}	X	D _{IN}	X

NOTES:

- X can be V_{IH} or V_{IL} for address or control pins except for RY/BY#, which is either V_{OL} or V_{OH}.
- RY/BY# output is open drain. When the WSM is ready, Erase is suspended or the device is in deep power-down mode, RY/BY# will be at V_{OH} if it is tied to V_{CC} through a resistor. When the RY/BY# at V_{OH} is independent of OE# while a WSM operation is in progress.
- RP# at GND ±0.2 V ensures the lowest deep power-down current.
- A₀ and A₁ at V_{IL} provide manufacturer ID codes in ×8 and ×16 modes respectively.
A₀ and A₁ at V_{IH} provide device ID codes in ×8 and ×16 modes respectively. All other addresses are set to zero.
- Commands for different Erase operations, Data Write operations of Lock-Block operations can only be successfully completed when V_{PP} = V_{PPH}.
- While the WSM is running, RY/BY# in Level-Mode (default) stays at V_{OL} until all operations are complete. RY/BY# goes to V_{OH} when the WSM is not busy or in erase suspend mode.
- RY/BY# may be at V_{OL} while the WSM is busy performing various operations. For example, a status register read during a write operation.

4.3 LH28F008SA-Compatible Mode Command Bus Definitions

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Array		Write	X	FFH	Read	AA	AD
Intelligent Identifier	1	Write	X	90H	Read	IA	ID
Read Compatible Status Register	2	Write	X	70H	Read	X	CSRD
Clear Status Register	3	Write	X	50H			
Word/Byte Write		Write	X	40H	Write	WA	WD
Alternate Word/Byte Write		Write	X	10H	Write	WA	WD
Block Erase/Confirm		Write	X	20H	Write	BA	D0H
Erase Suspend/Resume		Write	X	B0H	Write	X	D0H

ADDRESS

AA = Array Address
 BA = Block Address
 IA = Identifier Address
 WA = Write Address
 X = Don't Care

DATA

AD = Array Data
 CSRD = CSR Data
 ID = Identifier Data
 WD = Write Data

NOTES:

1. Following the intelligent identifier command, two Read operations access the manufacturer and device signature codes.
2. The CSR is automatically available after device enters Data Write, Erase, or Suspend operations.
3. Clears CSR.3, CSR.4 and CSR.5. Also clears GSR.5 and all BSR.5 and BSR.2 bits.
See Status register definitions.

4.4 LH28F016SA-Performance Enhancement Command Bus Definitions

Command	Mode	Notes	First Bus Cycle			Second Bus Cycle			Third Bus Cycle		
			Oper	Addr	Data	Oper	Addr	Data	Oper	Addr	Data
Read Extended Status Register		1	Write	X	71H	Read	RA	GSRD BSRD			
Page Buffer Swap		7	Write	X	72H						
Read Page Buffer			Write	X	75H	Read	PA	PD			
Single Load to Page Buffer			Write	X	74H	Write	PA	PD			
Sequential Load to Page Buffer	x8	4,6,10	Write	X	E0H	Write	X	BCL	Write	X	BCH
	x16	4,5,6,10	Write	X	E0H	Write	X	WCL	Write	X	WCH
Page Buffer Write to Flash	x8	3,4,9,10	Write	X	0CH	Write	A0	BC(L,H)	Write	WA	BC(H,L)
	x16	4,5,10	Write	X	0CH	Write	X	WCL	Write	WA	WCH
Two-Byte Write	x8	3	Write	X	FBH	Write	A0	WD(L,H)	Write	WA	WD(H,L)
Lock Block/Confirm			Write	X	77H	Write	BA	D0H			
Upload Status Bits/Confirm		2	Write	X	97H	Write	X	D0H			
Upload Device Information			Write	X	99H	Write	X	D0H			
Erase All Unlocked Blocks/Confirm			Write	X	A7H	Write	X	D0H			
RY/BY# Enable to Level-Mode		8	Write	X	96H	Write	X	01H			
RY/BY# Pulse-On-Write		8	Write	X	96H	Write	X	02H			
RY/BY# Pulse-On-Erase		8	Write	X	96H	Write	X	03H			
RY/BY# Disable		8	Write	X	96H	Write	X	04H			
Sleep			Write	X	F0H						
Abort			Write	X	80H						

ADDRESS

BA = Block Address
PA = Page Buffer Address
RA = Extended Register Address
WA = Write Address
X = Don't Care

DATA

AD = Array Data
PD = Page Buffer Data
BSRD = BSR Data
GSRD = GSR Data

WC (L.H) = Word Count (Low, High)
BC (L.H) = Byte Count (Low, High)
WD (L.H) = Write Data (Low, High)

NOTES:

1. RA can be the GSR address or any BSR address. See Figure 4.1 and 4.2 for Extended Status Register Memory Maps.
2. Upon device power-up, all BSR lock-bits come up locked. The Upload Status Bits command must be written to reflect the actual lock-bit status.
3. A₀ is automatically complemented to load second byte of data. BYTE# must be at V_{IL}.
A₀ value determines which WD/BC is supplied first: A₀ = 0 looks at the WDL/BCL, A₀ = 1 looks at the WDH/BCH.
4. BCH/WCH must be at 00H for this product because of the 256-Byte (128 Word) Page Buffer size and to avoid writing the Page Buffer contents into more than one 256-Byte segment within an array block. They are simply shown for future Page Buffer expandability.
5. In ×16 mode, only the lower byte DQ₀₋₇ is used for WCL and WCH. The upper byte DQ₈₋₁₅ is a don't care.
6. PA and PD (Whose count is given in cycles 2 and 3) are supplied starting in the 4th cycle which is not shown.
7. This command allows the user to swap between available Page Buffers (0 or 1).
8. These commands reconfigure RY/BY# output to one of two pulse-modes or enable and disable the RY/BY# function.
9. Write address, WA, is the Destination address in the flash array which must match the Source address in the Page Buffer. Refer to the LH28F016SA User's Manual.
10. BCL = 00H corresponds to a Byte count of 1. Similarly, WCL = 00H corresponds to a Word count of 1.

4.5 Compatible Status Register

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

<p>CSR.7 = WRITE STATE MACHINE STATUS 1 = Ready 0 = Busy</p> <p>CSR.6 = ERASE-SUSPEND STATUS 1 = Erase Suspended 0 = Erase in Progress/Completed</p> <p>CSR.5 = ERASE STATUS 1 = Error in Block Erasure 0 = Successful Block Erase</p> <p>CSR.4 = DATA-WRITE STATUS 1 = Error in Data Write 0 = Data Write Successful</p> <p>CSR.3 = V_{PP} STATUS 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK</p>	<p>NOTES:</p> <p>RY/BY# output or WSMS bit must be checked to determine completion of an operation (Erase Suspend, Erase or Data Write) before the appropriate Status bit (ESS, ES or DWS) is checked for success.</p> <p>If DWS and ES are set to "1" during an erase attempt, an improper command sequence was entered. Clear the CSR and attempt the operation again.</p> <p>The VPPS bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP}'s level only after the Data-Write or Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. VPPS is not guaranteed to report accurate feedback between V_{PP}L and V_{PP}H.</p>
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CSR.2-0 = RESERVED FOR FUTURE ENHANCEMENTS

These bits are reserved for future use: mask them out when polling the CSR.

4.6 Global Status Register

WSMS	OSS	DOS	DSS	QS	PBAS	PBS	PBSS
7	6	5	4	3	2	1	0

<p>GSR.7 = WRITE STATE MACHINE STATUS 1 = Ready 0 = Busy</p> <p>GSR.6 = OPERATION SUSPEND STATUS 1 = Operation Suspended 0 = Operation in Progress/Completed</p> <p>GSR.5 = DEVICE OPERATION STATUS 1 = Operation Unsuccessful 0 = Operation Successful or Currently Running</p> <p>GSR.4 = DEVICE SLEEP STATUS 1 = Device in Sleep 0 = Device Not in Sleep</p> <p>MATRIX 5/4 00 = Operation Successful or Currently Running 01 = Device in Sleep Mode or Pending Sleep 10 = Operation Unsuccessful 11 = Operation Unsuccessful or Aborted</p> <p>GSR.3 = QUEUE STATUS 1 = Queue Full 0 = Queue Available</p> <p>GSR.2 = PAGE BUFFER AVAILABLE STATUS 1 = One or Two Page Buffers Available 0 = No Page Buffer Available</p> <p>GSR.1 = PAGE BUFFER STATUS 1 = Selected Page Buffer Ready 0 = Selected Page Buffer Busy</p> <p>GSR.0 = PAGE BUFFER SELECT STATUS 1 = Page Buffer 1 Selected 0 = Page Buffer 0 Selected</p>	<p>NOTES:</p> <p>[1] RY/BY# output or WSMS bit must be checked to determine completion of an operation (Block Lock, Suspend, any RY/BY# reconfiguration, Upload Status Bits, Erase or Data Write) before the appropriate Status bit (OSS or DOS) is checked for success.</p> <p>If operation currently running, then GSR.7 = 0. If device pending sleep, then GSR.7 = 0.</p> <p>Operation aborted: Unsuccessful due to Abort command.</p> <p>The device contains two Page Buffers.</p> <p>Selected Page Buffer is currently busy with WSM operation.</p>
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NOTE:

- When multiple operations are queued, checking BSR.7 only provides indication of completion for that particular block. GSR.7 provides indication when all queued operations are completed.

4.7 Block Status Register

BS	BLS	BOS	BOAS	QS	VPPS	R	R
7	6	5	4	3	2	1	0

<p>BSR.7 = BLOCK STATUS 1 = Ready 0 = Busy</p> <p>BSR.6 = BLOCK-LOCK STATUS 1 = Block Unlocked for Write/Erase 0 = Block Locked for Write/Erase</p> <p>BSR.5 = BLOCK OPERATION STATUS 1 = Operation Unsuccessful 0 = Operation Successful or Currently Running</p> <p>BSR.4 = BLOCK OPERATION ABORT STATUS 1 = Operation Aborted 0 = Operation Not Aborted</p> <p>MATRIX 5/4 00 = Operation Successful or Currently Running 01 = Not a valid Combination 10 = Operation Unsuccessful 11 = Operation Aborted</p> <p>BSR.3 = QUEUE STATUS 1 = Queue Full 0 = Queue Available</p> <p>BSR.2 = V_{PP} STATUS 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK</p>	<p>NOTES:</p> <p>[1] RY/BY# output or BS bit must be checked to determine completion of an operation (Block Lock, Suspend, Erase or Data Write) before the appropriate Status bits (BOS, BLS) is checked for success.</p> <p>The BOAS bit will not be set until BSR.7 = 1.</p> <p>Operation halted via Abort command.</p>
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NOTES:

BSR.1-0 = RESERVED FOR FUTURE ENHANCEMENTS

These bits are reserved for future use; mask them out when polling the BSRs.

- When multiple operations are queued, checking BSR.7 only provides indication of completion for that particular block. BSR.7 provides indication when all queued operations are completed.

5.0 ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings *

Temperature Under Bias	0°C to + 80°C
Storage Temperature	-65°C to +125°C

*** WARNING:**

Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

V_{CC} = 3.3 V ±0.3 V Systems ⁽⁵⁾

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
T _A	Operating Temperature, Commercial	1	0	70	°C	Ambient Temperature
V _{CC}	V _{CC} with Respect to GND	2	- 0.2	7.0	V	
V _{PP}	V _{PP} Supply Voltage with Respect to GND	2,3	- 0.2	14.0	V	
V	Voltage on any Pin (except V _{CC} , V _{PP}) with Respect to GND	2	- 0.5	V _{CC} + 0.5	V	
I	Current into any Non-Supply Pin			± 30	mA	
I _{OUT}	Output Short Circuit Current	4		100	mA	

V_{CC} = 5.0 V ±0.5 V, V_{CC} = 5.0 V ±0.25 V Systems ^(5,6)

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
T _A	Operating Temperature, Commercial	1	0	70	°C	Ambient Temperature
V _{CC}	V _{CC} with Respect to GND	2	- 0.2	7.0	V	
V _{PP}	V _{PP} Supply Voltage with Respect to GND	2,3	- 0.2	14.0	V	
V	Voltage on any Pin (except V _{CC} , V _{PP}) with Respect to GND	2	- 2.0	7.0	V	
I	Current into any Non-Supply Pin			± 30	mA	
I _{OUT}	Output Short Circuit Current	4		100	mA	

NOTES:

- Operating temperature is for commercial product defined by this specification.
- Minimum DC voltage is - 0.5 V on input/output pins. During transitions, this level may undershoot to - 2.0 V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5 V which, during transitions, may overshoot to V_{CC} + 2.0 V for periods <20 ns.
- Maximum DC voltage on V_{PP} may overshoot to + 14.0 V for periods <20 ns.
- Output shorted for no more than one second. No more than one output shorted at a time.
- AC specifications are valid at both voltage ranges. See DC Characteristics tables for voltage range-specific specifications.
- 5% V_{CC} specifications refer to the LH28F016SA-70 in its High Speed Test configuration.

5.2 Capacitance

For a 3.3 V System:

Symbol	Parameter	Note	Typ	Max	Units	Test Conditions
C _{IN}	Capacitance Looking into an Address/Control Pin	1	6	8	pF	T _A = 25°C, f = 1.0 MHz
C _{OUT}	Capacitance Looking into an Output Pin	1	8	12	pF	T _A = 25°C, f = 1.0 MHz
C _{LOAD}	Load Capacitance Driven by Outputs for Timing Specifications	1		50	pF	For V _{CC} = 3.3V ± 0.3V
	Equivalent Testing Load Circuit			2.5	ns	50Ω transmission line delay

For a 5.0 V System:

Symbol	Parameter	Note	Typ	Max	Units	Test Conditions
C _{IN}	Capacitance Looking into an Address/Control Pin	1	6	8	pF	T _A = 25°C, f = 1.0 MHz
C _{OUT}	Capacitance Looking into an Output Pin	1	8	12	pF	T _A = 25°C, f = 1.0 MHz
C _{LOAD}	Load Capacitance Driven by Outputs for Timing Specifications	1		100	pF	For V _{CC} = 5.0V ± 0.5V
				30	pF	For V _{CC} = 5.0V ± 0.25V
	Equivalent Testing Load Circuit for V _{CC} ± 10%			2.5	ns	25Ω transmission line delay
	Equivalent Testing Load Circuit for V _{CC} ± 5%			2.5	ns	83Ω transmission line delay

NOTE:

1. Sampled, not 100% tested.

5.3 Timing Nomenclature

All 3.3 V system timings are measured from where signals cross 1.5 V.

For 5.0 V systems use the standard JEDEC cross point definitions.

Each timing parameter consists of 5 characters. Some common examples are defined below:

t _{CE}	t _{ELQV} time(t) from CE# (E) going low (L) to the outputs (Q) becoming valid (V)
t _{OE}	t _{GLQV} time(t) from OE# (G) going low (L) to the outputs (Q) becoming valid (V)
t _{ACC}	t _{AVQV} time(t) from address (A) valid (V) to the outputs (Q) becoming valid (V)
t _{AS}	t _{AVWH} time(t) from address (A) valid (V) to WE# (W) going high (H)
t _{DH}	t _{WHDX} time(t) from WE# (W) going high (H) to when the data (D) can become undefined (X)

	Pin Characters		Pin States
A	Address Inputs	H	High
D	Data Inputs	L	Low
Q	Data Outputs	V	Valid
E	CE# (Chip Enable)	X	Driven, but not necessarily valid
G	OE# (Output Enable)	Z	High Impedance
W	WE# (Write Enable)		
P	RP# (Deep Power-Down Pin)		
R	RY/BY# (Ready Busy)		
V	Any Voltage Level		
Y	3/5# Pin		
5V	V _{CC} at 4.5V Minimum		
3V	V _{CC} at 3.0V Minimum		

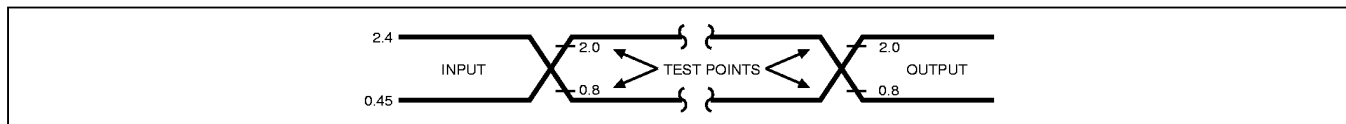


Figure 5. Transient Input/Output Reference Waveform (V_{CC} = 5.0 V) for Standard Test Configuration ⁽¹⁾

AC test inputs are driven at V_{OH} (2.4 VTTL) for a Logic "1" and V_{OL} (0.45 VTTL) for a Logic "0." Input timing begins at V_{IH} (2.0 VTTL) and V_{IL} (0.8 VTTL). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) <10 ns.

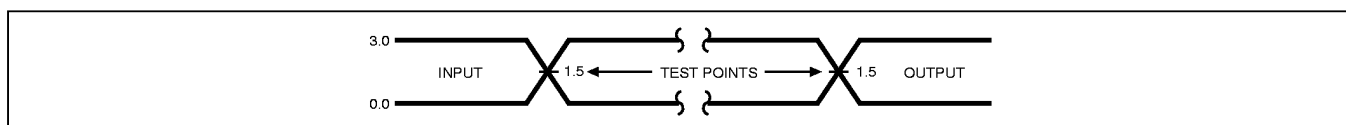
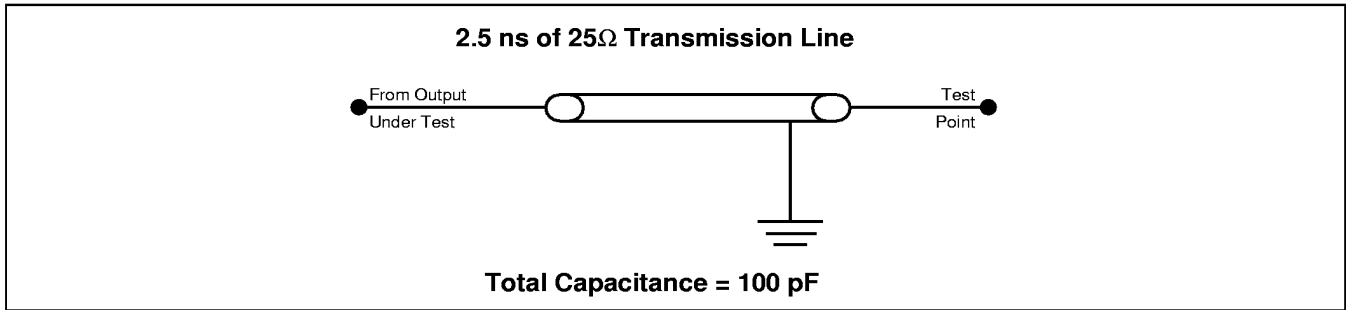


Figure 6. Transient Input/Output Reference Waveform (V_{CC} = 3.3 V) High Speed Reference Waveform ⁽²⁾ (V_{CC} = 5.0 V ±5%)

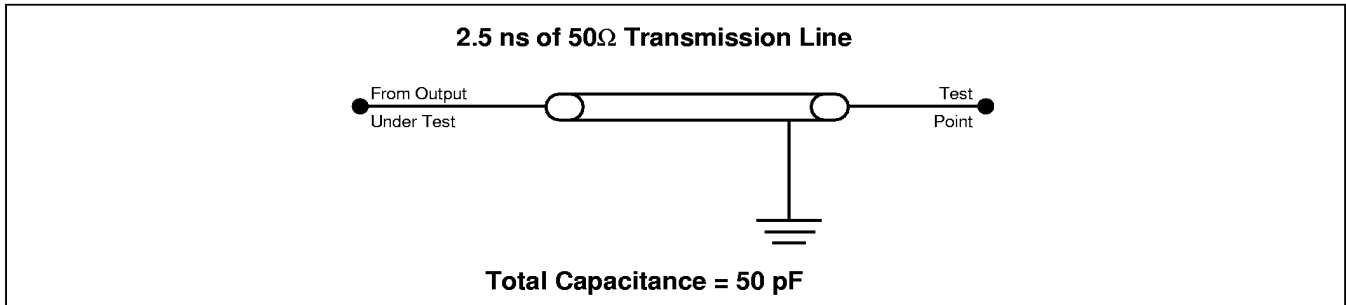
AC test inputs are driven at 3.0 V for a Logic "1" and 0.00 V for a Logic "0." Input timing begins, and output timing ends, at 1.5 V. Input rise and fall times (10% to 90%) <10 ns.

NOTES:

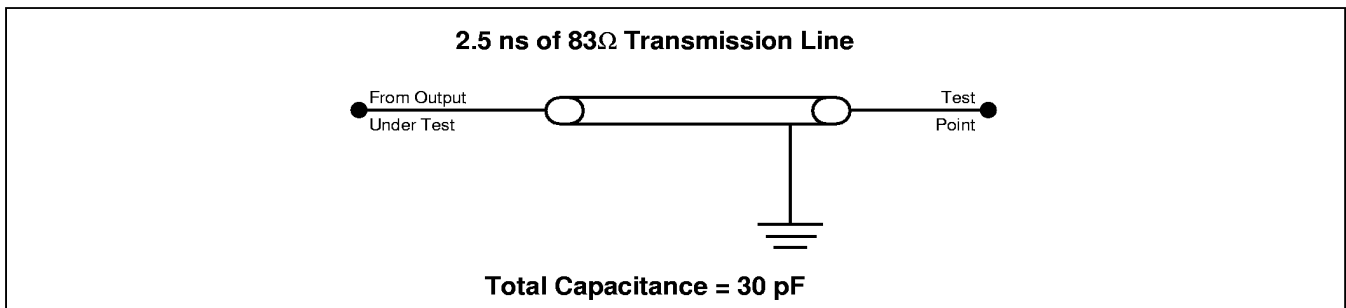
1. Testing characteristics for LH28F016SA-080/LH28F016SA-100.
2. Testing characteristics for LH28F016SA-070/LH28F016SA-120/LH28F016SA-150.



**Figure 7. Transient Equivalent Testing Load Circuit
($V_{CC} = 5.0\text{ V}$)**



**Figure 8. Transient Equivalent Testing Load Circuit
($V_{CC} = 3.3\text{ V}$)**



**Figure 9. High Speed Transient Equivalent Testing
Load Circuit ($V_{CC} = 5.0\text{ V} \pm 5\%$)**

5.4 DC Characteristics

$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$

3/5# = Pin Set High for 3.3 V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I_{IL}	Input Load Current	1			± 1	μA	$V_{CC} = V_{CC} \text{ Max}$, $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1			± 10	μA	$V_{CC} = V_{CC} \text{ Max}$, $V_{IN} = V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	1,5		50	100	μA	$V_{CC} = V_{CC} \text{ Max}$, CE ₀ #, CE ₁ #, RP# = $V_{CC} \pm 0.2\text{V}$ BYTE#, WP#, 3/5# = $V_{CC} \pm 0.2\text{V}$ or GND $\pm 0.2\text{V}$
				1	4	mA	$V_{CC} = V_{CC} \text{ Max}$, CE ₀ #, CE ₁ #, RP# = V_{IH} BYTE#, WP#, 3/5# = V_{IH} or V_{IL}
I_{CCD}	V_{CC} Deep Power-Down Current	1		1	5	μA	RP# = GND $\pm 0.2\text{V}$
I_{CCR1}	V_{CC} Read Current	1,4,5		30	35	mA	$V_{CC} = V_{CC} \text{ Max}$, CMOS: CE ₀ #, CE ₁ # = GND $\pm 0.2\text{V}$ BYTE# = GND $\pm 0.2\text{V}$ or $V_{CC} \pm 0.2\text{V}$ Inputs = GND $\pm 0.2\text{V}$ or $V_{CC} \pm 0.2\text{V}$, TTL: CE ₀ #, CE ₁ # = V_{IL} , BYTE# = V_{IL} or V_{IH} Inputs = V_{IL} or V_{IH} , f = 8 MHz, $I_{OUT} = 0 \text{ mA}$
I_{CCR2}	V_{CC} Read Current	1,4,5		15	20	mA	$V_{CC} = V_{CC} \text{ Max}$, CMOS: CE ₀ #, CE ₁ # = GND $\pm 0.2\text{V}$, BYTE# = $V_{CC} \pm 0.2\text{V}$ or GND $\pm 0.2\text{V}$ Inputs = GND $\pm 0.2\text{V}$ or $V_{CC} \pm 0.2\text{V}$, TTL: CE ₀ #, CE ₁ # = V_{IL} BYTE# = V_{IH} or V_{IL} Inputs = V_{IL} or V_{IH} , f = 4 MHz, $I_{OUT} = 0 \text{ mA}$
I_{CCW}	V_{CC} Write Current	1		8	12	mA	Word/Byte Write in Progress
I_{CCE}	V_{CC} Block Erase Current	1		6	12	mA	Block Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	1,2		3	6	mA	CE ₀ #, CE ₁ # = V_{IH} Block Erase Suspended
I_{PPS}	V_{PP} Standby Current	1		± 1	± 10	μA	$V_{PP} \leq V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1		0.2	5	μA	RP# = GND $\pm 0.2\text{V}$

5.4 DC Characteristics (Continued)

$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$

3/5# = Pin Set High for 3.3 V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I_{PPR}	V_{PP} Read Current	1			200	μA	$V_{PP} > V_{CC}$
I_{PPW}	V_{PP} Write Current	1		10	15	mA	$V_{PP} = V_{PPH}$, Word/Byte Write in Progress
I_{PPE}	V_{PP} Erase Current	1		4	10	mA	$V_{PP} = V_{PPH}$, Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1			200	μA	$V_{PP} = V_{PPH}$, Block Erase Suspended
V_{IL}	Input Low Voltage		- 0.3		0.8	V	
V_{IH}	Input High Voltage		2.0		$V_{CC} + 0.3$	V	
V_{OL}	Output Low Voltage				0.4	V	$V_{CC} = V_{CC}$ Min and $I_{OL} = 4 \text{ mA}$
V_{OH1}	Output High Voltage		2.4			V	$I_{OH} = - 2.0 \text{ mA}$ $V_{CC} = V_{CC}$ Min
V_{OH2}			$V_{CC} - 0.2$				$I_{OH} = - 100 \mu\text{A}$ $V_{CC} = V_{CC}$ Min
V_{PPL}	V_{PP} during Normal Operations	3	0.0		6.5	V	
V_{PPH}	V_{PP} during Write/ Erase Operations		11.4	12.0	12.6	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.0			V	

NOTES:

- All currents are in RMS unless otherwise noted. Typical values at $V_{CC} = 3.3 \text{ V}$, $V_{PP} = 12.0 \text{ V}$, $T = 25^\circ\text{C}$. These currents are valid for all product versions (package and speeds).
- I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR} .
- Block Erases, Word/Byte Writes, and Lock Block operations are inhibited when $V_{PP} = V_{PPL}$ and not guaranteed in the range between V_{PPH} and V_{PPL} .
- Automatic Power Saving (APS) reduces I_{CCR} to less than 1 mA in static operation.
- CMOS Inputs are either $V_{CC} \pm 0.2 \text{ V}$ or $\text{GND} \pm 0.2 \text{ V}$. TTL Inputs are either V_{IL} or V_{IH} .

5.5 DC Characteristics

$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$

3/5# Pin Set Low for 5 V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I_{IL}	Input Load Current	1			± 1	μA	$V_{CC} = V_{CC} \text{ Max}$ $V_{IN} = V_{CC} \text{ or GND}$
I_{LO}	Output Leakage Current	1			± 10	μA	$V_{CC} = V_{CC} \text{ Max}$ $V_{IN} = V_{CC} \text{ or GND}$
I_{CCS}	V_{CC} Standby Current	1,5		50	100	μA	$V_{CC} = V_{CC} \text{ Max}$ $CE_0\#, CE_1\#, RP\# = V_{CC} \pm 0.2\text{V}$ $BYTE\#, WP\#, 3/5\# = V_{CC} \pm 0.2\text{V}$ or $GND \pm 0.2\text{V}$
				2	4	mA	$V_{CC} = V_{CC} \text{ Max}$ $CE_0\#, CE_1\#, RP\# = V_{IH}$ $BYTE\#, WP\#, 3/5\# = V_{IH} \text{ or } V_{IL}$
I_{CCD}	V_{CC} Deep Power-Down Current	1		1	5	μA	$RP\# = GND \pm 0.2\text{V}$
I_{CCR1}	V_{CC} Read Current	1,4,5		50	60	mA	$V_{CC} = V_{CC} \text{ Max}$, CMOS: $CE_0\#, CE_1\# = GND \pm 0.2\text{V}$ $BYTE\# = GND \pm 0.2\text{V}$ or $V_{CC} \pm 0.2\text{V}$ Inputs = $GND \pm 0.2\text{V}$ or $V_{CC} \pm 0.2\text{V}$, TTL: $CE_0\#, CE_1\# = V_{IL}$, $BYTE\# = V_{IL}$ or V_{IH} Inputs = V_{IL} or V_{IH} , $f = 10 \text{ MHz}$, $I_{OUT} = 0 \text{ mA}$
I_{CCR2}	V_{CC} Read Current	1,4,5		30	35	mA	$V_{CC} = V_{CC} \text{ Max}$, CMOS: $CE_0\#, CE_1\# = GND \pm 0.2\text{V}$ $BYTE\# = V_{CC} \pm 0.2\text{V}$ or $GND \pm 0.2\text{V}$ Inputs = $GND \pm 0.2\text{V}$ or $V_{CC} \pm 0.2\text{V}$ TTL: $CE_0\#, CE_1\# = V_{IL}$, $BYTE\# = V_{IH}$ or V_{IL} , Inputs = V_{IL} or V_{IH} , $f = 5 \text{ MHz}$, $I_{OUT} = 0 \text{ mA}$
I_{CCW}	V_{CC} Write Current	1		25	35	mA	Word/Byte in Progress
I_{CCE}	V_{CC} Block Erase Current	1		18	25	mA	Block Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	1,2		5	10	mA	$CE_0\#, CE_1\# = V_{IH}$ Block Erase Suspended
I_{PPS}	V_{PP} Standby Current	1			± 10	μA	$V_{PP} \leq V_{CC}$

5.5 DC Characteristics (Continued)

$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$

3/5# Pin Set Low for 5 V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I _{PPD}	V _{PP} Deep Power-Down Current	1		0.2	5	μA	RP# = GND ± 0.2V
I _{PPR}	V _{PP} Read Current	1		65	200	μA	V _{PP} > V _{CC}
I _{PPW}	V _{PP} Write Current	1		7	12	mA	V _{PP} = V _{PPH} Word/Byte Write in Progress
I _{PPE}	V _{PP} Block Erase Current	1		5	10	mA	V _{PP} = V _{PPH} Block Erase in Progress
I _{PPES}	V _{PP} Erase Suspend Current	1		65	200	μA	V _{PP} = V _{PPH} Block Erase Suspended
V _{IL}	Input Low Voltage		- 0.5		0.8	V	
V _{IH}	Input High Voltage		2.0		V _{CC} + 0.5	V	
V _{OL}	Output Low Voltage				0.45	V	V _{CC} = V _{CC} Min I _{OL} = 5.8 mA
V _{OH1}	Output High Voltage		0.85 V _{CC}			V	I _{OH} = - 2.5 mA V _{CC} = V _{CC} Min
V _{OH2}			V _{CC} - 0.4				I _{OH} = - 100 μA V _{CC} = V _{CC} Min
V _{PPPL}	V _{PP} during Normal Operations	3	0.0		6.5	V	
V _{PPPH}	V _{PP} during Erase/Write Operations		11.4	12.0	12.6	V	
V _{LKO}	V _{CC} Erase/Write Lock Voltage		2.0			V	

NOTES:

- All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0 V, V_{PP} = 12.0 V, T = 25°C. These currents are valid for all product versions (package and speeds).
- I_{CCES} is specified with the device deselected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
- Block Erases, Word/Byte Writes, and Lock Block operations are inhibited when V_{PP} = V_{PPPL} and not guaranteed in the range between V_{PPH} and V_{PPPL}.
- Automatic Power Saving (APS) reduces I_{CCR} to less than 2 mA in Static operation.
- CMOS Inputs are either V_{CC} ± 0.2 V or GND ± 0.2 V. TTL Inputs are either V_{IL} or V_{IH}.

5.6 AC Characteristics - Read Only Operations ⁽¹⁾

V_{CC} = 3.3 V ±0.3 V, T_A = 0°C to +70°C

Versions ⁽⁵⁾			LH28F016SA-120		LH28F016SA-150		Units
Symbol	Parameter	Notes	Min	Max	Min	Max	
t _{AVAV}	Read Cycle Time		120		150		ns
t _{AVEL}	Address Setup to CE# Going Low	3,4	10		10		ns
t _{AVGL}	Address Setup to OE# Going Low	3,4	0		0		ns
t _{AVQV}	Address to Output Delay			120		150	ns
t _{ELQV}	CE# to Output Delay	2		120		150	ns
t _{PHQV}	RP# High to Output Delay			620		750	ns
t _{GLQV}	OE# to Output Delay	2		45		50	ns
t _{ELQX}	CE# to Output in Low Z	3	0		0		ns
t _{EHQZ}	CE# to Output in High Z	3		50		55	ns
t _{GLQX}	OE# to Output in Low Z	3	0		0		ns
t _{GHQZ}	OE# to Output in High Z	3		30		40	ns
t _{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		0		ns
t _{FLQV} t _{FHQV}	BYTE# to Output Delay	3		120		150	ns
t _{FLQZ}	BYTE# Low to Output in High Z	3		30		40	ns
t _{ELFL} t _{ELFH}	CE# Low to BYTE# High or Low	3		5		5	ns

5.6 AC Characteristics - Read Only Operations ⁽¹⁾ (Continued)

V_{CC} = 5.0 V ±0.5 V, T_A = 0°C to +70°C

Versions ⁽⁵⁾		V _{CC} ± 5%	LH28F016SA-070 ⁽⁶⁾		LH28F016SA-080 ⁽⁷⁾		LH28F016SA-100 ⁽⁶⁾		Units
		V _{CC} ± 10%	Min	Max	Min	Max	Min	Max	
Symbol	Parameter	Notes	Min	Max	Min	Max	Min	Max	
t _{AVAV}	Read Cycle Time		70		80		100		ns
t _{AVEL}	Address Setup to CE# Going Low	3,4	10		10		10		ns
t _{AVGL}	Address Setup to OE# Going Low	3,4	0		0		0		ns
t _{AVQV}	Address to Output Delay			70		80		100	ns
t _{ELQV}	CE# to Output Delay	2		70		80		100	ns
t _{PHQV}	RP# to Output Delay			400		480		550	ns
t _{GLQV}	OE# to Output Delay	2		30		35		40	ns
t _{ELQX}	CE# to Output in Low Z	3	0		0		0		ns
t _{EHQZ}	CE# to Output in High Z	3		25		30		35	ns
t _{GLQX}	OE# to Output in Low Z	3	0		0		0		ns
t _{GHQZ}	OE# to Output in High Z	3		25		30		35	ns
t _{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		0		0		ns
t _{ELQV} t _{FHQV}	BYTE# to Output Delay	3		70		80		100	ns
t _{FLQZ}	BYTE# Low to Output in High Z	3		25		30		30	ns
t _{ELFL} t _{ELFH}	CE# Low to BYTE# High or Low	3		5		5		5	ns

NOTES:

1. See AC Input/Output Reference Waveforms for timing measurements, Figures 5 and 6.
2. OE# may be delayed up to t_{ELQV} - t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
3. Sampled, not 100% tested.
4. This timing parameter is used to latch the correct BSR data onto the outputs.
5. Device Speeds are defined as:
70/80 ns at V_{CC} = 5.0 V equivalent to 120 ns at V_{CC} = 3.3 V
100 ns at V_{CC} = 5.0 V equivalent to 150 ns at V_{CC} = 3.3 V
6. See AC Input/Output Reference Waveforms and AC Testing Load Circuits for High Speed Test Configuration.
7. See Standard AC Input/Output Reference Waveforms and AC Testing Load Circuit.

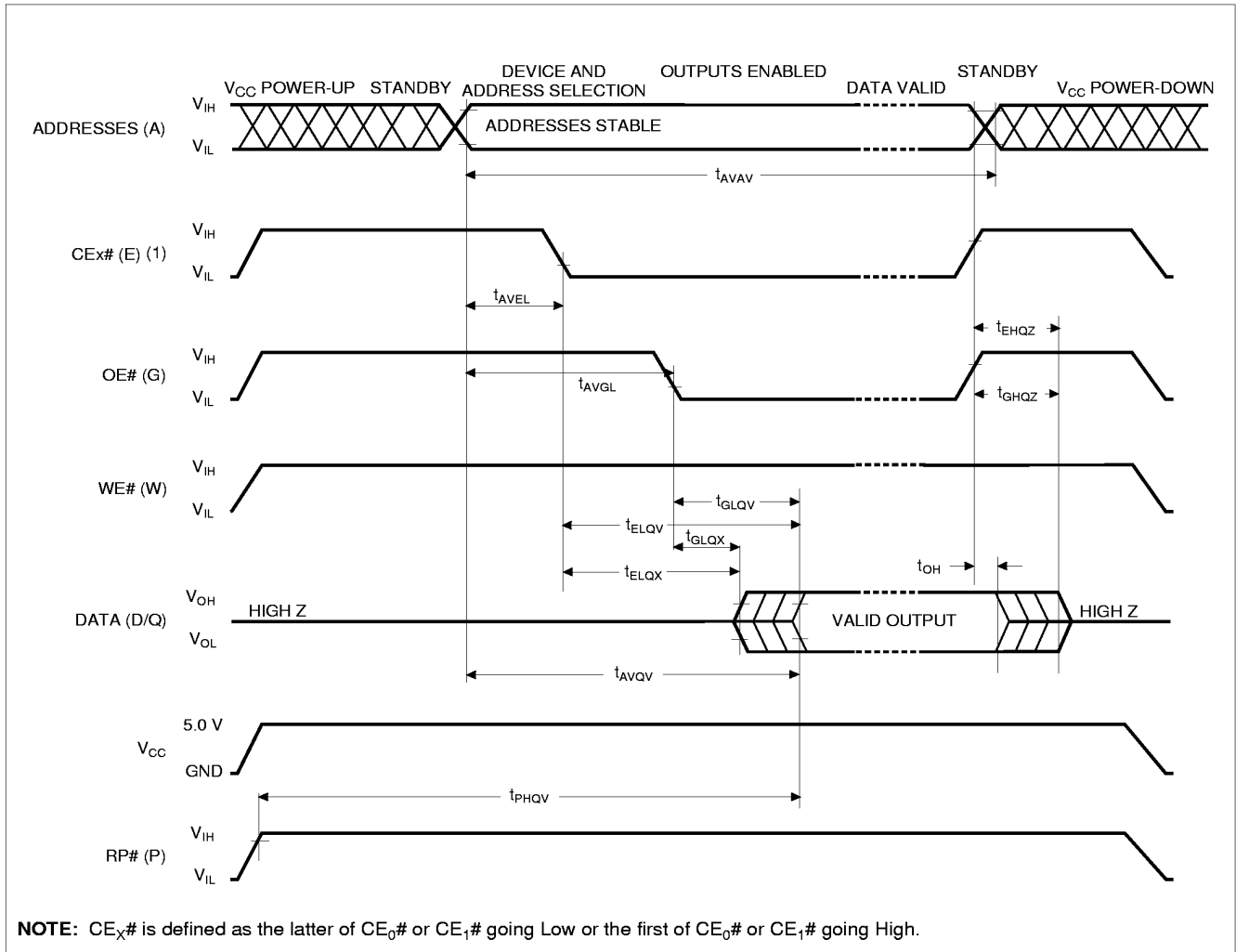


Figure 10. Read Timing Waveforms

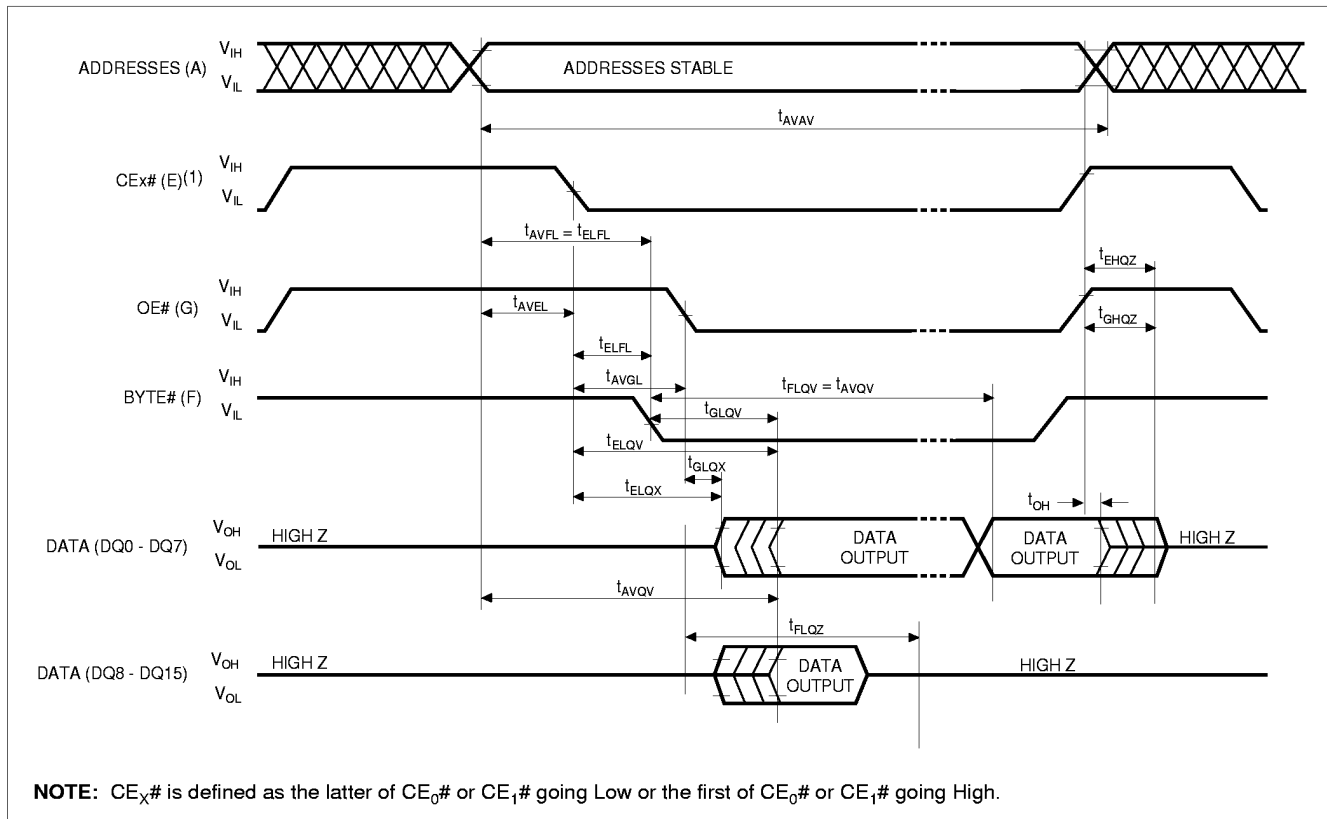
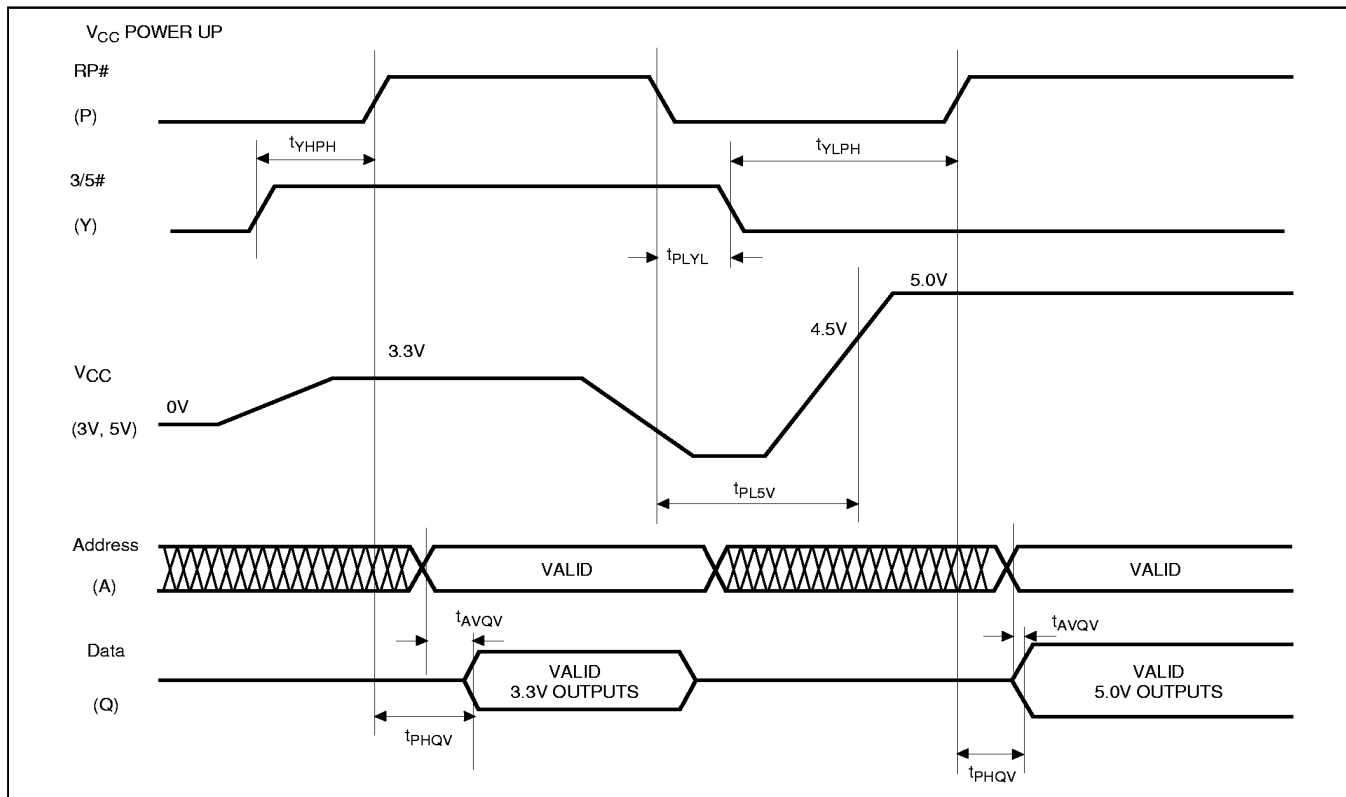


Figure 11. BYTE# Timing Waveforms

5.7 Power-Up and Reset Timings

Figure 12. V_{CC} Power-Up and RP# Reset Waveforms

Symbol	Parameter	Note	Min	Max	Unit
t _{PLYL} t _{PLYH}	RP# Low to 3/5 # Low (High)		0		μs
t _{YLPH} t _{YHPH}	3/5# Low (High) to RP # High	1	2		μs
t _{PL5V} t _{PL3V}	RP# Low to V _{CC} at 4.5V Minimum (to V _{CC} at 3.0V min or 3.6V max)	2	0		μs
t _{AVQV}	Address Valid to Data Valid for V _{CC} = 5V ± 10%	3		80	ns
t _{PHQV}	RP# High to Data Valid for V _{CC} = 5V ± 10%	3		480	ns

NOTES:

CE₀#, CE₁#, and OE# are switched low after Power-Up.

1. Minimum of 2 μs is required to meet the specified t_{PHQV} times.
2. The power supply may start to switch concurrently with RP# going Low.
3. The address access time and RP# high to data valid time are shown for 5 V V_{CC} operation. Refer to the AC Characteristics Read Only Operations 3.3 V V_{CC} operation and all other speed options.

5.8 AC Characteristics for WE# - Controlled Command Write Operations ⁽¹⁾

V_{CC} = 3.3 V ±0.3 V, T_A = 0°C to +70°C

Versions			LH28F016SA-120			LH28F016SA-150			Unit
Symbol	Parameter	Notes	Min	Typ	Max	Min	Typ	Max	
t _{AVAV}	Write Cycle Time		120			150			ns
t _{VPWH}	V _{PP} Setup to WE# Going High	3	100			100			ns
t _{PHL}	RP# Setup to CE# Going Low		480			480			ns
t _{ELWL}	CE# Setup to WE# Going Low		10			10			ns
t _{AVWH}	Address Setup to WE# Going High	2,6	75			75			ns
t _{DVWH}	Data Setup to WE# Going High	2,6	75			75			ns
t _{WLWH}	WE# Pulse Width		75			75			ns
t _{WHDX}	Data Hold from WE# High	2	10			10			ns
t _{WHAX}	Address Hold from WE# High	2	10			10			ns
t _{WHEH}	CE# Hold from WE# High		10			10			ns
t _{WHEL}	WE# Pulse Width High		45			75			ns
t _{GHWL}	Read Recovery before Write		0			0			ns
t _{WHRL}	WE# High to RY/BY# Going Low				100			100	ns
t _{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			0			ns
t _{PHWL}	RP# High Recovery to WE# Going Low		1			1			μs
t _{WHGL}	Write Recovery before Read		95			120			ns
t _{QVVL}	V _{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High		0			0			μs
t _{WHQV1}	Duration of Word/Byte Write Operation	4,5	5	9		5	9		μs
t _{WHQV2}	Duration of Block Erase Operation	4	0.3			0.3			s

AC Characteristics for WE# - Controlled Command Write Operations ⁽¹⁾ (Continued)V_{CC} = 5.0 ± 0.5 V, T_A = 0 °C to + 70 °C

Versions		VCC ± 5%	LH28F016SA-070									Unit
		VCC ± 10%				LH28F016SA-080			LH28F016SA-100			
Symbol	Parameter	Notes	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _{AVAV}	Write Cycle Time		70			80			100			ns
t _{VPWH}	V _{PP} Setup to WE# Going High	3	100			100			100			ns
t _{PHL}	RP# Setup to CE# Going Low		480			480			480			ns
t _{ELWL}	CE# Setup to WE# Going Low		0			0			0			ns
t _{AVWH}	Address Setup to WE# Going High	2,6	50			50			50			ns
t _{DVWH}	Data Setup to WE# Going High	2,6	50			50			50			ns
t _{WLWH}	WE# Pulse Width		40			50			50			ns
t _{WHDX}	Data Hold from WE# High	2	0			0			0			ns
t _{WHAX}	Address Hold from WE# High	2	10			10			10			ns
t _{WHEH}	CE# Hold from WE# High		10			10			10			ns
t _{WHWL}	WE# Pulse Width High		30			30			50			ns
t _{GHWL}	Read Recovery before Write		0			0			0			ns
t _{WHRL}	WE# High to RY/BY# Going Low				100			100			100	ns
t _{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			0			0			ns
t _{PHWL}	RP# High Recovery to WE# Going Low		1			1			1			μs
t _{WHGL}	Write Recovery before Read		60			65			80			ns
t _{QVVL}	V _{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High		0			0			0			μs
t _{WHQV1}	Duration of Word/Byte Write Operation	4,5	4.5	6		4.5	6		4.5	6		μs
t _{WHQV2}	Duration of Block Erase Operation	4	0.3			0.3			0.3			s

NOTES:

CE# is defined as the latter of CE₀# or CE₁# going Low or the first of CE₀# or CE₁# going High.

1. Read timing during write and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, but not 100% tested.
4. Write/Erase durations are measured to valid Status Register (CSR) Data.
5. Word/Byte write operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of WE# for all Command Write operations.

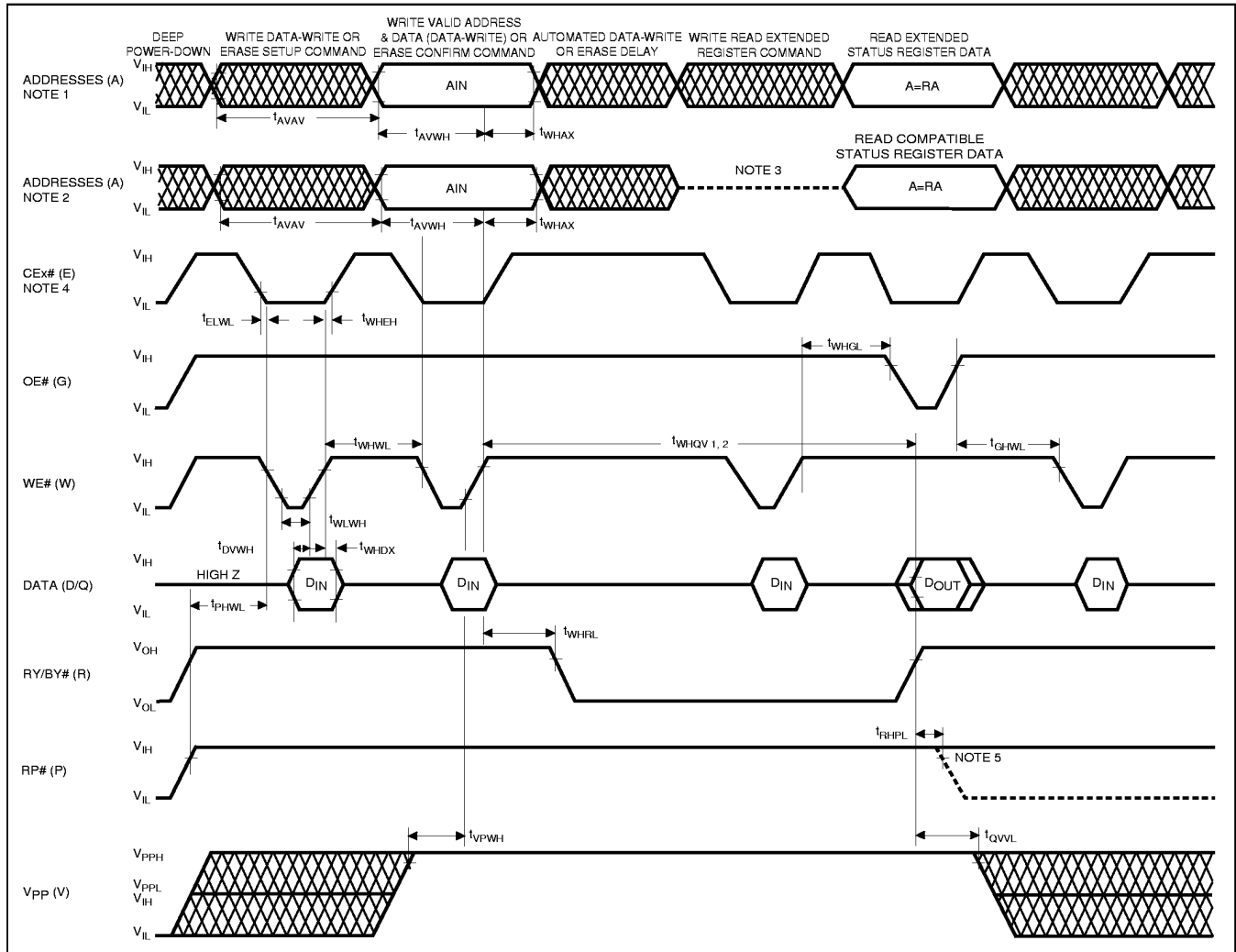


Figure 13. AC Waveforms for Command Write Operations

NOTES:

1. This address string depicts Data-Write/Erase cycles with corresponding verification via ESRD.
2. This address string depicts Data-Write/Erase cycles with corresponding verification via CSRD.
3. This cycle is invalid when using CSRD for verification during Data-Write/Erase operations.
4. $CE_x\#$ is defined as the latter of $CE_0\#$ or $CE_1\#$ going Low or the first of $CE_0\#$ or $CE_1\#$ going High.
5. RP# low transition is only to show t_{RHPL} ; not valid for above Read and Write cycles.

5.9 AC Characteristics for CE# - Controlled Command Write Operations ⁽¹⁾

V_{CC} = 3.3 V ±0.3 V, T_A = 0°C to 70°C

Versions			LH28F016SA-120			LH28F016SA-150			Unit
Symbol	Parameter	Notes	Min	Typ	Max	Min	Typ	Max	
t _{AVAV}	Write Cycle Time		120			150			ns
t _{PHWL}	RP# Setup to WE# Going Low		480			480			ns
t _{VPEH}	V _{PP} Setup to CE# Going High	3	100			100			ns
t _{WLEL}	WE# Setup to CE# Going Low		0			0			ns
t _{AVEH}	Address Setup to CE# Going High	2,6	75			75			ns
t _{DVEH}	Data Setup to CE# Going High	2,6	75			75			ns
t _{ELEH}	CE# Pulse Width		75			75			ns
t _{EHDX}	Data Hold from CE# High	2	10			10			ns
t _{EHAX}	Address Hold from CE# High	2	10			10			ns
t _{EHWH}	WE# Hold from CE# High		10			10			ns
t _{EHEL}	CE# Pulse Width High		45			75			ns
t _{GHEL}	Read Recovery before Write		0			0			ns
t _{EHRL}	CE# High to RY/BY# Going Low		0		100			100	ns
t _{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			0			ns
t _{PHEL}	RP# High Recovery to CE# Going Low		1			1			μs
t _{EHGL}	Write Recovery before Read		95			120			ns
t _{QVVL}	V _{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High		0			0			μs
t _{EHQV1}	Duration of Word/Byte Write Operation	4,5	5	9		5	9		μs
t _{EHQV2}	Duration of Block Erase Operation	4	0.3			0.3			s

AC Characteristics for CE# - Controlled Command Write Operations ⁽¹⁾ (Continued)V_{CC} = 5.0 V ±0.5 V, T_A = 0°C to 70°C

Versions		VCC ± 5%	LH28F016SA-070									Unit
		VCC ± 10%				LH28F016SA-080			LH28F016SA-100			
Symbol	Parameter	Notes	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _{AVAV}	Write Cycle Time		70			80			100			ns
t _{PHWL}	RP# Setup to WE# Going Low	3	480			480			480			ns
t _{VPEH}	V _{PP} Setup to CE# Going High	3	100			100			100			ns
t _{WLEL}	WE# Setup to CE# Going Low		0			0			0			ns
t _{AVEH}	Address Setup to CE# Going High	2,6	50			50			50			ns
t _{DVEH}	Data Setup to CE# Going High	2,6	50			50			50			ns
t _{ELEH}	CE# Pulse Width		40			50			50			ns
t _{EHDX}	Data Hold from CE# High	2	0			0			0			ns
t _{EHAX}	Address Hold from CE# High	2	10			10			10			ns
t _{EHWH}	WE# Hold from CE# High		10			10			10			ns
t _{EHEL}	CE# Pulse Width High		30			30			50			ns
t _{GHLEL}	Read Recovery before Write		0			0			0			ns
t _{EHRL}	CE# High to RY/BY# Going Low				100			100			100	ns
t _{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			0			0			ns
t _{PHLEL}	RP# High Recovery to CE# Going Low		1			1			1			μs
t _{EHGL}	Write Recovery before Read		60			65			80			ns
t _{QVVL}	V _{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High		0			0			0			μs
t _{EHQV1}	Duration of Word/Byte Write Operation	4,5	4.5	6		4.5	6		4.5	6		μs
t _{EHQV2}	Duration of Block Erase Operation	4	0.3			0.3			0.3			s

NOTES:CE# is defined as the latter of CE₀# or CE₁# going Low or the first of CE₀# or CE₁# going High.

1. Read timing during write and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, but not 100% tested.
4. Write/Erase durations are measured to valid Status Data.
5. Word/Byte write operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of CE# for all Command Write Operations.

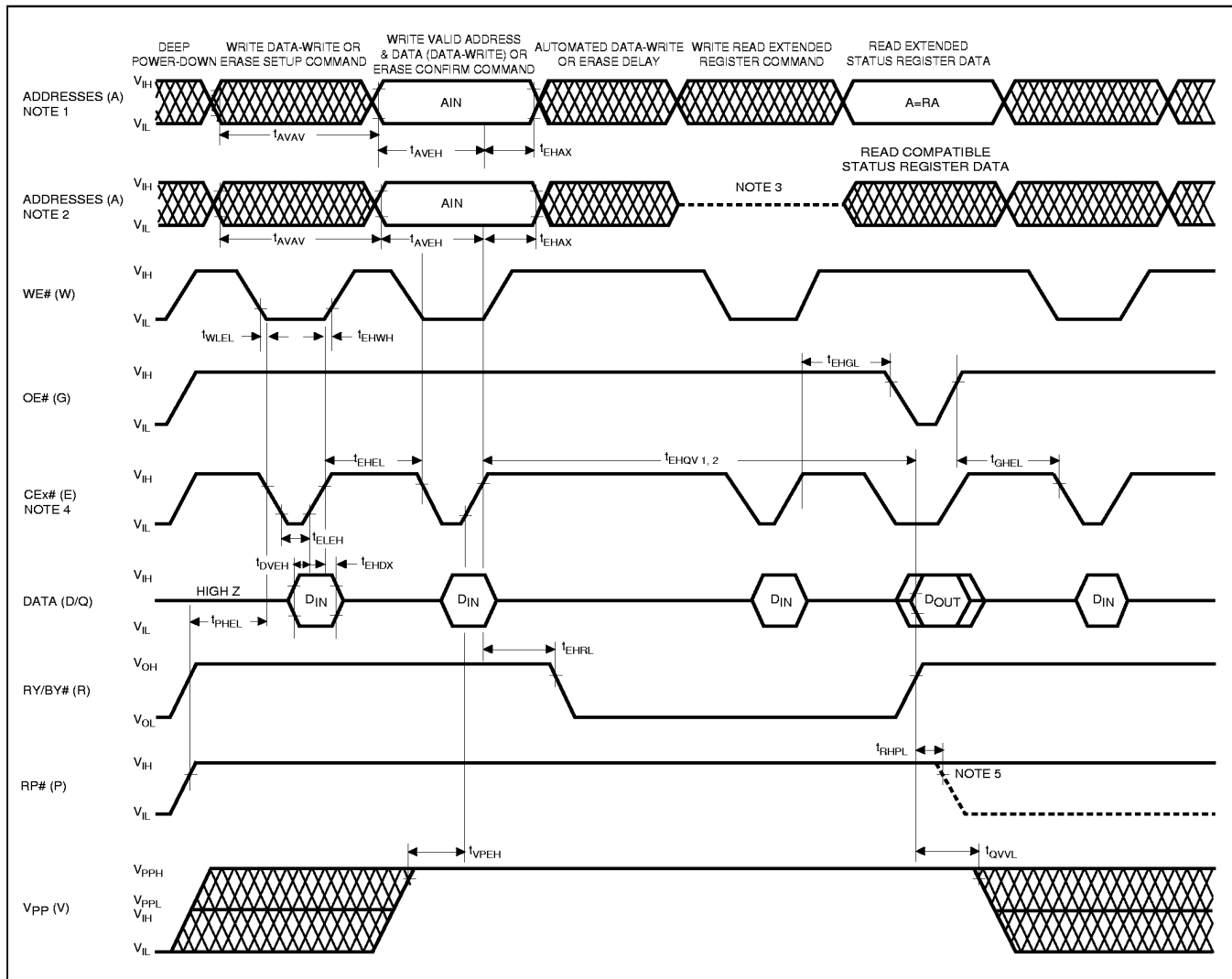


Figure 14. Alternate AC Waveforms for Command Write Operations

NOTES:

1. This address string depicts Data-Write/Erase cycles with corresponding verification via ESRD.
2. This address string depicts Data-Write/Erase cycles with corresponding verification via CSRD.
3. This cycle is invalid when using CSRD for verification during Data-Write/Erase operations.
4. CE_x# is defined as the latter of CE₀# or CE₁# going Low or the first of CE₀# or CE₁# going High.
5. RP# low transition is only to show t_{RHPL}; not valid for above Read and Write cycles.

5.10 AC Characteristics for Page Buffer Write Operations ⁽¹⁾

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$

Versions			LH28F016SA-120			LH28F016SA-150			Unit
Symbol	Parameter	Notes	Min	Typ	Max	Min	Typ	Max	
t_{AVAV}	Write Cycle Time		120			150			ns
t_{ELWL}	CE# Setup to WE# Going Low		10			10			ns
t_{AVWL}	Address Setup to WE# Going Low	3	0			0			ns
t_{DVWH}	Data Setup to WE# Going High	2	75			50			ns
t_{WLWH}	WE# Pulse Width		75			75			ns
t_{WHDX}	Data Hold from WE# High	2	10			10			ns
t_{WHAX}	Address Hold from WE# High	2	10			10			ns
t_{WHEH}	CE# Hold from WE# High		10			10			ns
t_{WHWL}	WE# Pulse Width High		45			75			ns
t_{GHWL}	Read Recovery before Write		0			0			ns
t_{WHGL}	Write Recovery before Read		95			120			ns

$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$

Versions			LH28F016SA-070			LH28F016SA-080			LH28F016SA-100			Unit
Symbol	Parameter	Notes	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{AVAV}	Write Cycle Time		70			80			100			ns
t_{ELWL}	CE# Setup to WE# Going Low		0			0			0			ns
t_{AVWL}	Address Setup to WE# Going Low	3	0			0			0			ns
t_{DVWH}	Data Setup to WE# Going High	2	50			50			50			ns
t_{WLWH}	WE# Pulse Width		40			50			50			ns
t_{WHDX}	Data Hold from WE# High	2	0			0			0			ns
t_{WHAX}	Address Hold from WE# High	2	10			10			10			ns
t_{WHEH}	CE# Hold from WE# High		10			10			10			ns
t_{WHWL}	WE# Pulse Width High		30			30			50			ns
t_{GHWL}	Read Recovery before Write		0			0			0			ns
t_{WHGL}	Write Recovery before Read		60			65			80			ns

NOTES:

CE# is defined as the latter of CE₀# or CE₁# going Low or the first of CE₀# or CE₁# going High.

1. These are WE#-controlled write timings, equivalent CE#-controlled write timings apply.
2. Sampled, but not 100% tested.
3. Address must be valid during the entire WE# Low pulse.

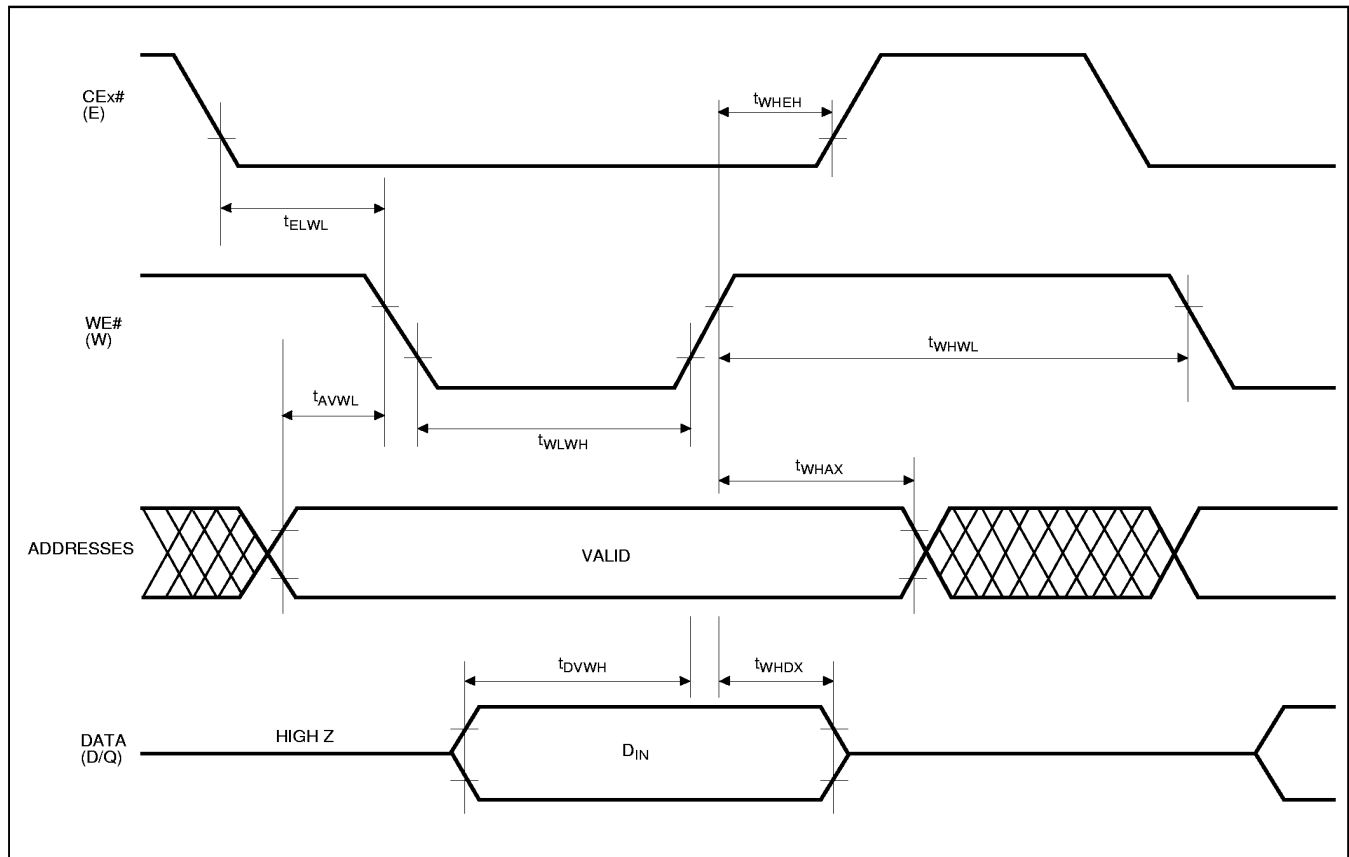


Figure 15. Page Buffer Write Timing Waveforms

5.11 Erase and Word/Byte Write Performance ⁽³⁾

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$

Symbol	Parameter	Notes	Min	Typ ⁽¹⁾	Max	Units	Test Conditions
t _{WHRH1}	Word/Byte Write Time	2		9		μs	
t _{WHRH2}	Block Write Time	2		0.6	2.1	s	Byte Write Mode
t _{WHRH3}	Block Write Time	2		0.3	1.0	s	Word Write Mode
	Block Erase Time	2		0.8	10	s	
	Full Chip Erase Time	2		25.6		s	

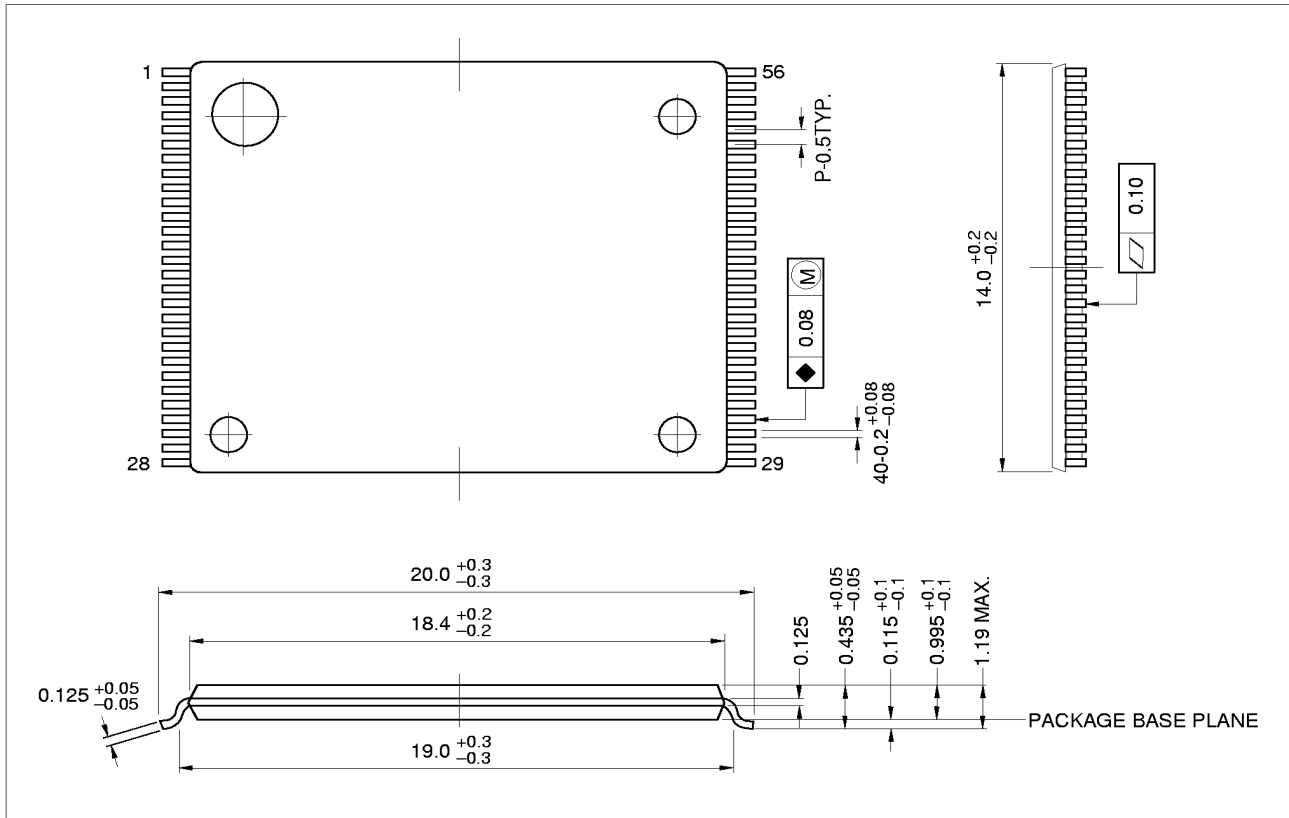
$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$

Symbol	Parameter	Notes	Min	Typ ⁽¹⁾	Max	Units	Test Conditions
t _{WHRH1}	Word/Byte Write Time	2		6		μs	
t _{WHRH2}	Block Write Time	2		0.4	2.1	s	Byte Write Mode
t _{WHRH3}	Block Write Time	2		0.2	1.0	s	Word Write Mode
	Block Erase Time	2		0.6	10	s	
	Full Chip Erase Time	2		19.2		s	

NOTES:

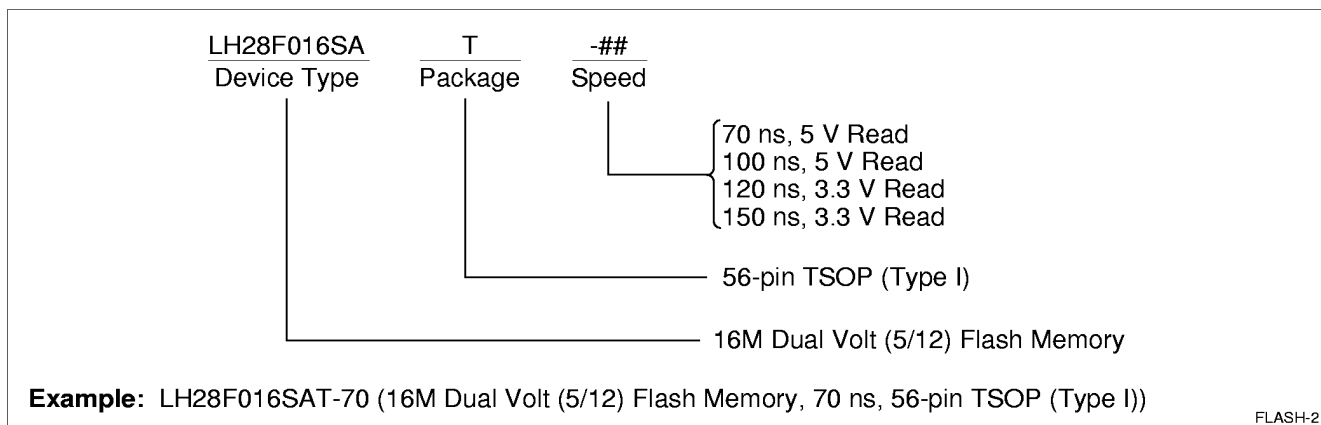
1. 25°C , $V_{PP} = 12.0\text{ V}$.
2. Excludes System-Level Overhead.
3. These performance numbers are valid for all speed versions.

PACKAGE DIAGRAM



56-Lead TSOP (Type I)

ORDERING INFORMATION



FLASH-2