

PRELIMINARY DATASHEET

## DATASHEET

**PRODUCT :** 4M (x8/x16) Flash Memory

**MODEL No :** ***LH28F400BVHE-TL85***

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## LH28F400BVHE-TL85

### 4M-BIT (512Kbit × 8 / 256Kbit × 16)

### SmartVoltage Flash MEMORY

- SmartVoltage Technology
  - 2.7V, 3.3V or 5V  $V_{CC}$
  - 2.7V, 3.3V, 5V or 12V  $V_{PP}$
- User-Configurable ×8 or ×16 Operation
- High-Performance Access Time
  - 85ns(5V±0.25V), 90ns(5V±0.5V),
  - 100ns(3.3V±0.3V), 120ns(2.7V-3.6V)
- Operating Temperature
  - -40°C to +85°C
- Optimized Array Blocking Architecture
  - Two 4K-word Boot Blocks
  - Six 4K-word Parameter Blocks
  - Seven 32K-word Main Blocks
  - Top Boot Location
- Extended Cycling Capability
  - 100,000 Block Erase Cycles
- Enhanced Automated Suspend Options
  - Word/Byte Write Suspend to Read
  - Block Erase Suspend to Word/Byte Write
  - Block Erase Suspend to Read
- Enhanced Data Protection Features
  - Absolute Protection with  $V_{PP}=GND$
  - Block Erase and Word/Byte Write Lockout during Power Transitions
  - Boot Blocks Protection with  $WP\#=V_{IL}$
- Automated Word/Byte Write and Block Erase
  - Command User Interface
  - Status Register
- Low Power Management
  - Deep Power-Down Mode
  - Automatic Power Savings Mode Decreases  $I_{CC}$  in Static Mode
- SRAM-Compatible Write Interface
- Industry-Standard Packaging
  - 48-Lead TSOP
- ETOX™\* Nonvolatile Flash Technology
- CMOS Process (P-type silicon substrate)
- Not designed or rated as radiation hardened

SHARP's LH28F400BVHE-TL85 Flash memory with SmartVoltage technology is a high-density, low-cost, nonvolatile, read/write storage solution for a wide range of applications. LH28F400BVHE-TL85 can operate at  $V_{CC}=2.7V$  and  $V_{PP}=2.7V$ . Its low voltage operation capability realize battery life and suits for cellular phone application.

Its Boot, Parameter and Main-blocked architecture, flexible voltage and extended cycling provide for highly flexible component suitable for portable terminals and personal computers. Its enhanced suspend capabilities provide for an ideal solution for code + data storage applications. For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the LH28F400BVHE-TL85 offers two levels of protection: absolute protection with  $V_{PP}$  at GND, selective hardware boot block locking. These alternatives give designers ultimate control of their code security needs.

The LH28F400BVHE-TL85 is manufactured on SHARP's 0.35 $\mu$ m ETOX™\* process technology. It come in industry-standard package: the 48-lead TSOP ideal for board constrained applications.

\*ETOX is a trademark of Intel Corporation.

## 1 INTRODUCTION

This datasheet contains LH28F400BVHE-TL85 specifications. Section 1 provides a flash memory overview. Sections 2, 3, 4 and 5 describe the memory organization and functionality. Section 6 covers electrical specifications.

### 1.1 Features

Key enhancements of LH28F400BVHE-TL85 SmartVoltage Flash memory are:

- SmartVoltage Technology
- Enhanced Suspend Capabilities
- Boot Block Architecture

Please note following important differences:

- $V_{PPLK}$  has been lowered to 1.5V to support 2.7V, 3.3V and 5V block erase and word/byte write operations. The  $V_{PP}$  voltage transitions to GND is recommended for designs that switch  $V_{PP}$  off during read operation.
- To take advantage of SmartVoltage technology, allow  $V_{CC}$  and  $V_{PP}$  connection to 2.7V, 3.3V or 5V.

### 1.2 Product Overview

The LH28F400BVHE-TL85 is a high-performance 4M-bit SmartVoltage Flash memory organized as 512K-byte of 8 bits or 256K-word of 16 bits. The 512K-byte/256K-word of data is arranged in two 8K-byte/4K-word boot blocks, six 8K-byte/4K-word parameter blocks and seven 64K-byte/32K-word main blocks which are individually erasable in-system. The memory map is shown in Figure 3.

SmartVoltage technology provides a choice of  $V_{CC}$  and  $V_{PP}$  combinations, as shown in Table 1, to meet system performance and power expectations. 2.7V  $V_{CC}$  consumes approximately one-fifth the power of 5V  $V_{CC}$ . But, 5V

$V_{CC}$  provides the highest read performance.  $V_{PP}$  at 2.7, 3.3V and 5V eliminates the need for a separate 12V converter, while  $V_{PP}=12V$  maximizes block erase and word/byte write performance. In addition to flexible erase and program voltages, the dedicated  $V_{PP}$  pin gives complete data protection when  $V_{PP} \leq V_{PPLK}$ .

Table 1.  $V_{CC}$  and  $V_{PP}$  Voltage Combinations Offered by SmartVoltage Technology

$V_{CC}$ Voltage	$V_{PP}$ Voltage
2.7V	2.7V, 3.3V, 5V, 12V
3.3V	3.3V, 5V, 12V
5V	5V, 12V

Internal  $V_{CC}$  and  $V_{PP}$  detection Circuitry automatically configures the device for optimized read and write operations.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase and word/byte write operations.

A block erase operation erases one of the device's 32K-word blocks typically within 0.39s (5V  $V_{CC}$ , 12V  $V_{PP}$ ), 4K-word blocks typically within 0.25s (5V  $V_{CC}$ , 12V  $V_{PP}$ ) independent of other blocks. Each block can be independently erased 100,000 times. Block erase suspend mode allows system software to suspend block erase to read or write data from any other block.

Writing memory data is performed in word/byte increments of the device's 32K-word blocks typically within 8.4 $\mu$ s (5V  $V_{CC}$ , 12V  $V_{PP}$ ), 4K-word blocks typically within 17 $\mu$ s (5V  $V_{CC}$ , 12V  $V_{PP}$ ). Word/byte write suspend mode enables the system to read data or execute code from any other flash memory array location.

The boot blocks can be locked for the WP# pin. Block erase or word/byte write for boot block must not be carried out by WP# to Low and RP# to V<sub>IH</sub>.

The status register indicates when the WSM's block erase or word/byte write operation is finished.

The RY/BY# output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status polling using RY/BY# minimizes both CPU overhead and system power consumption. When low, RY/BY# indicates that the WSM is performing a block erase or word/byte write. RY/BY#-high indicates that the WSM is ready for a new command, block erase is suspended (and word/byte write is inactive), word/byte write is suspended, or the device is in deep power-down mode.

The access time is 85ns ( $t_{AVQV}$ ) over the extended temperature range (-40°C to +85°C) and V<sub>CC</sub> supply voltage range of 4.75V-5.25V. At lower V<sub>CC</sub> voltages, the

access times are 90ns (4.5V-5.5V), 100ns (3.0V-3.6V) and 120ns (2.7V-3.6V).

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical I<sub>CCR</sub> current is 1mA at 5V V<sub>CC</sub>.

When CE# and RP# pins are at V<sub>CC</sub>, the I<sub>CC</sub> CMOS standby mode is enabled. When the RP# pin is at GND, deep power-down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time ( $t_{PHQV}$ ) is required from RP# switching high until outputs are valid. Likewise, the device has a wake time ( $t_{PHEL}$ ) from RP#-high until writes to the CUI are recognized. With RP# at GND, the WSM is reset and the status register is cleared.

The device is available in 48-lead TSOP (Thin Small Outline Package, 1.2 mm thick). Pinout is shown in Figure 2.

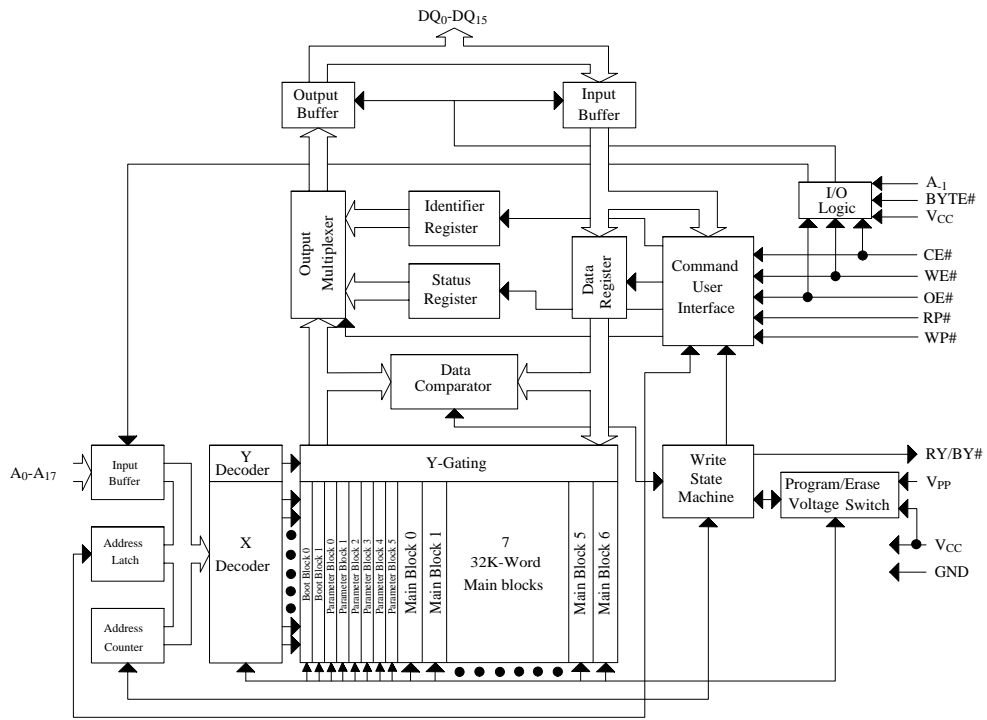


Figure 1. Block Diagram

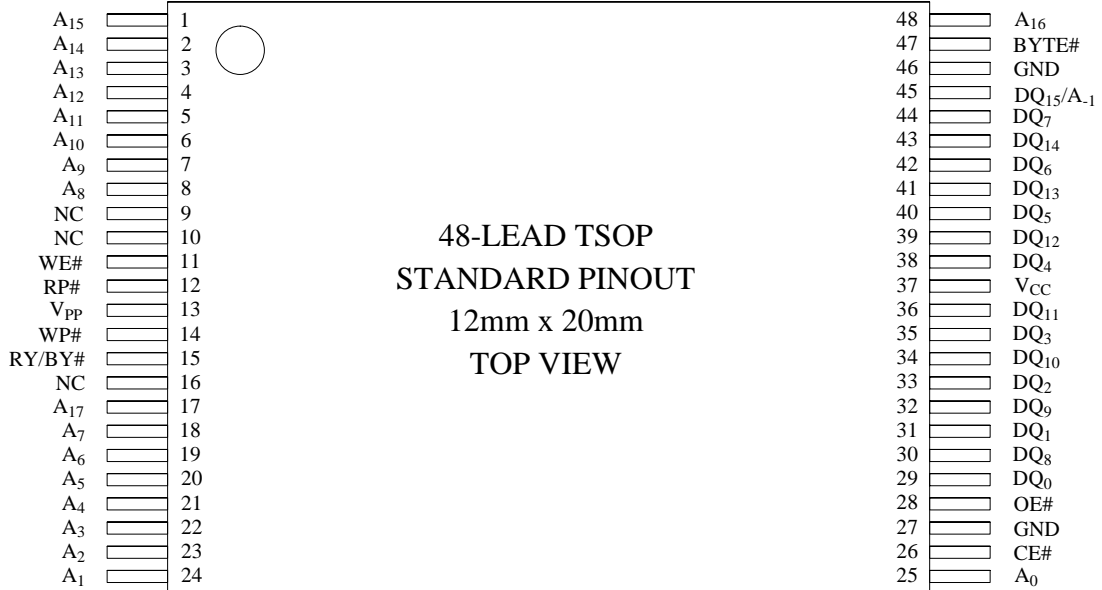


Figure 2. TSOP 48-Lead Pinout

Table 2. Pin Descriptions

Symbol	Type	Name and Function
$A_{-1}$ $A_0$ - $A_{17}$	INPUT	ADDRESS INPUTS: Addresses are internally latched during a write cycle. A-1 : Byte Select Address. Not used in $\times 16$ mode. A0-A10 : Row Address. Selects 1 of 2048 word lines. A11-A14 : Column Address. Selects 1 of 16 bit lines. A15-A17 : Main Block Address. (Boot and Parameter block Addresses are $A_{12}$ - $A_{17}$ .)
$DQ_0$ - $DQ_{15}$	INPUT/ OUTPUT	DATA INPUT/OUTPUTS: $DQ_0$ - $DQ_7$ :Inputs data and commands during CUI write cycles; outputs data during memory array, status register and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle. $DQ_8$ - $DQ_{15}$ :Inputs data during CUI write cycles in $\times 16$ mode; outputs data during memory array read cycles in $\times 16$ mode; not used for status register and identifier code read mode. Data pins float to high-impedance when the chip is deselected, outputs are disabled, or in $\times 8$ mode(Byte#= $V_{IL}$ ). Data is internally latched during a write cycle.
CE#	INPUT	CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. CE#-high deselected the device and reduces power consumption to standby levels.
RP#	INPUT	RESET/DEEP POWER-DOWN: Puts the device in deep power-down mode and resets internal automation. RP#-high enables normal operation. When driven low, RP# inhibits write operations which provides data protection during power transitions. Exit from deep power-down sets the device to read array mode. With $RP\#=V_{HH}$ , block erase or word/byte write can operate to all blocks without WP# state. Block erase or word/byte write with $V_{IH}<RP\#<V_{HH}$ produce spurious results and should not be attempted.
OE#	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
WE#	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the WE# pulse.
WP#	INPUT	WRITE PROTECT: Master control for boot blocks locking. When $V_{IL}$ , locked boot blocks cannot be erased and programmed.
BYTE#	INPUT	BYTE ENABLE: BYTE# $V_{IL}$ places device in $\times 8$ mode. All data is then input or output on $DQ_{0-7}$ , and $DQ_{8-15}$ float. BYTE# $V_{IH}$ places the device in $\times 16$ mode, and turns off the $A_{-1}$ input buffer.
RY/BY#	OUTPUT	READY/BUSY#: Indicates the status of the internal WSM. When low, the WSM is performing an internal operation (block erase or word/byte write). RY/BY#-high indicates that the WSM is ready for new commands, block erase is suspended, and word/byte write is inactive, word/byte write is suspended, or the device is in deep power-down mode. RY/BY# is always active and does not float when the chip is deselected or data outputs are disabled.
$V_{PP}$	SUPPLY	BLOCK ERASE AND WORD/BYTE WRITE POWER SUPPLY: For erasing array blocks or writing words/bytes. With $V_{PP}\leq V_{PPLK}$ , memory contents cannot be altered. Block erase and word/byte write with an invalid $V_{PP}$ (see DC Characteristics) produce spurious results and should not be attempted.
$V_{CC}$	SUPPLY	DEVICE POWER SUPPLY: Internal detection configures the device for 2.7V, 3.3V or 5V operation. To switch from one voltage to another, ramp $V_{CC}$ down to GND and then ramp $V_{CC}$ to the new voltage. Do not float any power pins. With $V_{CC}\leq V_{LKO}$ , all write attempts to the flash memory are inhibited. Device operations at invalid $V_{CC}$ voltage (see DC Characteristics) produce spurious results and should not be attempted.
GND	SUPPLY	GROUND: Do not float any ground pins.
NC		NO CONNECT: Lead is not internal connected; it may be driven or floated.



## 2 PRINCIPLES OF OPERATION

The LH28F400BVHE-TL85 SmartVoltage Flash memory includes an on-chip WSM to manage block erase and word/byte write functions. It allows for: 100% TTL-level control inputs, fixed power supplies during block erasure and word/byte write, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from deep power-down mode (see Bus Operations), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby and output disable operations.

Status register and identifier codes can be accessed through the CUI independent of the  $V_{PP}$  voltage. High voltage on  $V_{PP}$  enables successful block erasure and word/byte writing. All functions associated with altering memory contents—block erase, word/byte write, status and identifier codes—are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the block erase and word/byte write. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification and margining of data. Addresses and data are internally latch during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes or outputs status register data.

Interface software that initiates and polls progress of block erase and word/byte write can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read/write data from/to blocks other than that which is suspend. Word/byte write suspend allows system software to suspend a word/byte write to read data from any other flash memory array location.

Top Boot		
3FFFF	4K-word Boot Block	0
3F000 3EFFF	4K-word Boot Block	1
3E000 3DFFF	4K-word Parameter Block	0
3D000 3CFFF	4K-word Parameter Block	1
3C000 3BFFF	4K-word Parameter Block	2
3B000 3AFFF	4K-word Parameter Block	3
3A000 39FFF	4K-word Parameter Block	4
39000 38FFF	4K-word Parameter Block	5
38000 37FFF	32K-word Main Block	0
30000 2FFFF	32K-word Main Block	1
28000 27FFF	32K-word Main Block	2
20000 1FFFF	32K-word Main Block	3
18000 17FFF	32K-word Main Block	4
10000 0FFFF	32K-word Main Block	5
08000 07FFF	32K-word Main Block	6
00000		

Figure 3. Memory Map

### 2.1 Data Protection

Depending on the application, the system designer may choose to make the  $V_{PP}$  power supply switchable (available only when memory block erases or word/byte writes are required) or hardwired to  $V_{PPH1/2/3}$ . The device accommodates either design practice and encourages optimization of the processor-memory interface.

When  $V_{PP} \leq V_{PPLK}$ , memory contents cannot be altered. The CUI, with two-step block erase or word/byte write command sequences, provides protection from unwanted operations even when high voltage is applied to  $V_{PP}$ . All write functions are disabled when  $V_{CC}$  is below the write lockout voltage  $V_{LKO}$  or when  $RP\#$  is at  $V_{IL}$ . The device's boot blocks locking capability for  $WP\#$  provides additional protection from inadvertent code or data alteration by block erase and word/byte write operations. Refer to Table 6 for write protection alternatives.

### 3 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

#### 3.1 Read

Information can be read from any block, identifier codes or status register independent of the  $V_{PP}$  voltage. RP# can be at either  $V_{IH}$  or  $V_{HH}$ .

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to read array mode. Six control pins dictate the data flow in and out of the component: CE#, OE#, WE#, RP#, WP# and BYTE#. CE# and OE# must be driven active to obtain data at the outputs. CE# is the device selection control, and when active enables the selected memory device. OE# is the data output (DQ<sub>0</sub>-DQ<sub>15</sub>) control and when active drives the selected memory data onto the I/O bus. WE# must be at  $V_{IH}$  and RP# must be at  $V_{IH}$  or  $V_{HH}$ . Figure 13, 14 illustrates read cycle.

#### 3.2 Output Disable

With OE# at a logic-high level ( $V_{IH}$ ), the device outputs are disabled. Output pins (DQ<sub>0</sub>-DQ<sub>15</sub>) are placed in a high-impedance state.

#### 3.3 Standby

CE# at a logic-high level ( $V_{IH}$ ) places the device in standby mode which substantially reduces device power consumption. DQ<sub>0</sub>-DQ<sub>15</sub> outputs are placed in a high-impedance state independent of OE#. If deselected during

block erase or word/byte write, the device continues functioning, and consuming active power until the operation completes.

#### 3.4 Deep Power-Down

RP# at  $V_{IL}$  initiates the deep power-down mode.

In read modes, RP#-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. RP# must be held low for a minimum of 100ns. Time  $t_{PHQV}$  is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase or word/byte write modes, RP#-low will abort the operation. RY/BY# remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written. Time  $t_{PHWL}$  is required after RP# goes to logic-high ( $V_{IH}$ ) before another command can be written.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase or word/byte write modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. SHARP's flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

### 3.5 Read Identifier Codes Operation

The read identifier codes operation outputs the manufacturer code and device code (see Figure 4). Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms.

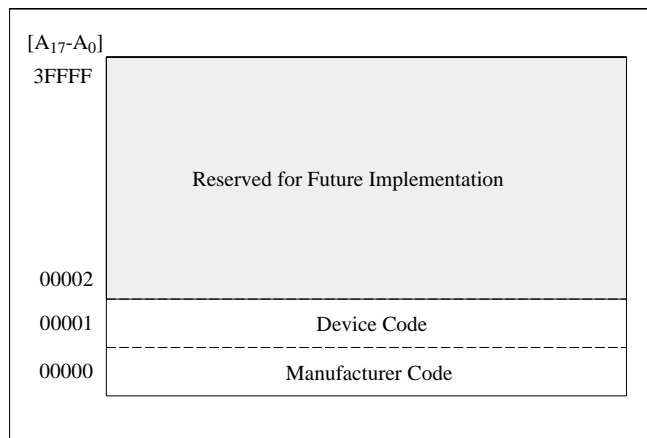


Figure 4. Device Identifier Code Memory Map

### 3.6 Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register. When  $V_{CC}=V_{CC1/2/3/4}$  and

$V_{PP}=V_{PPH1/2/3}$ , the CUI additionally controls block erasure and word/byte write.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Word/Byte Write command requires the command and address of the location to be written.

The CUI does not occupy an addressable memory location. It is written when WE# and CE# are active. The address and data needed to execute a command are latched on the rising edge of WE# or CE# (whichever goes high first). Standard microprocessor write timings are used. Figures 15 and 16 illustrate WE# and CE# controlled write operations.

## 4 COMMAND DEFINITIONS

When the  $V_{PP}$  voltage  $\leq V_{PPLK}$ , Read operations from the status register, identifier codes, or blocks are enabled. Placing  $V_{PPH1/2/3}$  on  $V_{PP}$  enables successful block erase and word/byte write operations.

Device operations are selected by writing specific commands into the CUI. Table 4 defines these commands.

Table 3.1. Bus Operations(BYTE#=V<sub>IH</sub>)<sup>(1,2)</sup>

Mode	Notes	RP#	CE#	OE#	WE#	Address	V <sub>PP</sub>	DQ <sub>0-15</sub>	RY/BY# <sup>(3)</sup>
Read	8	V <sub>IH</sub> or V <sub>HH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	X	X	D <sub>OUT</sub>	X
Output Disable		V <sub>IH</sub> or V <sub>HH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	X	X	High Z	X
Standby	10	V <sub>IH</sub> or V <sub>HH</sub>	V <sub>IH</sub>	X	X	X	X	High Z	X
Deep Power-Down	4,10	V <sub>IL</sub>	X	X	X	X	X	High Z	V <sub>OH</sub>
Read Identifier Codes	8	V <sub>IH</sub> or V <sub>HH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	See Figure 4	X	Note 5	V <sub>OH</sub>
Write	6,7,8	V <sub>IH</sub> or V <sub>HH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	X	X	D <sub>IN</sub>	X

Table 3.2. Bus Operations(BYTE#=V<sub>IL</sub>)<sup>(1,2)</sup>

Mode	Notes	RP#	CE#	OE#	WE#	Address	V <sub>PP</sub>	DQ <sub>0-7</sub>	DQ <sub>8-15</sub>	RY/BY# <sup>(3)</sup>
Read	8	V <sub>IH</sub> or V <sub>HH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	X	X	D <sub>OUT</sub>	High Z	X
Output Disable		V <sub>IH</sub> or V <sub>HH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	X	X	High Z	High Z	X
Standby	10	V <sub>IH</sub> or V <sub>HH</sub>	V <sub>IH</sub>	X	X	X	X	High Z	High Z	X
Deep Power-Down	4,10	V <sub>IL</sub>	X	X	X	X	X	High Z	High Z	V <sub>OH</sub>
Read Identifier Codes	8,9	V <sub>IH</sub> or V <sub>HH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	See Figure 4	X	Note 5	High Z	V <sub>OH</sub>
Write	6,7,8	V <sub>IH</sub> or V <sub>HH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	X	X	D <sub>IN</sub>	X	X

## NOTES:

1. Refer to DC Characteristics. When V<sub>PP</sub> ≤ V<sub>PPLK</sub>, memory contents can be read, but not altered.
2. X can be V<sub>IL</sub> or V<sub>IH</sub> for control pins and addresses, and V<sub>PPLK</sub> or V<sub>PPH1/2/3</sub> for V<sub>PP</sub>. See DC Characteristics for V<sub>PPLK</sub> and V<sub>PPH1/2/3</sub> voltages.
3. RY/BY# is V<sub>OL</sub> when the WSM is executing internal block erase or word/byte write algorithms. It is V<sub>OH</sub> during when the WSM is not busy, in block erase suspend mode (with word/byte write inactive), word/byte write suspend mode or deep power-down mode.
4. RP# at GND±0.2V ensures the lowest deep power-down current.
5. See Section 4.2 for read identifier code data.
6. Command writes involving block erase or word/byte write are reliably executed when V<sub>PP</sub>=V<sub>PPH1/2/3</sub> and V<sub>CC</sub>=V<sub>CC1/2/3/4</sub>. Block erase or word/byte write with V<sub>IH</sub><RP#<V<sub>HH</sub> produce spurious results and should not be attempted.
7. Refer to Table 4 for valid D<sub>IN</sub> during a write operation.
8. Never hold OE# low and WE# low at the same timing.
9. A<sub>-1</sub> set to V<sub>IL</sub> or V<sub>IH</sub> in byte mode (BYTE#=V<sub>IL</sub>).
10. WP# set to V<sub>IL</sub> or V<sub>IH</sub>.

Table 4. Command Definitions<sup>(7)</sup>

Command	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
			Oper <sup>(1)</sup>	Addr <sup>(2)</sup>	Data <sup>(3)</sup>	Oper <sup>(1)</sup>	Addr <sup>(2)</sup>	Data <sup>(3)</sup>
Read Array/Reset	1		Write	X	FFH			
Read Identifier Codes	≥2	4	Write	X	90H	Read	IA	ID
Read Status Register	2		Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Word/Byte Write	2	5,6	Write	WA	40H or 10H	Write	WA	WD
Block Erase and Word/Byte Write Suspend	1	5	Write	X	B0H			
Block Erase and Word/Byte Write Resume	1	5	Write	X	D0H			

## NOTES:

- BUS operations are defined in Table 3.1 and Table 3.2.
- X=Any valid address within the device.  
IA=Identifier Code Address: see Figure 4. A<sub>1</sub> set to V<sub>IL</sub> or V<sub>IH</sub> in Byte Mode (BYTE#=V<sub>IL</sub>).  
BA=Address within the block being erased. The each block can select by the address pin A<sub>17</sub> through A<sub>12</sub> combination.  
WA=Address of memory location to be written.
- SRD=Data read from status register. See Table 7 for a description of the status register bits.  
WD=Data to be written at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).  
ID=Data read from identifier codes.
- Following the Read Identifier Codes command, read operations access manufacturer and device codes. See Section 4.2 for read identifier code data.
- If the block is boot block, WP# must be at V<sub>IH</sub> or RP# must be at V<sub>HH</sub> to enable block erase or word/byte write operations. Attempts to issue a block erase or word/byte write to a boot block while WP# is V<sub>IH</sub> or RP# is V<sub>IH</sub>.
- Either 40H or 10H are recognized by the WSM as the word/byte write setup.
- Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

## 4.1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase or word/byte write, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend or Word/Byte Write Suspend command. The Read Array command functions independently of the  $V_{PP}$  voltage and RP# can be  $V_{IH}$  or  $V_{HH}$ .

## 4.2 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 4 retrieve the manufacturer and device codes (see Table 5 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the  $V_{PP}$  voltage and RP# can be  $V_{IH}$  or  $V_{HH}$ . Following the Read Identifier Codes command, the following information can be read:

Table 5. Identifier Codes

Code	Address [A <sub>17</sub> -A <sub>0</sub> ]	Data [DQ <sub>7</sub> -DQ <sub>0</sub> ]
Manufacture Code	00000H	B0H
Device Code	00001H	58H

## 4.3 Read Status Register Command

The status register may be read to determine when a block erase or word/byte write is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of OE# or CE#, whichever occurs. OE# or CE# must toggle to  $V_{IH}$  before further reads to update the status register latch. The Read Status Register command functions independently of the  $V_{PP}$  voltage. RP# can be  $V_{IH}$  or  $V_{HH}$ .

## 4.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 or SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status

Register command. These bits indicate various failure conditions (see Table 7). By allowing system software to reset these bits, several operations (such as cumulatively erasing multiple blocks or writing several words/bytes in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied  $V_{PP}$  Voltage. RP# can be  $V_{IH}$  or  $V_{HH}$ . This command is not functional during block erase or word/byte write suspend modes.

## 4.5 Block Erase Command

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by an block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFFFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 5). The CPU can detect block erase completion by analyzing the output data of the RY/BY# pin or status register bit SR.7.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable block erasure can only occur when  $V_{CC}=V_{CC1/2/3/4}$  and  $V_{PP}=V_{PPH1/2/3}$ . In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while  $V_{PP}\leq V_{PPLK}$ , SR.3 and SR.5 will be set to "1". Successful block erase for boot blocks requires that the corresponding if set, that WP#= $V_{IH}$  or RP#= $V_{HH}$ . If block erase is attempted to boot block when the corresponding WP#= $V_{IL}$  or RP#= $V_{IH}$ , SR.1 and SR.5 will be set to "1". Block erase operations with  $V_{IH}<RP#<V_{HH}$  produce spurious results and should not be attempted.

## 4.6 Word/Byte Write Command

Word/byte write is executed by a two-cycle command sequence. Word/byte write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the word/byte write and write verify algorithms internally. After the word/byte write sequence is written, the device automatically outputs status register data when read (see Figure 6). The CPU can detect the completion of the word/byte write event by analyzing the RY/BY# pin or status register bit SR.7.

When word/byte write is complete, status register bit SR.4 should be checked. If word/byte write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable word/byte writes can only occur when  $V_{CC}=V_{CC1/2/3/4}$  and  $V_{PP}=V_{PPH1/2/3}$ . In the absence of this high voltage, memory contents are protected against word/byte writes. If word/byte write is attempted while  $V_{PP}\leq V_{PPLK}$ , status register bits SR.3 and SR.4 will be set to "1". Successful word/byte write for boot blocks requires that the corresponding if set, that  $WP#=V_{IH}$  or  $RP#=V_{HH}$ . If word/byte write is attempted to boot block when the corresponding  $WP#=V_{IL}$  or  $RP#=V_{IH}$ , SR.1 and SR.4 will be set to "1". Word/byte write operations with  $V_{IH}<RP#<V_{HH}$  produce spurious results and should not be attempted.

## 4.7 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or word/byte write data in another block of memory. Once the block-erase process starts,

writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to "1"). RY/BY# will also transition to  $V_{OH}$ . Specification  $t_{WHRH2}$  defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A Word/Byte Write command sequence can also be issued during erase suspend to program data in other blocks. Using the Word/Byte Write Suspend command (see Section 4.8), a word/byte write operation can also be suspended. During a word/byte write operation with block erase suspended, status register bit SR.7 will return to "0" and the RY/BY# output will transition to  $V_{OL}$ . However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and RY/BY# will return to  $V_{OL}$ . After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 7).  $V_{PP}$  must remain at  $V_{PPH1/2/3}$  (the same  $V_{PP}$  level used for block erase) while block erase is suspended.  $RP\#$  must also remain at  $V_{IH}$  or  $V_{HH}$  (the same  $RP\#$  level used for block erase).  $WP\#$  must also remain at  $V_{IL}$  or  $V_{IH}$  (the same  $WP\#$  level used for block erase). Block erase cannot resume until word/byte write operations initiated during block erase suspend have completed.

## 4.8 Word/Byte Write Suspend Command

The Word/Byte Write Suspend command allows word/byte write interruption to read data in other flash memory locations. Once the word/byte write process starts, writing the Word/Byte Write Suspend command requests that the WSM suspend the word/byte write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Word/Byte Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the word/byte write operation has been suspended (both will be set to "1"). RY/BY# will also transition to  $V_{OH}$ . Specification  $t_{WHRH1}$  defines the word/byte write suspend latency.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while word/byte write is suspended are Read Status Register and Word/Byte Write Resume. After Word/Byte Write Resume command is written to the flash memory, the WSM will continue the word/byte write process. Status register bits SR.2 and SR.7 will automatically clear and RY/BY# will return to  $V_{OL}$ . After the Word/Byte Write Resume command is written, the device automatically outputs status register data when read (see Figure 8).  $V_{PP}$  must remain at  $V_{PPH1/2/3}$  (the same  $V_{PP}$  level used for word/byte write) while in word/byte write suspend mode. RP# must also remain at  $V_{IH}$  or  $V_{HH}$  (the same RP# level used for word/byte write). WP# must also remain at  $V_{IL}$  or  $V_{IH}$  (the same WP# level used for word/byte write).

## 4.9 Considerations of Suspend

After the suspend command write to the CUI, read status register command has to write to CUI, then status register bit SR.6 or SR.2 should be checked for places the device in suspend mode.

## 4.10 Block Locking

This Boot Block Flash memory architecture features two hardware-lockable boot blocks so that the kernel code for the system can be kept secure while other blocks are programmed or erased as necessary.

### 4.10.1 $V_{PP}=V_{IL}$ for Complete Protection

The  $V_{PP}$  programming voltage can be held low for complete write protection of all blocks in the flash device.

### 4.10.2 $WP#=V_{IL}$ for Block Locking

The lockable blocks are locked when  $WP#=V_{IL}$ ; any program or erase operation to a locked block will result in an error, which will be reflected in the status register. For top configuration, the top two boot blocks are lockable. For the bottom configuration, the bottom two boot blocks are lockable. Unlocked blocks can be programmed or erased normally (Unless  $V_{PP}$  is below  $V_{PPLK}$ ).

### 4.10.3 $WP#=V_{IH}$ for Block Unlocking

$WP#=V_{IH}$  unlocks all lockable blocks.

These blocks can now be programmed or erased.

WP# controls 2 boot blocks locking and  $V_{PP}$  provides protection against spurious writes. Table 6 defines the write protection methods.

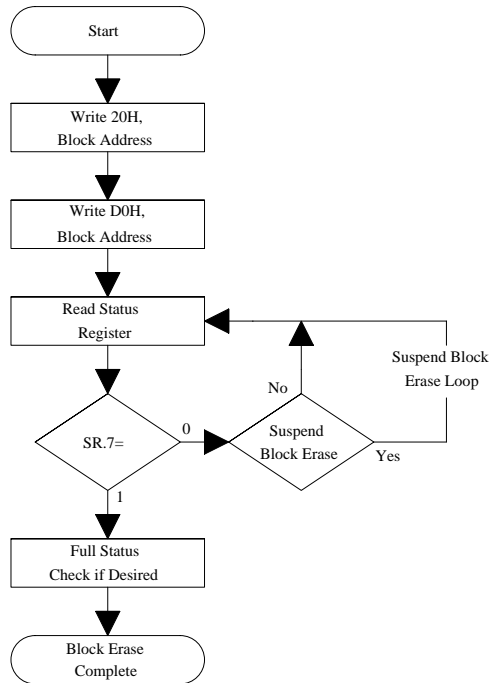
Table 6. Write Protection Alternatives

Operation	$V_{PP}$	RP#	WP#	Effect
Block Erase or Word/Byte Write	$V_{IL}$	X	X	All Blocks Locked.
	$>V_{PPLK}$	$V_{IL}$	X	All Blocks Locked.
		$V_{HH}$	X	All Blocks Unlocked.
		$V_{IH}$	$V_{IL}$	2 Boot Blocks Locked.
			$V_{IH}$	All Blocks Unlocked.



Table 7. Status Register Definition

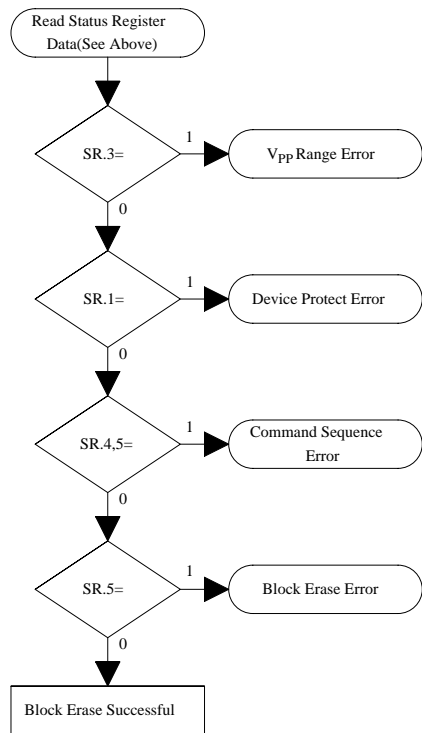
WSMS	ESS	ES	WBWS	VPPS	WBWSS	DPS	R
7	6	5	4	3	2	1	0
<p>SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy</p> <p>SR.6 = ERASE SUSPEND STATUS (ESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed</p> <p>SR.5 = ERASE STATUS (ES) 1 = Error in Block Erasure 0 = Successful Block Erase</p> <p>SR.4 = WORD/BYTE WRITE STATUS (WBWS) 1 = Error in Word/Byte Write 0 = Successful Word/Byte Write</p> <p>SR.3 = <math>V_{pp}</math> STATUS (VPPS) 1 = <math>V_{pp}</math> Low Detect, Operation Abort 0 = <math>V_{pp}</math> OK</p> <p>SR.2 = WORD/BYTE WRITE SUSPEND STATUS (WBWSS) 1 = Word/Byte Write Suspended 0 = Word/Byte Write in Progress/Completed</p> <p>SR.1 = DEVICE PROTECT STATUS (DPS) 1 = WP# or RP# Lock Detected, Operation Abort 0 = Unlock</p> <p>SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p>				<p>NOTES:</p> <p>Check RY/BY# or SR.7 to determine block erase or word/byte write completion. SR.6-0 are invalid while SR.7="0".</p> <p>If both SR.5 and SR.4 are "1"s after a block erase attempt, an improper command sequence was entered.</p> <p>SR.3 does not provide a continuous indication of <math>V_{pp}</math> level. The WSM interrogates and indicates the <math>V_{pp}</math> level only after Block Erase or Word/Byte Write command sequences. SR.3 is not guaranteed to reports accurate feedback only when <math>V_{pp} \neq V_{PPH1/2/3}</math>.</p> <p>The WSM interrogates the WP# and RP# only after Block Erase or Word/Byte Write command sequences. It informs the system, depending on the attempted operation, if the WP# is not <math>V_{IH}</math>, RP# is not <math>V_{HH}</math>.</p> <p>SR.0 is reserved for future use and should be masked out when polling the status register.</p>			



Bus Operation	Command	Comments
Write	Erase Setup	Data=20H Addr=Within Block to be Erased
Write	Erase Confirm	Data=D0H Addr=Within Block to be Erased
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent block erasures.  
Full status check can be done after each block erase or after a sequence of block erasures.  
Write FFH after the last operation to place device in read array mode.

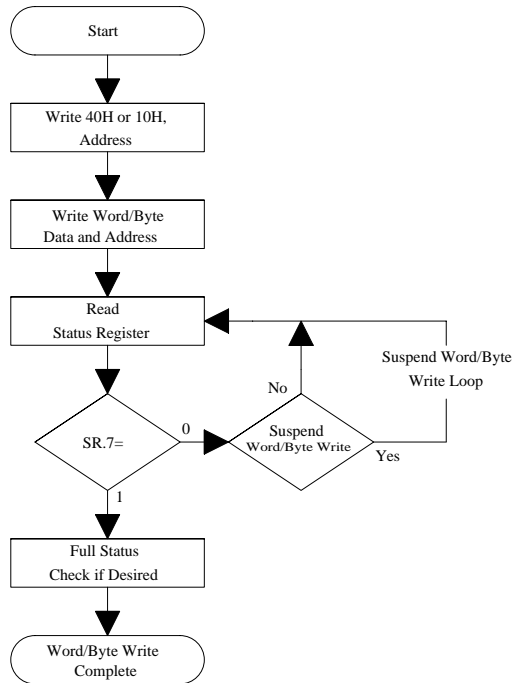
FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=Vpp Error Detect
Standby		Check SR.1 1=Device Protect Detect
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Block Erase Error

SR.5,SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked.  
If error is detected, clear the Status Register before attempting retry or other error recovery.

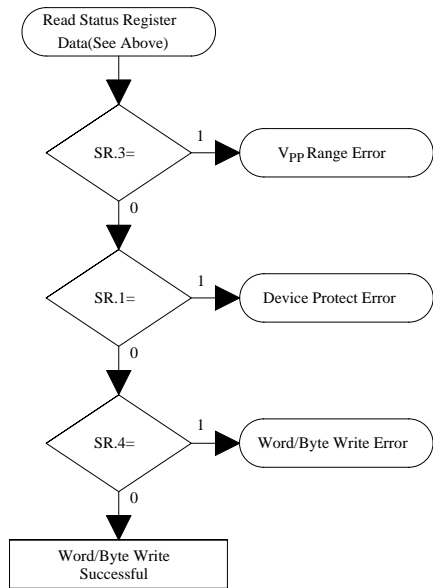
Figure 5. Automated Block Erase Flowchart



Bus Operation	Command	Comments
Write	Setup Word/Byte Write	Data=40H or 10H Addr=Location to Be Written
Write	Word/Byte Write	Data=Data to Be Written Addr=Location to Be Written
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent byte writes.  
 SR full status check can be done after each Word/Byte write, or after a sequence of Word/Byte writes.  
 Write FFH after the last Word/Byte write operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=Vpp Error Detect
Standby		Check SR.1 1=Device Protect Detect
Standby		Check SR.4 1=Data Write Error

SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked.  
 If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 6. Automated Word/Byte Write Flowchart

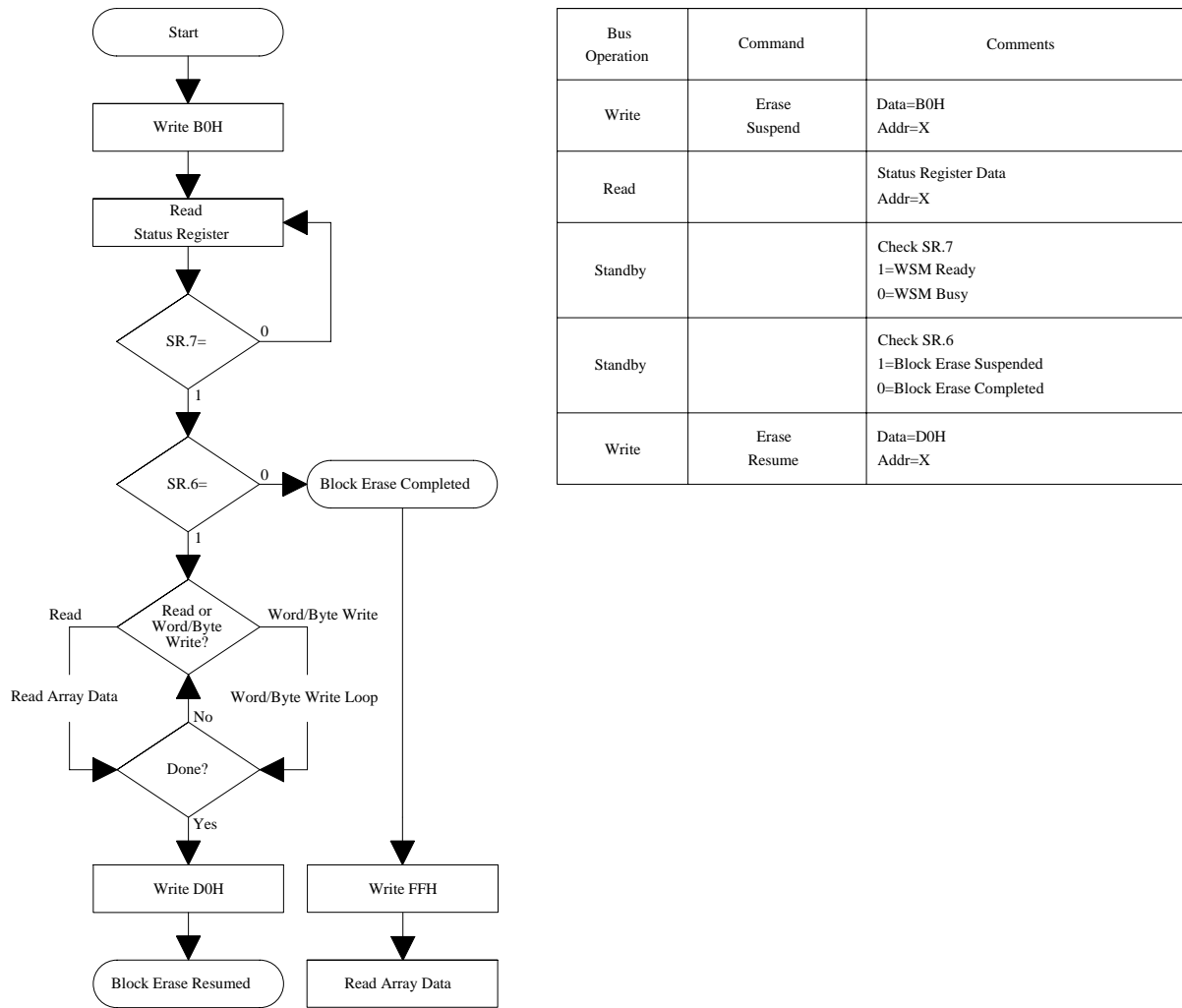
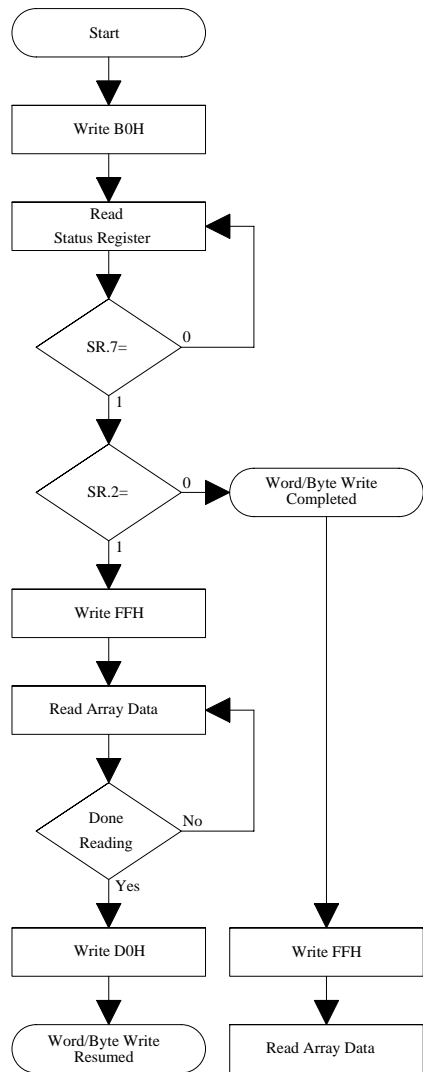


Figure 7. Block Erase Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Word/Byte Write Suspend	Data=B0H Addr=X
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.2 1=Word/Byte Write Suspended 0=Word/Byte Write Completed
Write	Read Array	Data=FFH Addr=X
Read		Read Array locations other than that being written.
Write	Word/Byte Write Resume	Data=D0H Addr=X

Figure 8. Word/Byte Write Suspend/Resume Flowchart

## 5 DESIGN CONSIDERATIONS

### 5.1 Three-Line Output Control

The device will often be used in large memory arrays. SHARP provides three control inputs to accommodate multiple memory connections. Three-line control provides for:

- a. Lowest possible memory power dissipation.
- b. Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable CE# while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. RP# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

### 5.2 RY/BY#, Block Erase and Word/Byte Write Polling

RY/BY# is a full CMOS output that provides a hardware method of detecting block erase and word/byte write completion. It transitions low after block erase or word/byte write commands and returns to  $V_{OH}$  when the WSM has finished executing the internal algorithm.

RY/BY# can be connected to an interrupt input of the system CPU or controller. It is active at all times. RY/BY# is also  $V_{OH}$  when the device is in block erase suspend

(with word/byte write inactive), word/byte write suspend or deep power-down modes.

### 5.3 Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of CE# and OE#. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 $\mu$ F ceramic capacitor connected between its  $V_{CC}$  and GND and between its  $V_{PP}$  and GND. These high-frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7 $\mu$ F electrolytic capacitor should be placed at the array's power supply connection between  $V_{CC}$  and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

### 5.4 $V_{PP}$ Trace on Printed Circuit Boards

Updating flash memories that reside in the target system requires that the printed circuit board designer pay attention to the  $V_{PP}$  Power supply trace. The  $V_{PP}$  pin supplies the memory cell current for word/byte writing and block erasing. Use similar trace widths and layout considerations given to the  $V_{CC}$  power bus. Adequate  $V_{PP}$  supply traces and decoupling will decrease  $V_{PP}$  voltage spikes and overshoots.

## 5.5 $V_{CC}$ , $V_{PP}$ , RP# Transitions

Block erase and word/byte write are not guaranteed if  $V_{PP}$  falls outside of a valid  $V_{PPH1/2/3}$  range,  $V_{CC}$  falls outside of a valid  $V_{CC1/2/3/4}$  range, or  $RP\# \neq V_{IH}$  or  $V_{HH}$ . If  $V_{PP}$  error is detected, status register bit SR.3 is set to "1" along with SR.4 or SR.5, depending on the attempted operation. If RP# transitions to  $V_{IL}$  during block erase or word/byte write, RY/BY# will remain low until the reset operation is complete. Then, the operation will abort and the device will enter deep power-down. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored. Device power-off or RP# transitions to  $V_{IL}$  clear the status register.

The CUI latches commands issued by system software and is not altered by  $V_{PP}$  or CE# transitions or WSM actions. Its state is read array mode upon power-up, after exit from deep power-down or after  $V_{CC}$  transitions below  $V_{LKO}$ .

After block erase or word/byte write, even after  $V_{PP}$  transitions down to  $V_{PPLK}$ , the CUI must be placed in read array mode via the Read Array command if subsequent access to the memory array is desired.

## 5.6 Power-Up/Down Protection

The device is designed to offer protection against accidental block erasure or word/byte writing during power transitions. Upon power-up, the device is indifferent as to which power supply ( $V_{PP}$  or  $V_{CC}$ ) powers-up first. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against spurious writes for  $V_{CC}$  voltages above  $V_{LKO}$  when  $V_{PP}$  is active. Since both WE# and CE# must be low for a command write, driving either to  $V_{IH}$  will inhibit writes. The CUI's two-step command sequence architecture provides added level of protection against data alteration.

WP# provide additional protection from inadvertent code or data alteration. The device is disabled while  $RP\# = V_{IL}$  regardless of its control inputs state.

## 5.7 Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's nonvolatility increases usable battery life because data is retained when system power is removed.

In addition, deep power-down mode ensures extremely low power consumption even when system power is applied. For example, portable computing products and other power sensitive applications that use an array of devices for solid-state storage can consume negligible power by lowering RP# to  $V_{IL}$  standby or sleep modes. If access is again needed, the devices can be read following the  $t_{PHQV}$  and  $t_{PHWL}$  wake-up cycles required after RP# is first raised to  $V_{IH}$ . See AC Characteristics— Read Only and Write Operations and Figures 13, 14, 15 and 16 for more information.

## 6 ELECTRICAL SPECIFICATIONS

### 6.1 Absolute Maximum Ratings\*

#### Operating Temperature

During Read, Block Erase and  
Word/Byte Write.....-40°C to +85°C<sup>(1)</sup>  
Temperature under Bias ..... -40°C to +85°C

Storage Temperature ..... -65°C to +125°C

#### Voltage On Any Pin

(except V<sub>CC</sub>, V<sub>PP</sub>, and RP#) ..... -0.5V to +7.0V<sup>(2)</sup>

V<sub>CC</sub> Supply Voltage..... -0.2V to +7.0V<sup>(2)</sup>

#### V<sub>PP</sub> Update Voltage during Block

Erase and Word/Byte Write ..... -0.2V to +14.0V<sup>(2,3)</sup>

RP# Voltage ..... -0.5V to +14.0V<sup>(2,3)</sup>

Output Short Circuit Current..... 100mA<sup>(4)</sup>

*\*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

#### NOTES:

1. Operating temperature is for extended temperature product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V<sub>CC</sub> and V<sub>PP</sub> pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins and V<sub>CC</sub> is V<sub>CC</sub>+0.5V which, during transitions, may overshoot to V<sub>CC</sub>+2.0V for periods <20ns.
3. Maximum DC voltage on V<sub>PP</sub> and RP# may overshoot to +14.0V for periods <20ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

### 6.2 Operating Conditions

Temperature and V<sub>CC</sub> Operating Conditions

Symbol	Parameter	Min.	Max.	Unit	Test Condition
T <sub>A</sub>	Operating Temperature	-40	+85	°C	Ambient Temperature
V <sub>CC1</sub>	V <sub>CC</sub> Supply Voltage (2.7V-3.6V)	2.7	3.6	V	
V <sub>CC2</sub>	V <sub>CC</sub> Supply Voltage (3.3V±0.3V)	3.0	3.6	V	
V <sub>CC3</sub>	V <sub>CC</sub> Supply Voltage (5V±0.25V)	4.75	5.25	V	
V <sub>CC4</sub>	V <sub>CC</sub> Supply Voltage (5V±0.5V)	4.50	5.50	V	

#### 6.2.1 CAPACITANCE<sup>(1)</sup>

T<sub>A</sub>=+25°C, f=1MHz

Symbol	Parameter	Typ.	Max.	Unit	Condition
C <sub>IN</sub>	Input Capacitance	7	10	pF	V <sub>IN</sub> =0.0V
C <sub>OUT</sub>	Output Capacitance	9	12	pF	V <sub>OUT</sub> =0.0V

#### NOTE:

1. Sampled, not 100% tested.



### 6.2.2 AC INPUT/OUTPUT TEST CONDITIONS

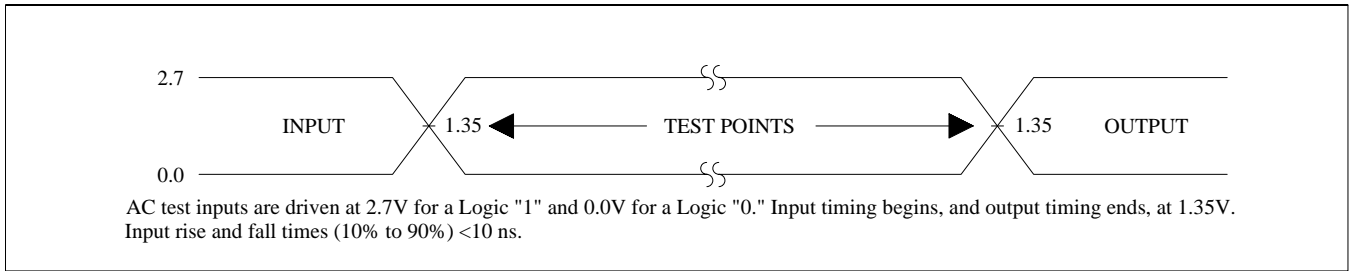


Figure 9. Transient Input/Output Reference Waveform for  $V_{CC}=2.7V-3.6V$

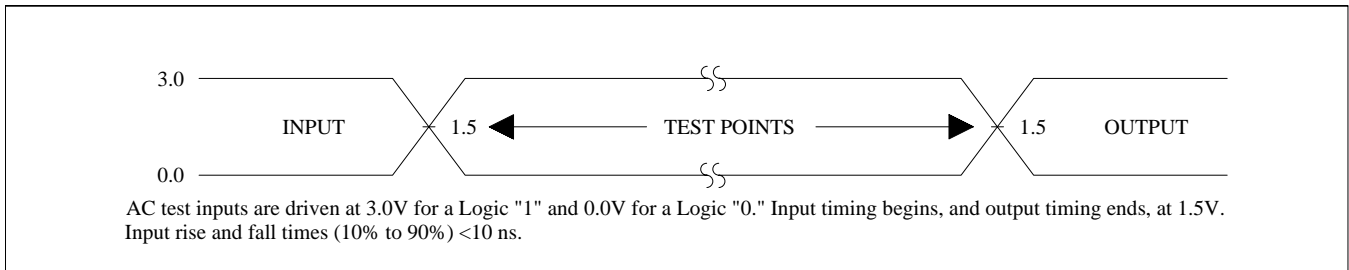


Figure 10. Transient Input/Output Reference Waveform for  $V_{CC}=3.3V\pm0.3V$  and  $V_{CC}=5V\pm0.25V$  (High Speed Testing Configuration)

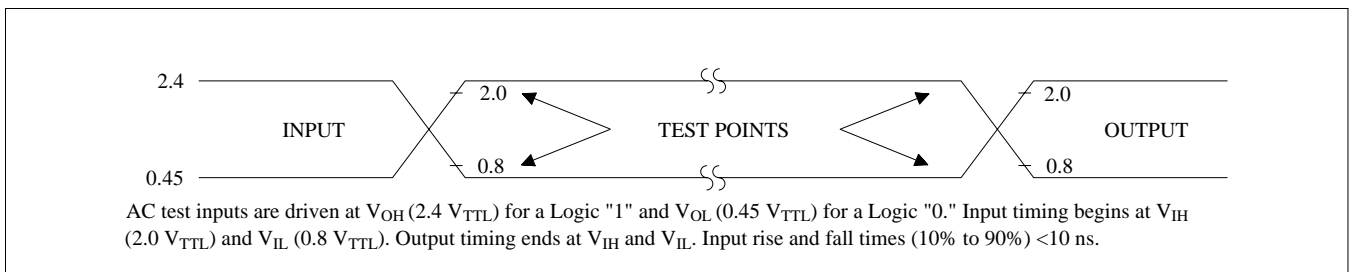


Figure 11. Transient Input/Output Reference Waveform for  $V_{CC}=5V\pm0.5V$  (Standard Testing Configuration)

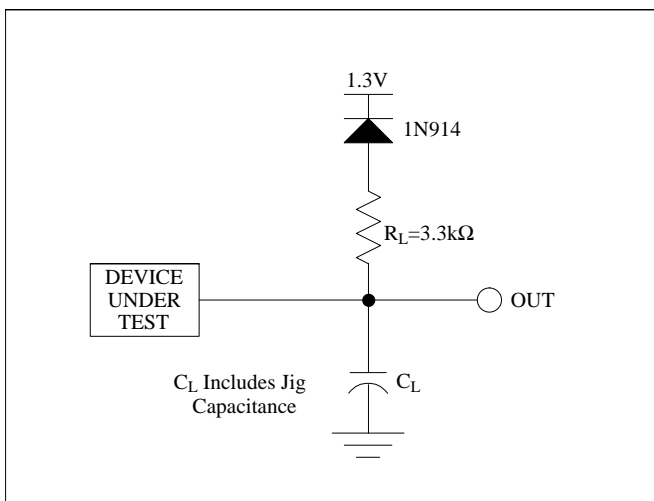


Figure 12. Transient Equivalent Testing Load Circuit

Test Configuration Capacitance Loading Value

Test Configuration	$C_L$ (pF)
$V_{CC}=3.3V\pm0.3V, 2.7V-3.6V$	30
$V_{CC}=5V\pm0.25V$	30
$V_{CC}=5V\pm0.5V$	100

## 6.2.3 DC CHARACTERISTICS

DC Characteristics

Sym.	Parameter	Notes	V <sub>CC</sub> =2.7V-3.6V		V <sub>CC</sub> =5V±0.5V		Unit	Test Conditions
			Typ.	Max.	Typ.	Max.		
I <sub>LI</sub>	Input Load Current	1		±0.5		±1	μA	V <sub>CC</sub> =V <sub>CC</sub> Max. V <sub>IN</sub> =V <sub>CC</sub> or GND
I <sub>LO</sub>	Output Leakage Current	1		±0.5		±10	μA	V <sub>CC</sub> =V <sub>CC</sub> Max. V <sub>OUT</sub> =V <sub>CC</sub> or GND
I <sub>CCS</sub>	V <sub>CC</sub> Standby Current	1,3,6, 10	25	50	30	100	μA	CMOS Inputs V <sub>CC</sub> =V <sub>CC</sub> Max. CE#=RP#=V <sub>CC</sub> ±0.2V
		1,3,6	0.2	2	0.4	2	mA	TTL Inputs V <sub>CC</sub> =V <sub>CC</sub> Max. CE#=RP#=V <sub>IH</sub>
I <sub>CCD</sub>	V <sub>CC</sub> Deep Power-Down Current	1,10	4	20		20	μA	RP#=GND±0.2V I <sub>OUT</sub> (RY/BY#)=0mA
I <sub>CCR</sub>	V <sub>CC</sub> Read Current	1,5,6	15	25		50	mA	CMOS Inputs V <sub>CC</sub> =V <sub>CC</sub> Max., CE#=GND f=5MHz(3.3V±0.3V), f=5MHz(2.7V-3.6V) f=8MHz(5V±0.5V) I <sub>OUT</sub> =0mA
I <sub>CCW</sub>	V <sub>CC</sub> Word/Byte Write Current	1,7	5	17	—	—	mA	V <sub>PP</sub> =2.7V-3.6V
			5	17		35	mA	V <sub>PP</sub> =4.5V-5.5V
			5	12		30	mA	V <sub>PP</sub> =11.4V-12.6V
I <sub>CCE</sub>	V <sub>CC</sub> Block Erase Current	1,7	4	17	—	—	mA	V <sub>PP</sub> =2.7V-3.6V
			4	17		30	mA	V <sub>PP</sub> =4.5V-5.5V
			4	12		25	mA	V <sub>PP</sub> =11.4V-12.6V
I <sub>CCWS</sub> I <sub>CCES</sub>	V <sub>CC</sub> Word/Byte Write or Block Erase Suspend Current	1,2	1	6	1	10	mA	CE#=V <sub>IH</sub>
I <sub>PPS</sub> I <sub>PPR</sub>	V <sub>PP</sub> Standby or Read Current	1	±2	±15	±2	±15	μA	V <sub>PP</sub> ≤V <sub>CC</sub>
			10	200	10	200	μA	V <sub>PP</sub> >V <sub>CC</sub>
I <sub>PPD</sub>	V <sub>PP</sub> Deep Power-Down Current	1	0.1	5	0.1	5	μA	RP#=GND±0.2V
I <sub>PPW</sub>	V <sub>PP</sub> Word/Byte Write Current	1,7	12	40	—	—	mA	V <sub>PP</sub> =2.7V-3.6V
				40		40	mA	V <sub>PP</sub> =4.5V-5.5V
				30		30	mA	V <sub>PP</sub> =11.4V-12.6V
I <sub>PPE</sub>	V <sub>PP</sub> Block Erase Current	1,7	8	25	—	—	mA	V <sub>PP</sub> =2.7V-3.6V
				25		25	mA	V <sub>PP</sub> =4.5V-5.5V
				20		20	mA	V <sub>PP</sub> =11.4V-12.6V
I <sub>PPWS</sub> I <sub>PPES</sub>	V <sub>PP</sub> Word/Byte Write or Block Erase Suspend Current	1	10	200	10	200	μA	V <sub>PP</sub> =V <sub>PPH1/2/3</sub>

## DC Characteristics (Continued)

Sym.	Parameter	Notes	V <sub>CC</sub> =2.7V-3.6V		V <sub>CC</sub> =5V±0.5V		Unit	Test Conditions
			Min.	Max.	Min.	Max.		
V <sub>IL</sub>	Input Low Voltage	7	-0.5	0.8	-0.5	0.8	V	
V <sub>IH</sub>	Input High Voltage	7	2.0	V <sub>CC</sub> +0.5	2.0	V <sub>CC</sub> +0.5	V	
V <sub>OL</sub>	Output Low Voltage	3,7		0.4		0.45	V	V <sub>CC</sub> =V <sub>CC</sub> Min. I <sub>OL</sub> =5.8mA(5V±0.5V) I <sub>OL</sub> =2.0mA(3.3V±0.3V) I <sub>OL</sub> =2.0mA(2.7V-3.6V)
V <sub>OH1</sub>	Output High Voltage (TTL)	3,7	2.4		2.4		V	V <sub>CC</sub> =V <sub>CC</sub> Min. I <sub>OH</sub> =-2.5mA(5V±0.5V) I <sub>OH</sub> =-2.0mA(3.3V±0.3V) I <sub>OH</sub> =-1.5mA(2.7V-3.6V)
V <sub>OH2</sub>	Output High Voltage (CMOS)	3,7	0.85		0.85		V	V <sub>CC</sub> =V <sub>CC</sub> Min. I <sub>OH</sub> =-2.0mA
			V <sub>CC</sub> -0.4		V <sub>CC</sub> -0.4		V	V <sub>CC</sub> =V <sub>CC</sub> Min. I <sub>OH</sub> =-100µA
V <sub>PPLK</sub>	V <sub>PP</sub> Lockout Voltage during Normal Operations	4,7		1.5		1.5	V	
V <sub>PPH1</sub>	V <sub>PP</sub> Voltage during Word/Byte Write or Block Erase Operations		2.7	3.6	—	—	V	
V <sub>PPH2</sub>	V <sub>PP</sub> Voltage during Word/Byte Write or Block Erase Operations		4.5	5.5	4.5	5.5	V	
V <sub>PPH3</sub>	V <sub>PP</sub> Voltage during Word/Byte Write or Block Erase Operations		11.4	12.6	11.4	12.6	V	
V <sub>LKO</sub>	V <sub>CC</sub> Lockout Voltage		2.0		2.0		V	
V <sub>HH</sub>	RP# Unlock Voltage	8,9	11.4	12.6	11.4	12.6	V	Unavailable WP#

## NOTES:

- All currents are in RMS unless otherwise noted. Typical values at nominal V<sub>CC</sub> voltage and T<sub>A</sub>=+25°C.
- I<sub>CCWS</sub> and I<sub>CCES</sub> are specified with the device de-selected. If read or word/byte written while in erase suspend mode, the device's current draw is the sum of I<sub>CCWS</sub> or I<sub>CCES</sub> and I<sub>CCR</sub> or I<sub>CCW</sub>, respectively.
- Includes RY/BY#.
- Block erases and word/byte writes are inhibited when V<sub>PP</sub> ≤ V<sub>PPLK</sub>, and not guaranteed in the range between V<sub>PPLK</sub>(max.) and V<sub>PPH1</sub>(min.), between V<sub>PPH1</sub>(max.) and V<sub>PPH2</sub>(min.), between V<sub>PPH2</sub>(max.) and V<sub>PPH3</sub>(min.), and above V<sub>PPH3</sub>(max.).
- Automatic Power Savings (APS) reduces typical I<sub>CCR</sub> to 1mA at 5V V<sub>CC</sub> and 3mA at 2.7V and 3.3V V<sub>CC</sub> in static operation.
- CMOS inputs are either V<sub>CC</sub>±0.2V or GND±0.2V. TTL inputs are either V<sub>IL</sub> or V<sub>IH</sub>.
- Sampled, not 100% tested.
- Boot block erases and word/byte writes are inhibited when the corresponding RP#=V<sub>IH</sub> and WP#=V<sub>IL</sub>. Block erase and word/byte write operations are not guaranteed with V<sub>IH</sub><RP#<V<sub>HH</sub> and should not be attempted.
- RP# connection to a V<sub>HH</sub> supply is allowed for a maximum cumulative period of 80 hours.
- BYTE# input level is V<sub>CC</sub>±0.2V in word mode or GND±0.2V in byte mode. WP# input level is V<sub>CC</sub>±0.2V or GND±0.2V.

6.2.4 AC CHARACTERISTICS - READ-ONLY OPERATIONS<sup>(1)</sup>

$$V_{CC}=2.7V-3.6V, T_A=-40^{\circ}C \text{ to } +85^{\circ}C$$

Sym.	Parameter	Notes	Min.	Max.	Unit
t <sub>AVAV</sub>	Read Cycle Time		120		ns
t <sub>AVQV</sub>	Address to Output Delay			120	ns
t <sub>ELQV</sub>	CE# to Output Delay	2		120	ns
t <sub>PHQV</sub>	RP# High to Output Delay			600	ns
t <sub>GLQV</sub>	OE# to Output Delay	2		50	ns
t <sub>ELQX</sub>	CE# to Output in Low Z	3	0		ns
t <sub>EHQZ</sub>	CE# High to Output in High Z	3		55	ns
t <sub>GLQX</sub>	OE# to Output in Low Z	3	0		ns
t <sub>GHQZ</sub>	OE# High to Output in High Z	3		20	ns
t <sub>OH</sub>	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		ns
t <sub>FVQV</sub>	BYTE# to Output Delay	3		120	ns
t <sub>FLQZ</sub>	BYTE# Low to Output in High Z	3		30	ns
t <sub>ELFV</sub>	CE# to BYTE# High or Low	3,6		5	ns

NOTE:

See 5.0V V<sub>CC</sub> Read-Only Operations for notes 1 through 6.

$$V_{CC}=3.3V\pm 0.3V, T_A=-40^{\circ}C \text{ to } +85^{\circ}C$$

Sym.	Parameter	Notes	Min.	Max.	Unit
t <sub>AVAV</sub>	Read Cycle Time		100		ns
t <sub>AVQV</sub>	Address to Output Delay			100	ns
t <sub>ELQV</sub>	CE# to Output Delay	2		100	ns
t <sub>PHQV</sub>	RP# High to Output Delay			600	ns
t <sub>GLQV</sub>	OE# to Output Delay	2		50	ns
t <sub>ELQX</sub>	CE# to Output in Low Z	3	0		ns
t <sub>EHQZ</sub>	CE# High to Output in High Z	3		55	ns
t <sub>GLQX</sub>	OE# to Output in Low Z	3	0		ns
t <sub>GHQZ</sub>	OE# High to Output in High Z	3		20	ns
t <sub>OH</sub>	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		ns
t <sub>FVQV</sub>	BYTE# to Output Delay	3		100	ns
t <sub>FLQZ</sub>	BYTE# Low to Output in High Z	3		30	ns
t <sub>ELFV</sub>	CE# to BYTE# High or Low	3,6		5	ns

NOTE:

See 5.0V V<sub>CC</sub> Read-Only Operations for notes 1 through 6.

$V_{CC}=5V\pm 0.5V, 5V\pm 0.25V, T_A=-40^{\circ}C \text{ to } +85^{\circ}C$ 

Sym.	Parameter	Notes	$V_{CC}=5V\pm 0.25V^{(4)}$		$V_{CC}=5V\pm 0.5V^{(5)}$		Unit
			Min.	Max.	Min.	Max.	
$t_{AVAV}$	Read Cycle Time		85		90		ns
$t_{AVQV}$	Address to Output Delay			85		90	ns
$t_{ELQV}$	CE# to Output Delay	2		85		90	ns
$t_{PHQV}$	RP# High to Output Delay			400		400	ns
$t_{GLQV}$	OE# to Output Delay	2		40		45	ns
$t_{ELQX}$	CE# to Output in Low Z	3	0		0		ns
$t_{EHQZ}$	CE# High to Output in High Z	3		55		55	ns
$t_{GLQX}$	OE# to Output in Low Z	3	0		0		ns
$t_{GHQZ}$	OE# High to Output in High Z	3		10		10	ns
$t_{OH}$	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		0		ns
$t_{FVQV}$	BYTE# to Output Delay	3		85		90	ns
$t_{FLQZ}$	BYTE# Low to Output in High Z	3		25		30	ns
$t_{ELFV}$	CE# to BYTE# High or Low	3,6		5		5	ns

## NOTES:

1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. OE# may be delayed up to  $t_{ELQV}-t_{GLQV}$  after the falling edge of CE# without impact on  $t_{ELQV}$ .
3. Sampled, not 100% tested.
4. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (High Speed Configuration) for testing characteristics.
5. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (Standard Configuration) for testing characteristics.
6. If BYTE# transfer during reading cycle, exist the regulations separately.

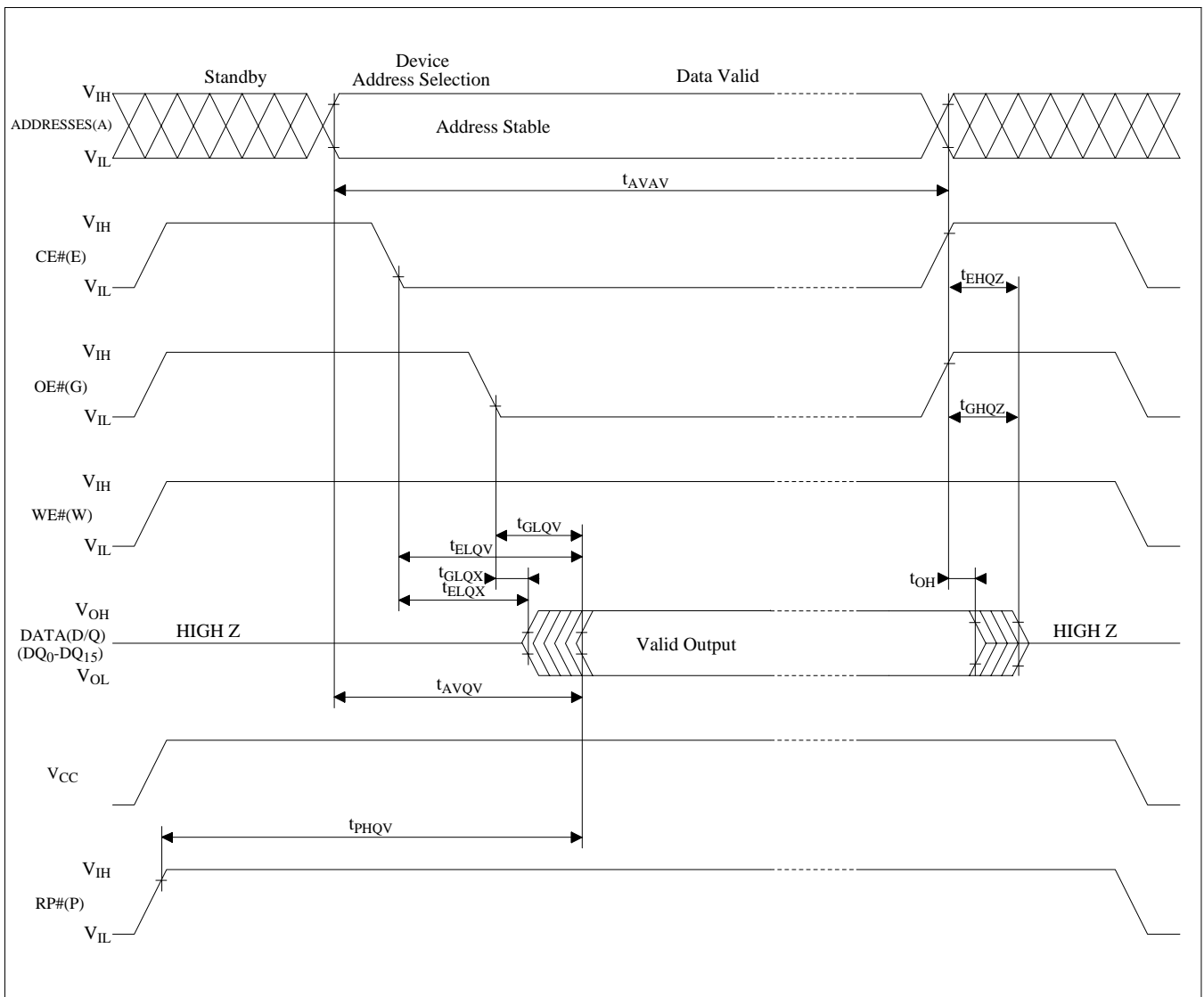


Figure 13. AC Waveform for Read Operations

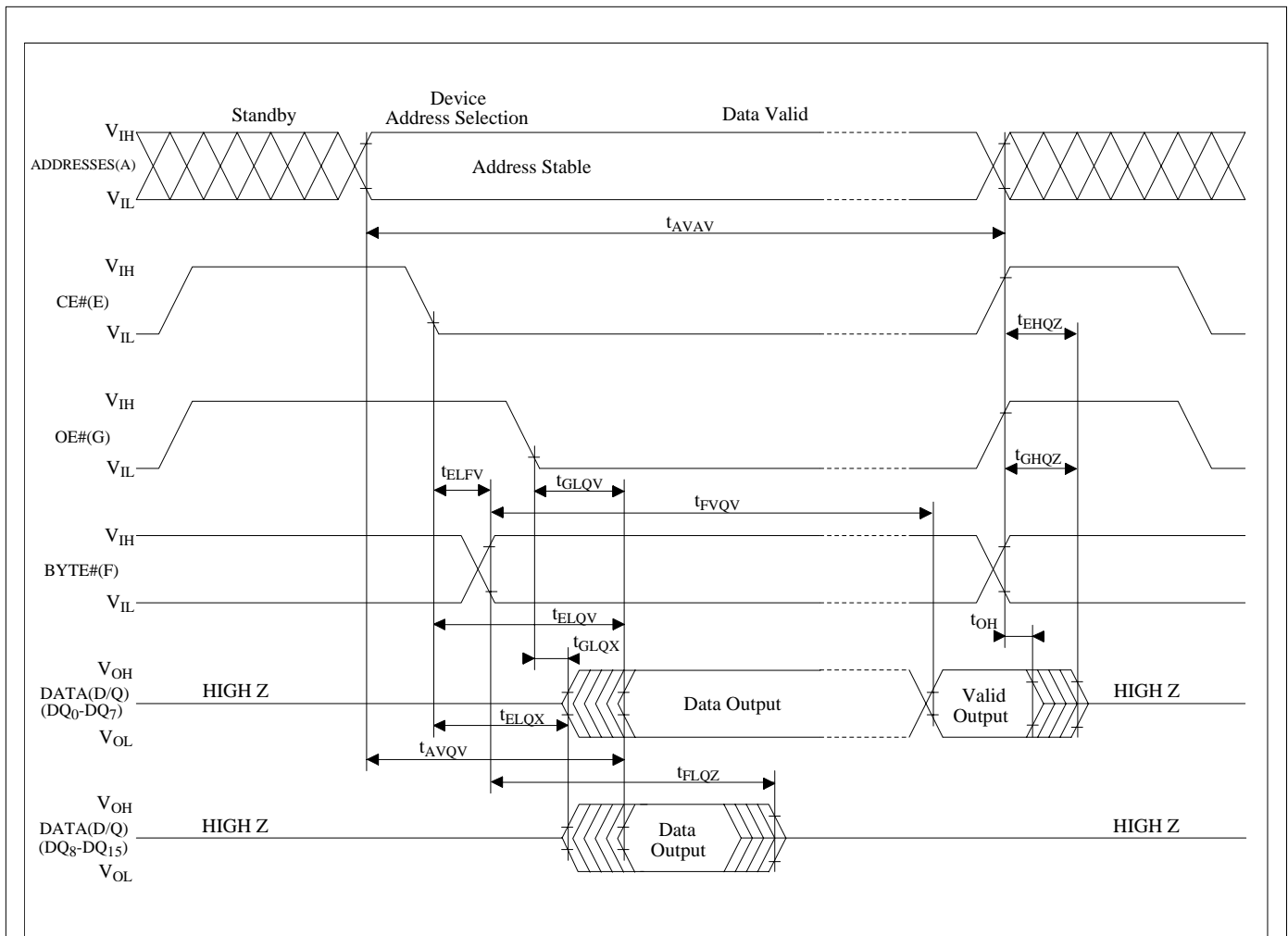


Figure 14. BYTE# timing Waveform

6.2.5 AC CHARACTERISTICS - WRITE OPERATIONS<sup>(1)</sup>
 $V_{CC}=2.7V-3.6V, T_A=-40^{\circ}C \text{ to } +85^{\circ}C$ 

Sym.	Parameter	Notes	Min.	Max.	Unit
$t_{AVAV}$	Write Cycle Time		120		ns
$t_{PHWL}$	RP# High Recovery to WE# Going Low	2	1		$\mu s$
$t_{ELWL}$	CE# Setup to WE# Going Low		10		ns
$t_{WLWH}$	WE# Pulse Width		50		ns
$t_{PHHWH}$	RP# $V_{HH}$ Setup to WE# Going High	2	100		ns
$t_{SHWH}$	WP# $V_{IH}$ Setup to WE# Going High	2	100		ns
$t_{VPWH}$	$V_{PP}$ Setup to WE# Going High	2	100		ns
$t_{AVWH}$	Address Setup to WE# Going High	3	50		ns
$t_{DVWH}$	Data Setup to WE# Going High	3	50		ns
$t_{WHDX}$	Data Hold from WE# High		0		ns
$t_{WHAX}$	Address Hold from WE# High		5		ns
$t_{WHEH}$	CE# Hold from WE# High		10		ns
$t_{WHWL}$	WE# Pulse Width High		30		ns
$t_{WHRL}$	WE# High to RY/BY# Going Low			100	ns
$t_{WHGL}$	Write Recovery before Read		0		ns
$t_{QVVL}$	$V_{PP}$ Hold from Valid SRD, RY/BY# High	2,4	0		ns
$t_{QVPH}$	RP# $V_{HH}$ Hold from Valid SRD, RY/BY# High	2,4	0		ns
$t_{QVSL}$	WP# $V_{IH}$ Hold from Valid SRD, RY/BY# High	2,4	0		ns
$t_{FVWH}$	BYTE# Setup to WE# Going High	7	50		ns
$t_{WHFV}$	BYTE# Hold from WE# High	7	120		ns

NOTE:

See 5.0V  $V_{CC}$  AC Characteristics - Write Operations for notes 1 through 7.



$V_{CC}=3.3V\pm 0.3V, T_A=-40^{\circ}C \text{ to } +85^{\circ}C$ 

Sym.	Parameter	Notes	Min.	Max.	Unit
$t_{AVAV}$	Write Cycle Time		100		ns
$t_{PHWL}$	RP# High Recovery to WE# Going Low	2	1		$\mu s$
$t_{ELWL}$	CE# Setup to WE# Going Low		10		ns
$t_{WLWH}$	WE# Pulse Width		50		ns
$t_{PHHWH}$	RP# $V_{HH}$ Setup to WE# Going High	2	100		ns
$t_{SHWH}$	WP# $V_{IH}$ Setup to WE# Going High	2	100		ns
$t_{VPWH}$	$V_{PP}$ Setup to WE# Going High	2	100		ns
$t_{AVWH}$	Address Setup to WE# Going High	3	50		ns
$t_{DVWH}$	Data Setup to WE# Going High	3	50		ns
$t_{WHDX}$	Data Hold from WE# High		0		ns
$t_{WHAX}$	Address Hold from WE# High		5		ns
$t_{WHEH}$	CE# Hold from WE# High		10		ns
$t_{WHWL}$	WE# Pulse Width High		30		ns
$t_{WHRL}$	WE# High to RY/BY# Going Low			100	ns
$t_{WHGL}$	Write Recovery before Read		0		ns
$t_{QVVL}$	$V_{PP}$ Hold from Valid SRD, RY/BY# High	2,4	0		ns
$t_{QVPH}$	RP# $V_{HH}$ Hold from Valid SRD, RY/BY# High	2,4	0		ns
$t_{QVSL}$	WP# $V_{IH}$ Hold from Valid SRD, RY/BY# High	2,4	0		ns
$t_{FVWH}$	BYTE# Setup to WE# Going High	7	50		ns
$t_{WHFV}$	BYTE# Hold from WE# High	7	100		ns

NOTE:

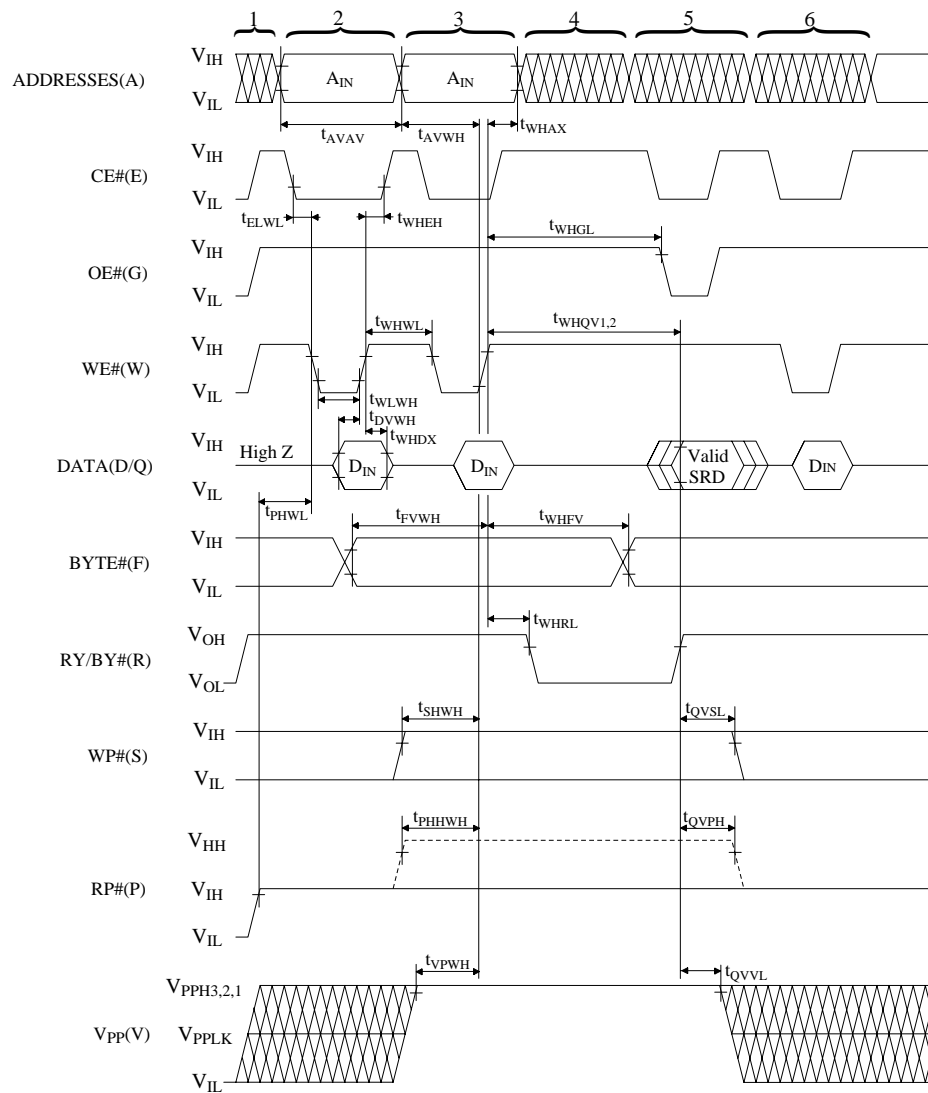
See 5.0V  $V_{CC}$  AC Characteristics - Write Operations for notes for notes 1 through 7.

$$V_{CC}=5V\pm 0.5V, 5V\pm 0.25V, T_A=-40^{\circ}C \text{ to } +85^{\circ}C$$

Sym.	Parameter	Notes	$V_{CC}=5V\pm 0.25V^{(5)}$		$V_{CC}=5V\pm 0.5V^{(6)}$		Unit
			Min.	Max.	Min.	Max.	
$t_{AVAV}$	Write Cycle Time		85		90		ns
$t_{PHWL}$	RP# High Recovery to WE# Going Low	2	1		1		$\mu$ s
$t_{ELWL}$	CE# Setup to WE# Going Low		10		10		ns
$t_{WLWH}$	WE# Pulse Width		40		40		ns
$t_{PHHWH}$	RP# $V_{HH}$ Setup to WE# Going High	2	100		100		ns
$t_{SHWH}$	WP# $V_{IH}$ Setup to WE# Going High	2	100		100		ns
$t_{VPWH}$	$V_{PP}$ Setup to WE# Going High	2	100		100		ns
$t_{AVWH}$	Address Setup to WE# Going High	3	40		40		ns
$t_{DVWH}$	Data Setup to WE# Going High	3	40		40		ns
$t_{WHDX}$	Data Hold from WE# High		0		0		ns
$t_{WHAX}$	Address Hold from WE# High		5		5		ns
$t_{WHEH}$	CE# Hold from WE# High		10		10		ns
$t_{WHWL}$	WE# Pulse Width High		30		30		ns
$t_{WHRL}$	WE# High to RY/BY# Going Low			90		90	ns
$t_{WHGL}$	Write Recovery before Read		0		0		ns
$t_{QVVL}$	$V_{PP}$ Hold from Valid SRD, RY/BY# High	2,4	0		0		ns
$t_{QVPH}$	RP# $V_{HH}$ Hold from Valid SRD, RY/BY# High	2,4	0		0		ns
$t_{QVSL}$	WP# $V_{IH}$ Hold from Valid SRD, RY/BY# High	2,4	0		0		ns
$t_{FVWH}$	BYTE# Setup to WE# Going High	7	40		40		ns
$t_{WHFV}$	BYTE# Hold from WE# High	7	85		90		ns

## NOTES:

1. Read timing characteristics during block erase and word/byte write operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid  $A_{IN}$  and  $D_{IN}$  for block erase or word/byte write.
4.  $V_{PP}$  should be held at  $V_{PPH1/2/3}$  (and if necessary RP# should be held at  $V_{HH}$ ) until determination of block erase or word/byte write success (SR.1/3/4/5=0).
5. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (High Seed Configuration) for testing characteristics.
6. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (Standard Configuration) for testing characteristics.
7. If BYTE# switch during reading cycle, exist the regulations separately.



## NOTES:

1.  $V_{CC}$  power-up and standby.
2. Write block erase or word/byte write setup.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Figure 15. AC Waveform for WE#-Controlled Write Operations

6.2.6 ALTERNATIVE CE#-CONTROLLED WRITES<sup>(1)</sup>
 $V_{CC}=2.7V-3.6V, T_A=-40^{\circ}C \text{ to } +85^{\circ}C$ 

Sym.	Parameter	Notes	Min.	Max.	Unit
t <sub>AVAV</sub>	Write Cycle Time		120		ns
t <sub>PHEL</sub>	RP# High Recovery to CE# Going Low	2	1		μs
t <sub>WLEL</sub>	WE# Setup to CE# Going Low		0		ns
t <sub>ELEH</sub>	CE# Pulse Width		70		ns
t <sub>PHHEH</sub>	RP#V <sub>HH</sub> Setup to CE# Going High	2	100		ns
t <sub>SHEH</sub>	WP#V <sub>IH</sub> Setup to CE# Going High	2	100		ns
t <sub>VPEH</sub>	V <sub>PP</sub> Setup to CE# Going High	2	100		ns
t <sub>AVEH</sub>	Address Setup to CE# Going High	3	50		ns
t <sub>DVEH</sub>	Data Setup to CE# Going High	3	50		ns
t <sub>EHDx</sub>	Data Hold from CE# High		0		ns
t <sub>EHAX</sub>	Address Hold from CE# High		5		ns
t <sub>EHWH</sub>	WE# Hold from CE# High		0		ns
t <sub>EHEL</sub>	CE# Pulse Width High		25		ns
t <sub>EHRL</sub>	CE# High to RY/BY# Going Low			100	ns
t <sub>EHGL</sub>	Write Recovery before Read		0		ns
t <sub>QVVL</sub>	V <sub>PP</sub> Hold from Valid SRD, RY/BY# High	2,4	0		ns
t <sub>QVPH</sub>	RP# V <sub>HH</sub> Hold from Valid SRD, RY/BY# High	2,4	0		ns
t <sub>QVSL</sub>	WP# V <sub>IH</sub> Hold from Valid SRD, RY/BY# High	2,4	0		ns
t <sub>FVEH</sub>	BYTE# Setup to CE# Going High	7	50		ns
t <sub>EHFV</sub>	BYTE# Hold from CE# High	7	120		ns

## NOTE:

See 5.0V V<sub>CC</sub> Alternative CE#-Controlled Writes for notes 1 through 7.

$V_{CC}=3.3V\pm 0.3V, T_A=-40^{\circ}C \text{ to } +85^{\circ}C$ 

Sym.	Parameter	Notes	Min.	Max.	Unit
$t_{AVAV}$	Write Cycle Time		100		ns
$t_{PHEL}$	RP# High Recovery to CE# Going Low	2	1		$\mu s$
$t_{WLEL}$	WE# Setup to CE# Going Low		0		ns
$t_{ELEH}$	CE# Pulse Width		70		ns
$t_{PHHEH}$	RP# $V_{HH}$ Setup to CE# Going High	2	100		ns
$t_{SHEH}$	WP# $V_{IH}$ Setup to CE# Going High	2	100		ns
$t_{VPEH}$	$V_{PP}$ Setup to CE# Going High	2	100		ns
$t_{AVEH}$	Address Setup to CE# Going High	3	50		ns
$t_{DVEH}$	Data Setup to CE# Going High	3	50		ns
$t_{EHDX}$	Data Hold from CE# High		0		ns
$t_{EHAX}$	Address Hold from CE# High		5		ns
$t_{EHWL}$	WE# Hold from CE# High		0		ns
$t_{EHEL}$	CE# Pulse Width High		25		ns
$t_{EHRL}$	CE# High to RY/BY# Going Low			100	ns
$t_{EHGL}$	Write Recovery before Read		0		ns
$t_{QVVL}$	$V_{PP}$ Hold from Valid SRD, RY/BY# High	2,4	0		ns
$t_{QVPH}$	RP# $V_{HH}$ Hold from Valid SRD, RY/BY# High	2,4	0		ns
$t_{QVSL}$	WP# $V_{IH}$ Hold from Valid SRD, RY/BY# High	2,4	0		ns
$t_{FVEH}$	BYTE# Setup to CE# Going High	7	50		ns
$t_{EHFV}$	BYTE# Hold from CE# High	7	100		ns

NOTE:

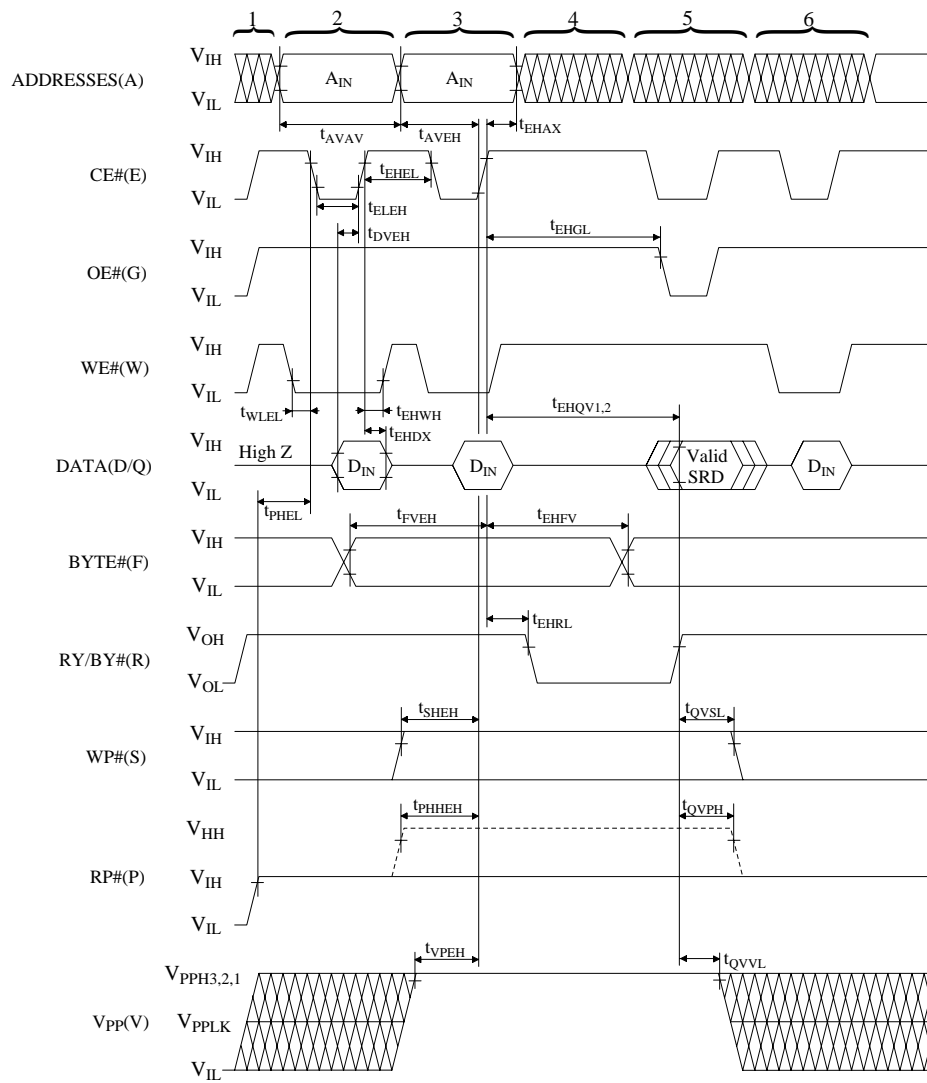
See 5V  $V_{CC}$  Alternative CE#-Controlled Writes for Notes 1 through 7.

$$V_{CC}=5V\pm 0.5V, 5V\pm 0.25V, T_A=-40^{\circ}C \text{ to } +85^{\circ}C$$

Sym.	Parameter	Notes	$V_{CC}=5V\pm 0.25V^{(5)}$		$V_{CC}=5V\pm 0.5V^{(6)}$		Unit
			Min.	Max.	Min.	Max.	
$t_{AVAV}$	Write Cycle Time		85		90		ns
$t_{PHEL}$	RP# High Recovery to CE# Going Low	2	1		1		$\mu s$
$t_{WLEL}$	WE# Setup to CE# Going Low		0		0		ns
$t_{ELEH}$	CE# Pulse Width		50		50		ns
$t_{PHHEH}$	RP# $V_{HH}$ Setup to CE# Going High	2	100		100		ns
$t_{SHEH}$	WP# $V_{IH}$ Setup to CE# Going High	2	100		100		ns
$t_{VPEH}$	$V_{PP}$ Setup to CE# Going High	2	100		100		ns
$t_{AVEH}$	Address Setup to CE# Going High	3	40		40		ns
$t_{DVEH}$	Data Setup to CE# Going High	3	40		40		ns
$t_{EHDX}$	Data Hold from CE# High		0		0		ns
$t_{EHAX}$	Address Hold from CE# High		5		5		ns
$t_{EHWL}$	WE# Hold from CE# High		0		0		ns
$t_{EHEL}$	CE# Pulse Width High		25		25		ns
$t_{EHRL}$	CE# High to RY/BY# Going Low			90		90	ns
$t_{EHGL}$	Write Recovery before Read		0		0		ns
$t_{QVVL}$	$V_{PP}$ Hold from Valid SRD, RY/BY# High	2,4	0		0		ns
$t_{QVPH}$	RP# $V_{HH}$ Hold from Valid SRD, RY/BY# High	2,4	0		0		ns
$t_{QVSL}$	WP# $V_{IH}$ Hold from Valid SRD, RY/BY# High	2,4	0		0		ns
$t_{FVEH}$	BYTE# Setup to CE# Going High	7	40		40		ns
$t_{EHFV}$	BYTE# Hold from CE# High	7	85		90		ns

## NOTES:

1. In systems where CE# defines the write pulse width (within a longer WE# timing waveform), all setup, hold, and inactive WE# times should be measured relative to the CE# waveform.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid  $A_{IN}$  and  $D_{IN}$  for block erase or word/byte write.
4.  $V_{PP}$  should be held at  $V_{PPH1/2/3}$  (and if necessary RP# should be held at  $V_{HH}$ ) until determination of block erase or word/byte write success (SR.1/3/4/5=0).
5. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (High Seed Configuration) for testing characteristics.
6. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (Standard Configuration) for testing characteristics.
7. If BYTE# switch during reading cycle, exist the regulations separately.



## NOTES:

1.  $V_{CC}$  power-up and standby.
2. Write block erase or word/byte write setup.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Figure 16. AC Waveform for CE#-Controlled Write Operations

## 6.2.7 RESET OPERATIONS

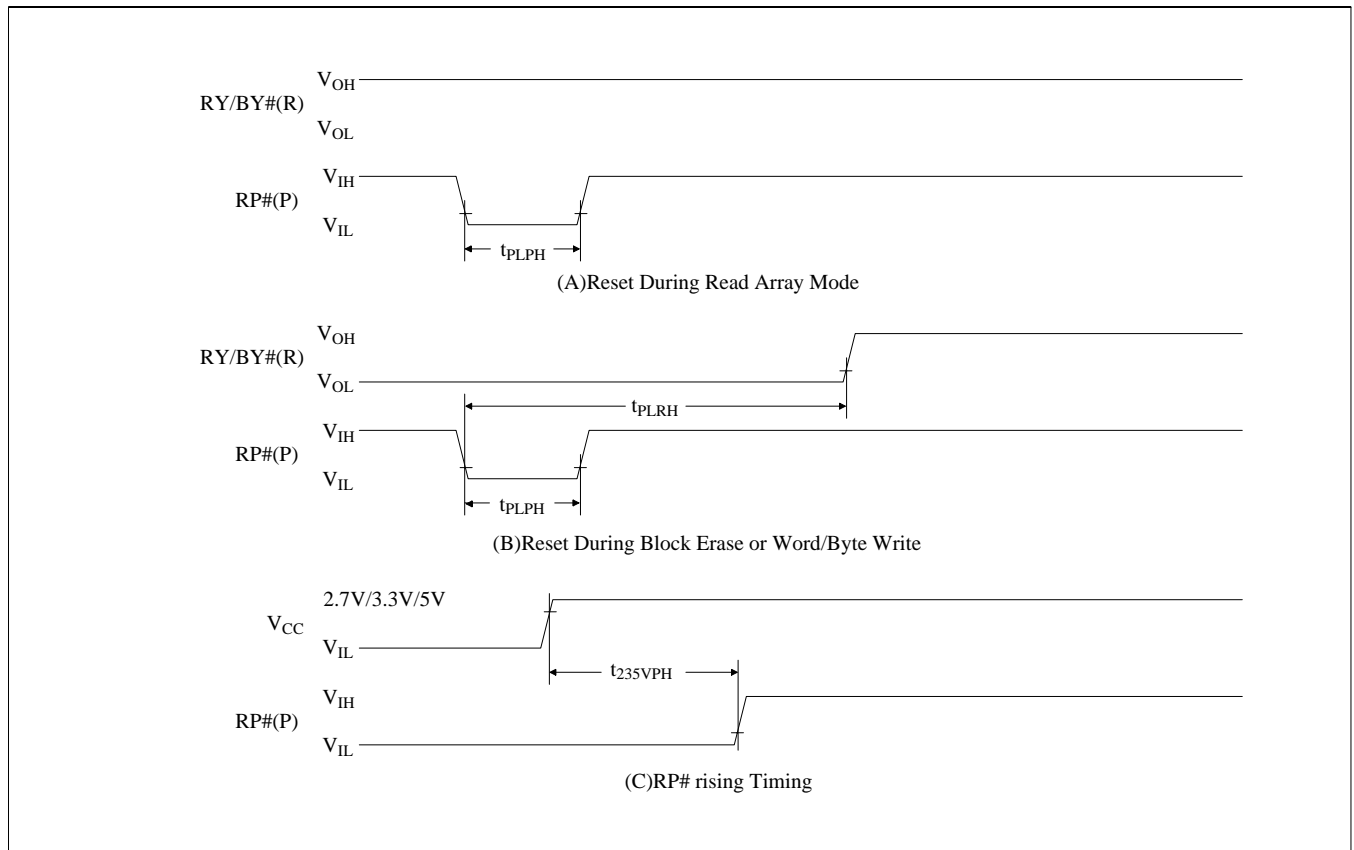


Figure 17. AC Waveform for Reset Operation

Reset AC Specifications

Sym.	Parameter	Notes	$V_{CC}=2.7V-3.6V$		$V_{CC}=3.0V-3.6V$		$V_{CC}=4.5V-5.5V$		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PLPH}$	RP# Pulse Low Time (If RP# is tied to $V_{CC}$ , this specification is not applicable)		100		100		100		ns
$t_{PLRH}$	RP# Low to Reset during Block Erase or Word/Byte Write	1,2		22		20		12	$\mu s$
$t_{235VPH}$	$V_{CC}$ 2.7V to RP# High $V_{CC}$ 3.0V to RP# High $V_{CC}$ 4.5V to RP# High	3	100		100		100		ns

## NOTES:

1. If RP# is asserted while a block erase or word/byte write operation is not executing, the reset will complete within 100ns.
2. A reset time,  $t_{P_{H_{QV}}}$ , is required from the later of RY/BY# or RP# going high until outputs are valid.
3. When the device power-up, holding RP# low minimum 100ns is required after  $V_{CC}$  has been in predefined range and also has been in stable there.



6.2.8 BLOCK ERASE AND WORD/BYTE WRITE PERFORMANCE<sup>(3)</sup> $V_{CC}=2.7V-3.6V, T_A=-40^{\circ}C$  to  $+85^{\circ}C$ 

Sym.	Parameter		Notes	$V_{pp}=2.7V-3.6V$		$V_{pp}=4.5V-5.5V$		$V_{pp}=11.4V-12.6V$		Unit
				Typ. <sup>(1)</sup>	Max.	Typ. <sup>(1)</sup>	Max.	Typ. <sup>(1)</sup>	Max.	
$t_{WHQV1}$ $t_{EHQV1}$	Word/Byte Write Time	32K word Block	2	44.6		17.7		12.6		$\mu s$
		4K word Block	2	45.9		26.1		24.5		$\mu s$
	Block Write Time	32K word Block	2,4	1.46		0.58		0.42		s
		4K word Block	2,4	0.19		0.11		0.11		s
$t_{WHQV2}$ $t_{EHQV2}$	Block Erase Time	32K word Block	2	1.14		0.61		0.51		s
		4K word Block	2	0.38		0.32		0.31		s
$t_{WHRH1}$ $t_{EHRH1}$	Word/Byte Write Suspend Latency Time to Read			7	8	6	8	6	7	$\mu s$
$t_{WHRH2}$ $t_{EHRH2}$	Erase Suspend Latency Time to Read			18	22	11	14	11	14	$\mu s$

NOTE:

See 5V  $V_{CC}$  Block Erase and Word/Byte Write Performance for Notes 1 through 4. $V_{CC}=3.3V\pm 0.3V, T_A=-40^{\circ}C$  to  $+85^{\circ}C$ 

Sym.	Parameter		Notes	$V_{pp}=3.0V-3.6V$		$V_{pp}=4.5V-5.5V$		$V_{pp}=11.4V-12.6V$		Unit
				Typ. <sup>(1)</sup>	Max.	Typ. <sup>(1)</sup>	Max.	Typ. <sup>(1)</sup>	Max.	
$t_{WHQV1}$ $t_{EHQV1}$	Word/Byte Write Time	32K word Block	2	44		17.3		12.3		$\mu s$
		4K word Block	2	45		25.6		24		$\mu s$
	Block Write Time	32K word Block	2,4	1.44		0.57		0.41		s
		4K word Block	2,4	0.19		0.11		0.1		s
$t_{WHQV2}$ $t_{EHQV2}$	Block Erase Time	32K word Block	2	1.11		0.59		0.5		s
		4K word Block	2	0.37		0.31		0.3		s
$t_{WHRH1}$ $t_{EHRH1}$	Word/Byte Write Suspend Latency Time to Read			6	7	5	7	5	6	$\mu s$
$t_{WHRH2}$ $t_{EHRH2}$	Erase Suspend Latency Time to Read			16.2	20	9.6	12	9.6	12	$\mu s$

NOTE:

See 5V  $V_{CC}$  Block Erase and Word/Byte Write Performance for Notes 1 through 4.

$V_{CC}=5V\pm 0.5V, 5V\pm 0.25V, T_A=-40^{\circ}C \text{ to } +85^{\circ}C$ 

Sym.	Parameter		Notes	$V_{PP}=4.5V-5.5V$		$V_{PP}=11.4V-12.6V$		Unit
				Typ. <sup>(1)</sup>	Max.	Typ. <sup>(1)</sup>	Max.	
$t_{WHQV1}$	Word/Byte Write Time	32K word Block	2	12.2		8.4		$\mu s$
$t_{EHQV1}$		4K word Block	2	18.3		17		$\mu s$
	Block Write Time	32K word Block	2,4	0.4		0.28		s
		4K word Block	2,4	0.08		0.07		s
$t_{WHQV2}$	Block Erase Time	32K word Block	2	0.46		0.39		s
$t_{EHQV2}$		4K word Block	2	0.26		0.25		s
$t_{WHRH1}$ $t_{EHRH1}$	Word/Byte Write Suspend Latency Time to Read			5	6	4	5	$\mu s$
$t_{WHRH2}$ $t_{EHRH2}$	Erase Suspend Latency Time to Read			9.6	12	9.6	12	$\mu s$

## NOTES:

1. Typical values measured at  $T_A=+25^{\circ}C$  and nominal voltages. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. Sampled but not 100% tested.
4. All values are in word mode (BYTE#=V<sub>IH</sub>). At byte mode (BYTE#=V<sub>IL</sub>), those values are double.

## Flash memory LHFXXVXX family Data Protection

Noises having a level exceeding the limit specified in this document may be generated under specific operating conditions on some systems.

Such noises, when induced onto WE# signal or power supply, may be interpreted as false commands, causing undesired memory updating.

To protect the data stored in the flash memory against unwanted overwriting, systems operating with the flash memory should have the following write protect designs, as appropriate:

### 1) Protecting data in specific block

By setting a WP# to low, only the boot block can be protected against overwriting.

Parameter and main blocks cannot be locked.

System program, etc. , can be locked by storing them in the boot block.

When a high voltage is applied to RP#, overwrite operation is enabled for all blocks.

For further information on controlling of WP# and RP#, refer to the chapter 4.10.

### 2) Data protection through V<sub>PP</sub>

When the level of V<sub>PP</sub> is lower than V<sub>PP<sub>PLK</sub></sub> (lockout voltage), write operation on the flash memory is disabled. All blocks are locked and the data in the blocks are completely write protected.

For the lockout voltage, refer to the chapter 4.10 and 6.2.3.

### 3) Data protection through RP#

When the RP# is kept low during power up and power down sequence such as voltage transition, write operation on the flash memory is disabled, write protecting all blocks.

For the details of RP# control, refer to the chapter 5.6 and 6.2.7.

### 4) Noise rejection of WE#

Consider noise rejection of WE# in order to prevent false write command input.

## A-1 RECOMMENDED OPERATING CONDITIONS

### A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

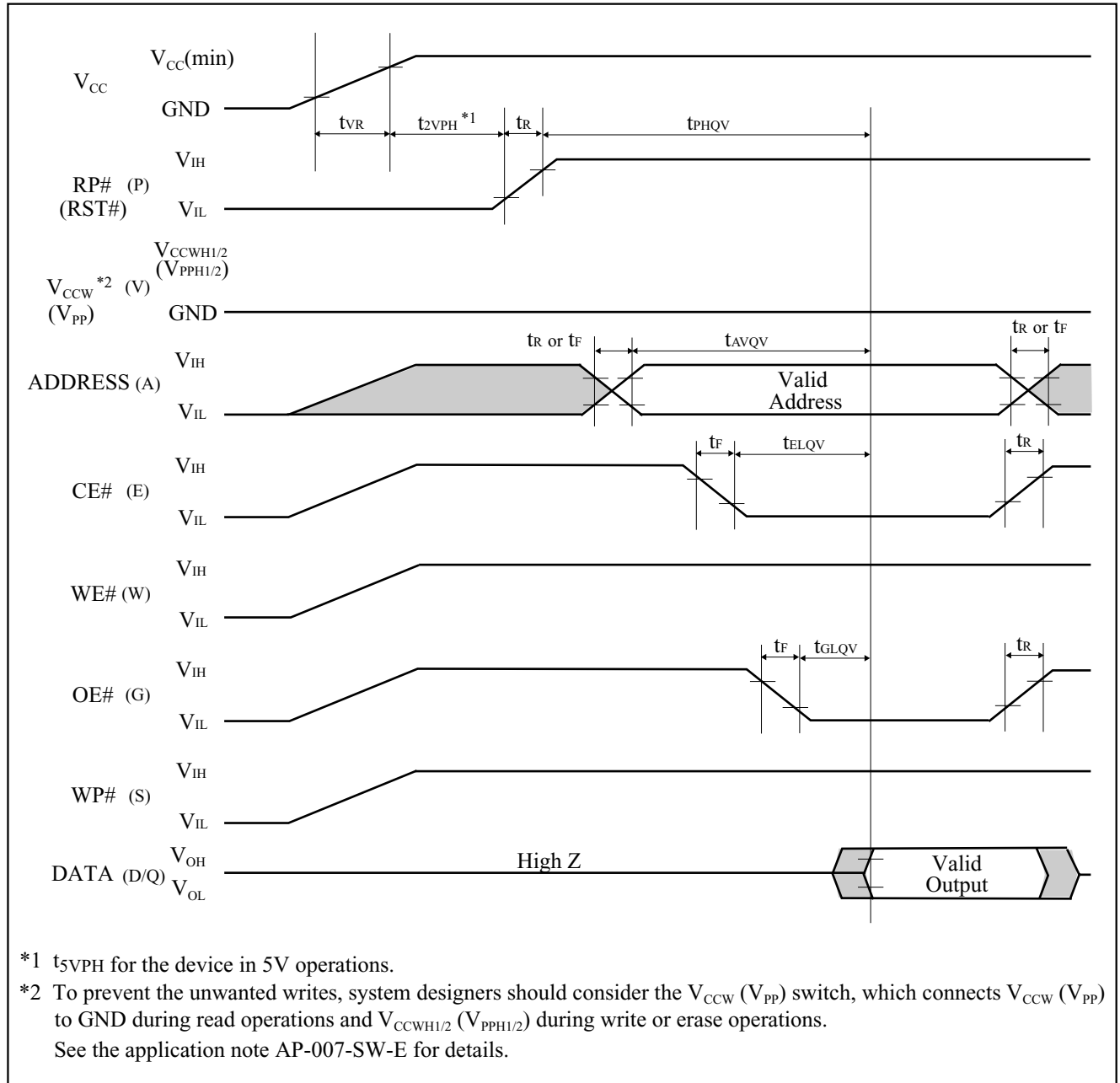


Figure A-1. AC Timing at Device Power-Up

For the AC specifications  $t_{VR}$ ,  $t_R$ ,  $t_F$  in the figure, refer to the next page. See the “ELECTRICAL SPECIFICATIONS” described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

## A-1.1.1 Rise and Fall Time

Symbol	Parameter	Notes	Min.	Max.	Unit
$t_{VR}$	$V_{CC}$ Rise Time	1	0.5	30000	$\mu\text{s}/\text{V}$
$t_R$	Input Signal Rise Time	1, 2		1	$\mu\text{s}/\text{V}$
$t_F$	Input Signal Fall Time	1, 2		1	$\mu\text{s}/\text{V}$

## NOTES:

1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.  
 $t_R(\text{Max.})$  and  $t_F(\text{Max.})$  for RP# (RST#) are  $100\mu\text{s}/\text{V}$ .

## A-1.2 Glitch Noises

Do not input the glitch noises which are below  $V_{IH}$  (Min.) or above  $V_{IL}$  (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

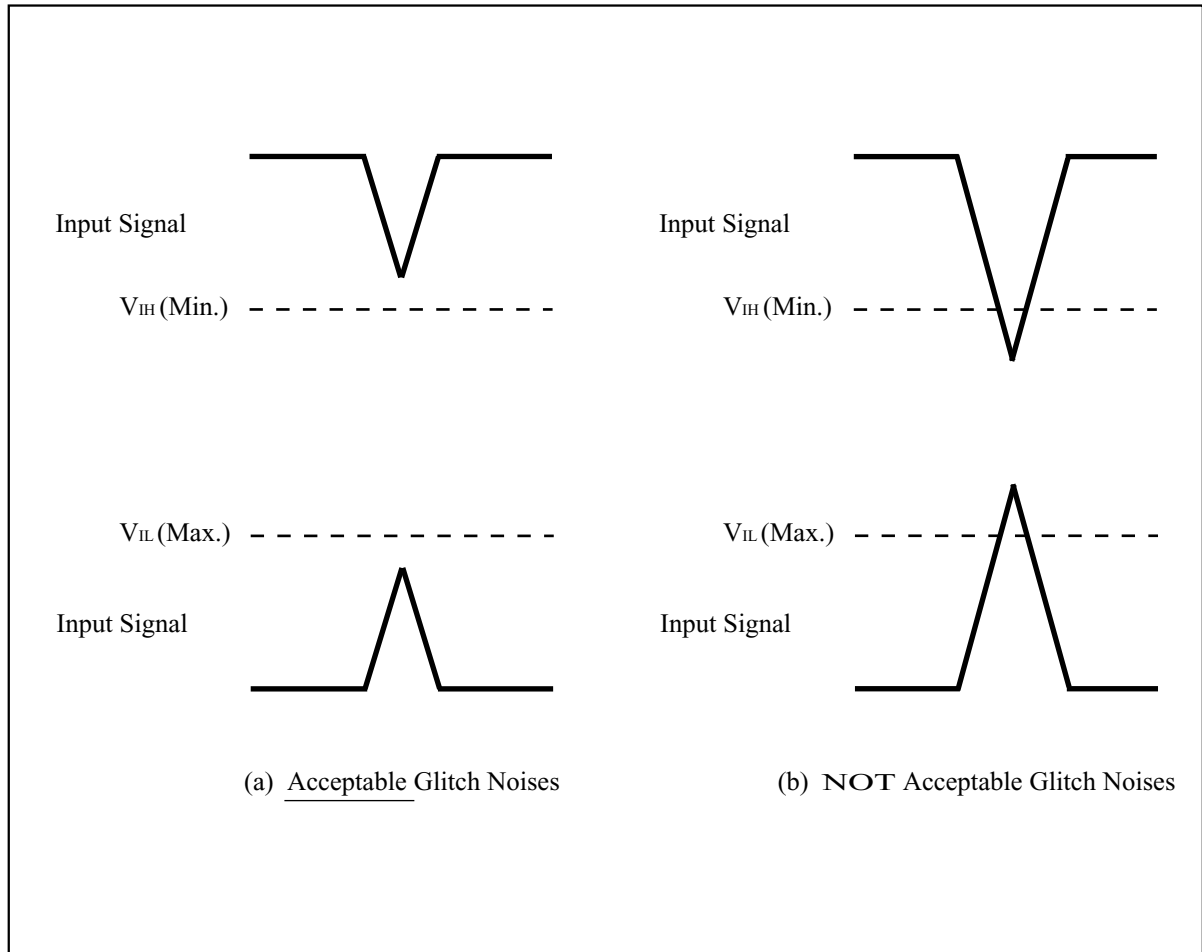


Figure A-2. Waveform for Glitch Noises

See the "DC CHARACTERISTICS" described in specifications for  $V_{IH}$  (Min.) and  $V_{IL}$  (Max.).

A-2 RELATED DOCUMENT INFORMATION<sup>(1)</sup>

Document No.	Document Name
AP-001-SD-E	Flash Memory Family Software Drivers
AP-006-PT-E	Data Protection Method of SHARP Flash Memory
AP-007-SW-E	RP#, $V_{PP}$ Electric Potential Switching Circuit

## NOTE:

1. International customers should contact their local SHARP or distribution sales office.