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April 1st, 2010
Renesas Electronics Corporation

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MOS INTEGRATED CIRCUIT

μPD16431A

1/2, 1/3, 1/4-DUTY LCD CONTROLLER/DRIVER

DESCRIPTION

The μPD16431A is an LCD controller/driver that enables display of segment type LCDs of 1/2, 1/3, or 1/4 duty cycle. This controller/driver has 56 segment output lines of which eight can also be used as LED output lines. Because the LCD driver contained in the μPD16431A has separate logic and power supply, up to 6.5 V of LCD driver voltage can be set. In addition, key source output lines for key scanning and key input data lines are also provided, so that the μPD16431A is ideal for applications in the front panel of an automobile stereo system.

FEATURES

- Various display modes
  - 1/2 duty: 112 segment outputs or 96 segment outputs + 8 LED outputs
  - 1/3 duty: 168 segment outputs or 144 segment outputs + 8 LED outputs
  - 1/4 duty: 224 segment outputs or 192 segment outputs + 8 LED outputs
- Key scan circuit (key source outputs are shared with LCD driver outputs)
- Independent LCD driver power supply V_{LCD} (can be set to V_{DD} to 6.5 V)
- Serial data input/output (SCK, STB, DATA)
- On-chip oscillator incorporated
- Power-ON reset circuit

ORDERING INFORMATION

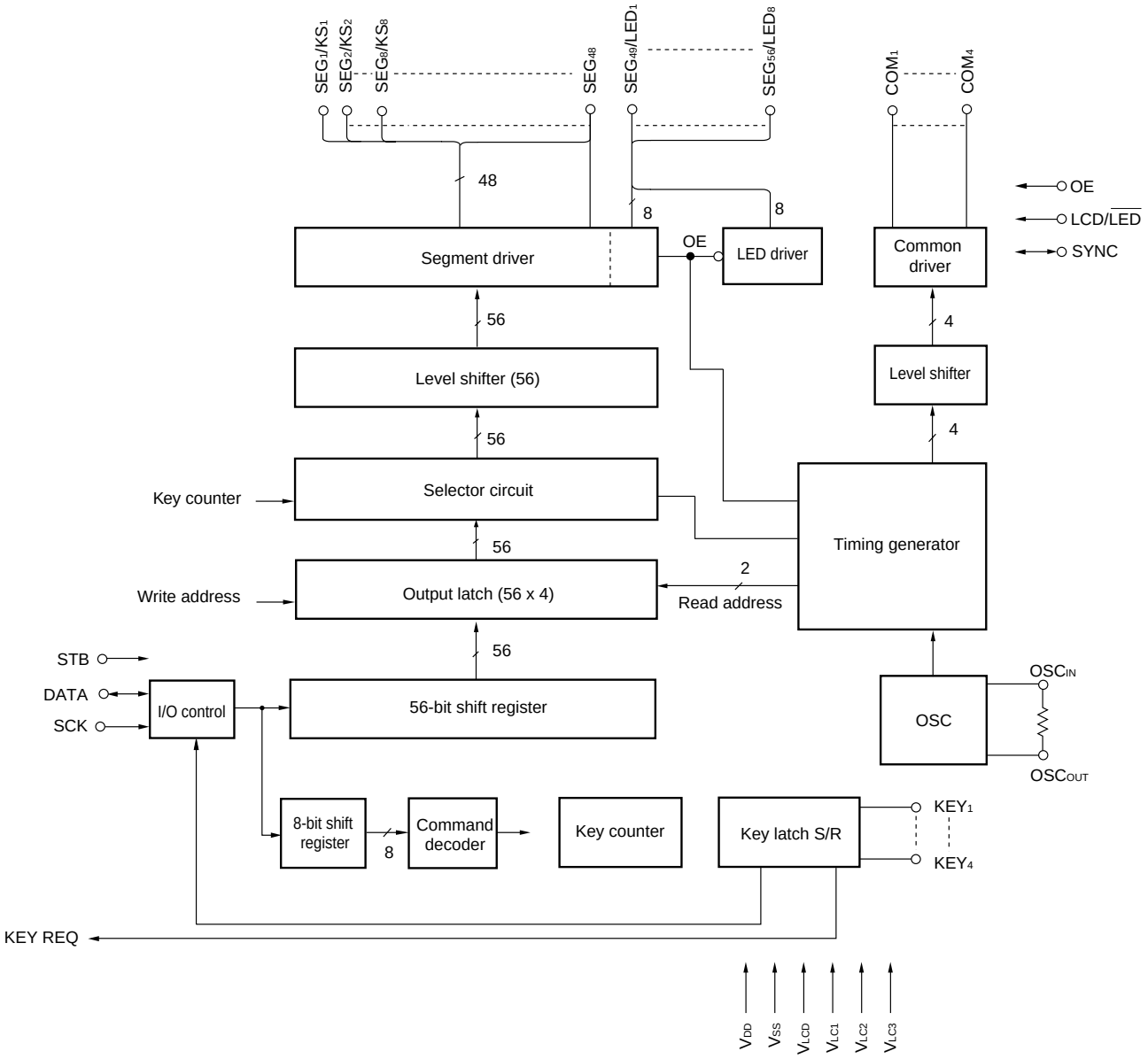
Part Number	Package
μPD16431AGC-7ET	80-PIN PLASTIC LQFP (14 x 14), 0.65 pitch

Document No. S15129EJ3V0DS00 (3rd Edition)
Date Published December 2001 NS CP(K)

The mark ★ shows major revised points.

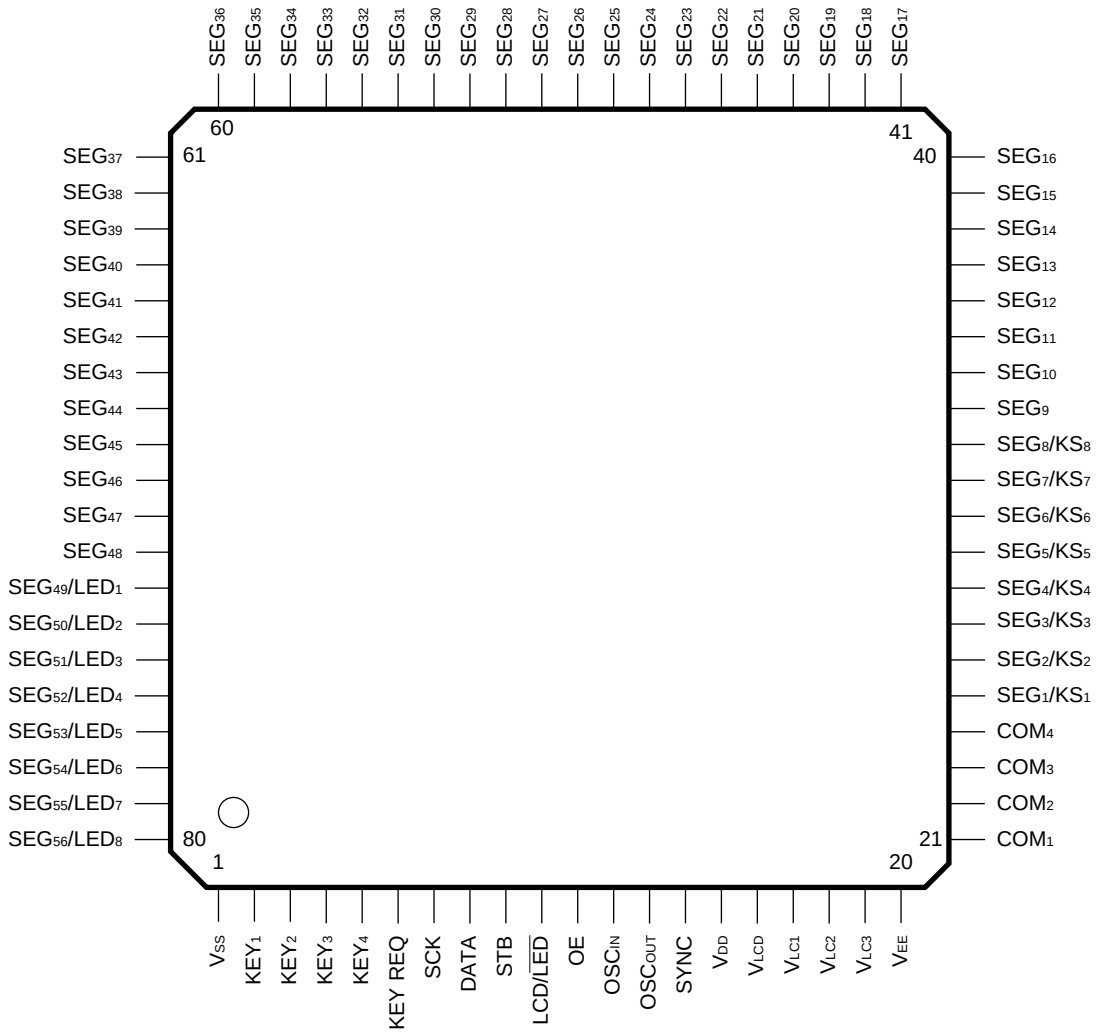
CONTENT

1. BLOCK DIAGRAM



2. PIN CONFIGURATION

- **μPD16431AGC-7ET**



Note Though V_{SS} and V_{EE} are internally connected, be sure to connect all the power supply pins (V_{DD}, V_{SS}, V_{LCD}, and V_{EE}).

3. PIN DESCRIPTIONS

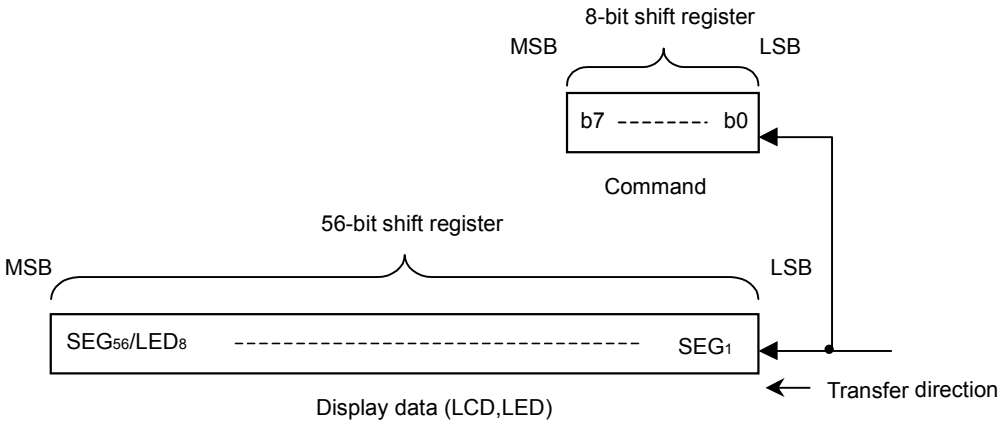
Symbol	Pin Name	Pin No.	I/O	Function
SEG_1/KS_1 to SEG_8/KS_8	Segment/key source	25 to 32	O	These pins serve as LCD segment output pins and key source output pins for key scanning.
SEG_9/SEG_{48}	Segment	33 to 72	O	LCD segment output pins.
SEG_{49}/LED_1 to SEG_{56}/LED_8	Segment/LED	73 to 80	O	These pins can be used as LCD segment output or LED output pins depending on the setting of the LCD/$\overline{LED}$ pin.
COM_1 to COM_4	Common	21 to 24	O	LCD common output pins
SCK	Shift clock	7	I	Data shift clock. Data is read at the rising edge, and is output at the falling edge of this clock.
DATA	Data	8	I/O	This pin inputs a command or display data, or outputs key data. A command or data is input at the rising edge of the shift clock, starting from the most significant bit. Key data is output at the falling edge of the shift clock, starting from the most significant bit. This pin serves as an open-drain pin in the output mode. Output is CMOS output.
STB	Strobe	9	I	Data can be input when this signal goes low. When it goes high, command processing is performed.
LCD/$\overline{LED}$	LCD/LED select	10	I	When this signal goes high, the SEG_n/LED_m pins function as LCD segment output pins; when it goes low, they function as LED driver output pins. The LED driver has a drive capability of 15 mA and is N-ch open drain.
$\overline{OE}$ Note	Output enable	11	I	When this signal goes low, all the segment output and LED output pins are off ($SEG_n = COM_n = V_{LCD}$). Internal data are saved.
OSC_{IN}	Oscillation	12	I	Connect a resistor for oscillation circuit across these pins. When an external oscillator is used, input a clock signal to the OSC_{IN} pin and leave the OSC_{OUT} pin open, depending on the setting status of the CLS pin.
OSC_{OUT}		13	O	
SYNC	Synchronizing signal	14	I/O	A synchronizing signal input pin. When two or more μPD16431As are used, each device is wired-ORed. This pin must be pulled up when this chip is used alone.
KEY_1 to KEY_4	Key data	2 to 5	I	Key data input pins for key scanning.
KEY REQ	Key request	6	O	This signal goes high when a key is pressed (key data = H). Read the key data only while this pin is high.
V_{DD}	Logic power supply	15	–	Power supply pin for internal logic.
V_{SS}	Logic GND	1	–	GND pin for internal logic and LED output.
V_{LCD}	LCD drive power supply	16	–	Power supply pin for LCD drive.
V_{EE}	LCD GND	20	–	GND pin for LCD drive.
V_{LC1} to V_{LC3}	Power supply for LCD drive	17 to 19	–	Power supply for driving dot matrix LCD.

Note At OE = L, the key data cannot be written correctly, even when the display ON/OFF of the status command is set to the 'normal operation' (10). Also, in this state, unnecessary waveforms are generated from between SEG_1/KS_1 to SEG_8/KS_8 during the key scanning period (the display is OFF).

4. PIN FUNCTION

4.1 Configuration of Shift Register

Two shift registers, an 8-bit command register and a 56-bit display register, are provided. The first 8 bits of input data are recognized as a command and are sent to the command register, and the 9th bit and those that follow are recognized as display data and are sent to the display register.



The meaning of the display data is as follows:

LCD: 0 → OFF, 1 → ON

LED: 0 → ON, 1 → OFF

Be sure to transfer 56 bits of display data.

4.2 Configuration of Output Latch

MSB		LSB	
SEG56/LED8	----------	SEG1	COM1 (latch address[Note]:00)
SEG56/LED8	----------	SEG1	COM2 (latch address[Note]:01)
SEG56/LED8	----------	SEG1	COM3 (latch address[Note]:10)
SEG56/LED8	----------	SEG1	COM4 (latch address[Note]:11)

Note Bits b3 and b4 of status command (Refer to **5. COMMAND (2) Status Command**).

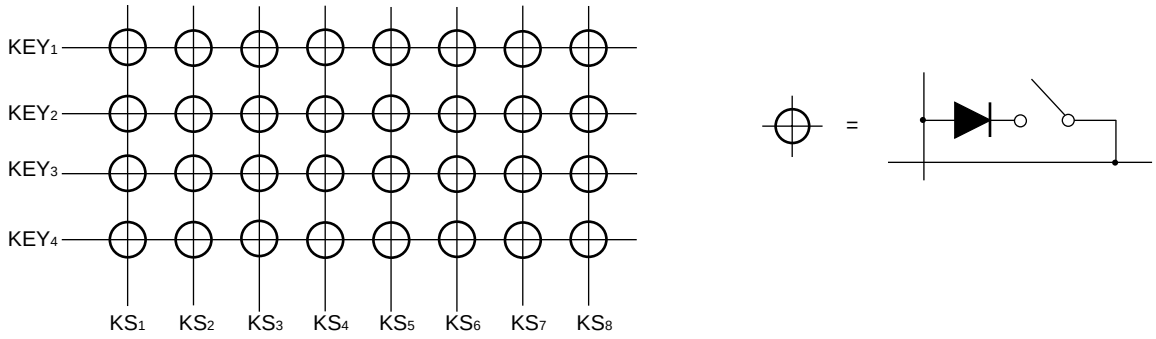
4.3 Key Matrix Configuration

An example of key matrix configurations is shown below.

(1) When pressing three or more times is assumed:

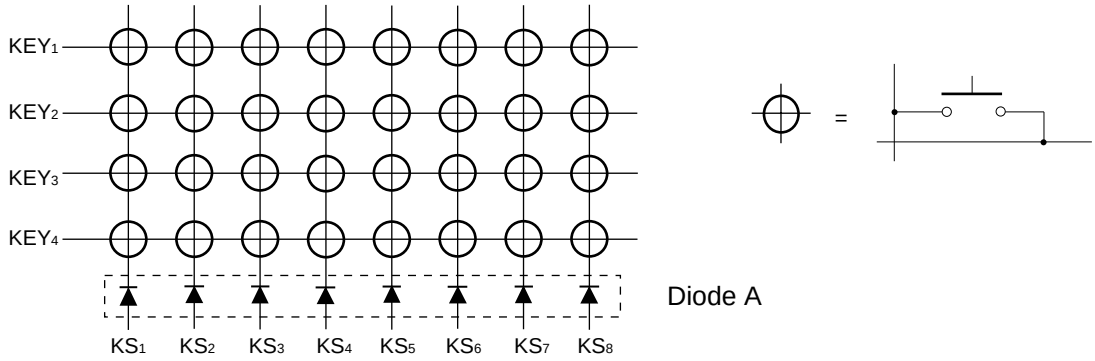
★ In this configuration, it is assumed that three or more switches are pressed simultaneously.

Note, however, that if three or more switches are pressed per KS (Key source output), the switches may not be recognized correctly.



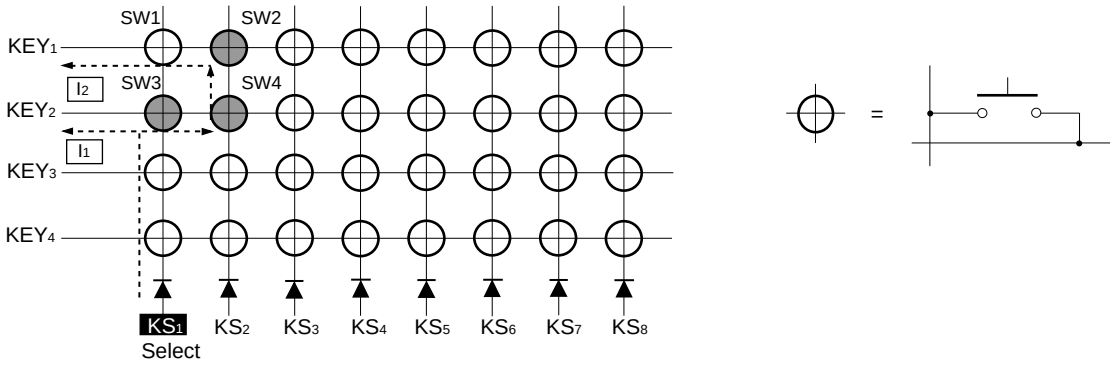
(2) When pressing twice or more times is assured:

A configuration example is shown below. In this configuration, 0 to 2 ON switches can be recognized.



In this configuration, pressing three or more switches simultaneously may cause OFF switches to be determined to be ON.

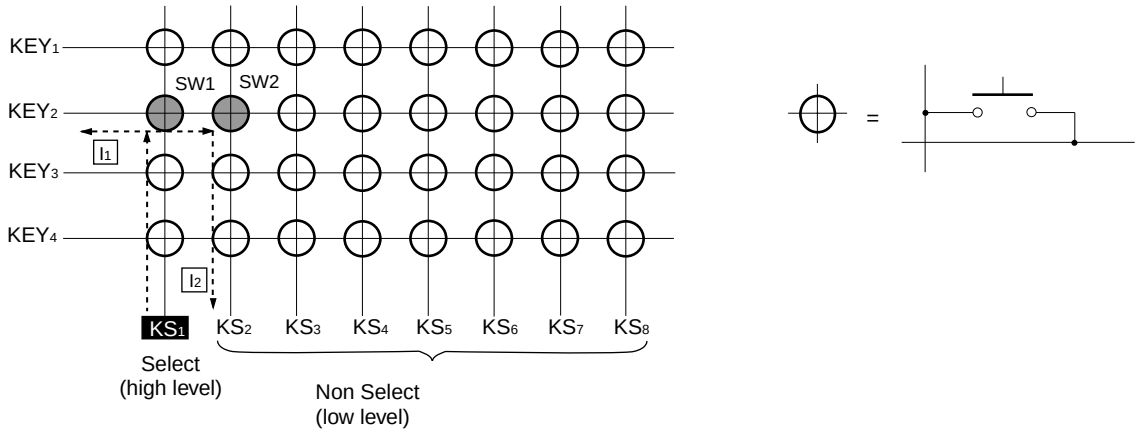
For example, if SW2 to SW4 are ON and KS_1 has been selected (high level) as shown below, SW3 in which current I_1 is running is supposed to be detected to be ON. However, since SW2 and SW4 are ON, current I_2 runs thus resulting in SW1 to be recognized as being ON.



If diode A is not available, not only the key data may not be read correctly, but the LCD display may be affected or IC may be damaged or deteriorated.

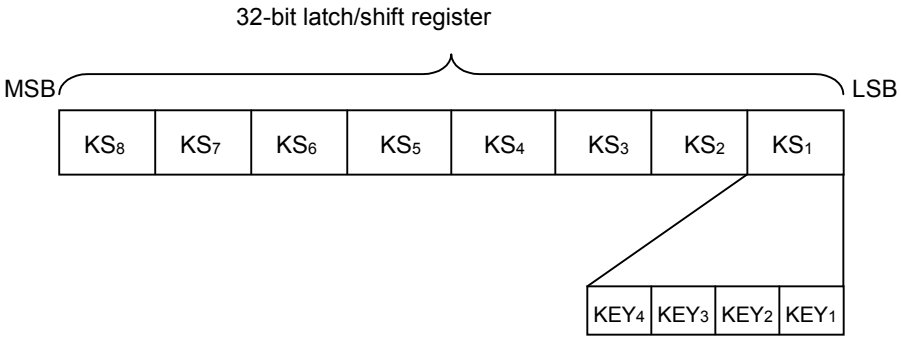
For example, if SW1 and SW2 are ON and KS_1 has been selected (high level) as shown below, this will cause not only current I_1 which is supposed to run but also short-circuited current I_2 of KS_1 and KS_2 to run. It is possible that this will then cause the following three problems:

(1) Since the level to KEY_2 is not correctly sent, the key data cannot be latched correctly.
(2) If KS_2 is used as SEG_2 as well, the LCD display may be distorted (such as causing unintended segments to light up).
(3) Since the short-circuited current (current I_2) of KS_2 (high level) to KS_2 (low level) runs, IC may be damaged or deteriorated.



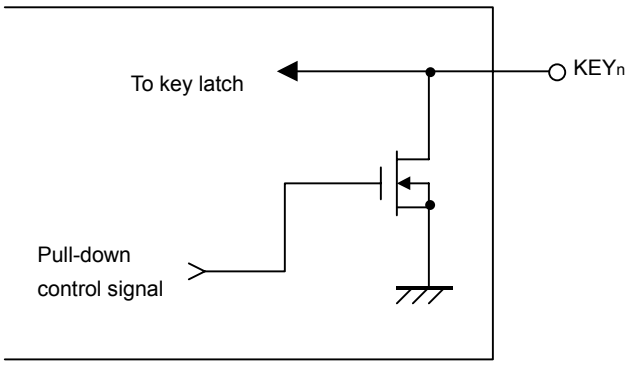
4.4 Configuration of Key Data Latch

The key data is latched as illustrated below and is read by a read command, starting from the most significant bit. Key data is read once a frame and latched when coinciding with the immediately preceding data. In other words, it requires at least 2 frames from the time the key is pressed till data is confirmed to be the key data (the key request becoming H).



The key data is 0 when off and 1 when on.

4.4.1 Key input equivalent circuit



- The pull-down control signal goes high only during key source output and turns on the pull-down transistor.
- The on-resistance of the pull-down transistor is several kΩ.

5. COMMAND

A command sets a display mode and a status.

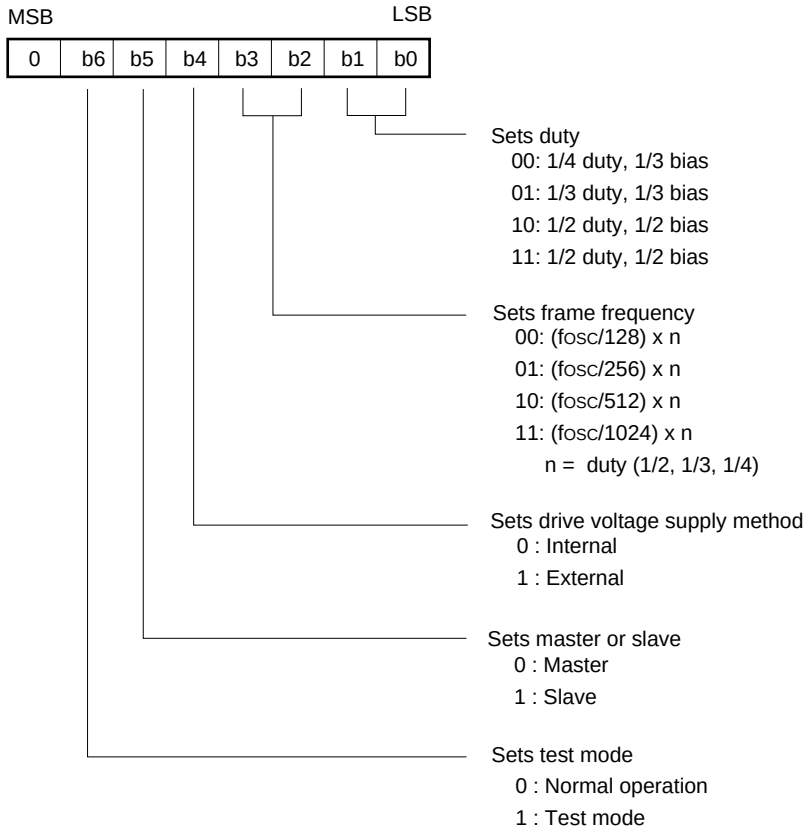
The first 1 byte input after the STB pin has fallen is regarded as a command.

If the STB pin is made low while a command/data is transferred, serial communication is initialized, and the command/data being transferred is made invalid (the command/data that has been already transferred remains valid, however).

(1) Display setting command

This command initializes the μPD16431A and sets a duty cycle, frame frequency, drive voltage supply method, test mode, and whether the μPD16431A operates as the master or a slave.

When this command is executed, display is forcibly turned off and key scanning is stopped. To resume the display, the normal operation of the 'status command' must be executed. Note, however, that nothing is executed if the same mode is selected.

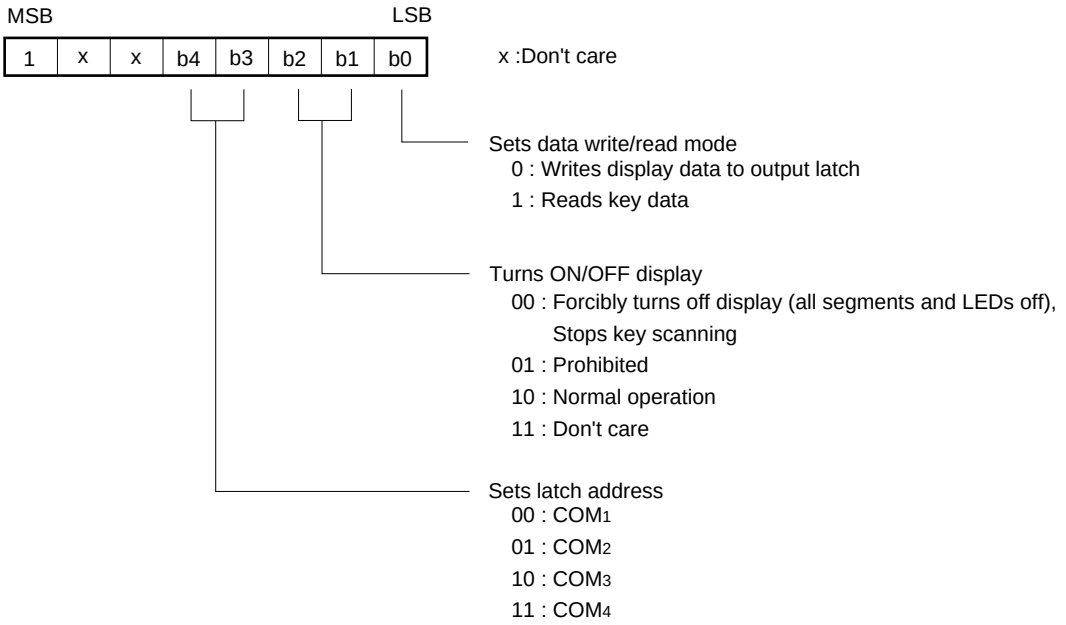


Values when power is applied

	0	0	0	0	0	0	0

(2) Status command

This command sets a data write/read mode, turns ON/OFF display, and sets a latch address.



Value when power is applied

	x	x	0	0	0	0	0

6. OUTPUT SELECT VOLTAGE

(1) COM

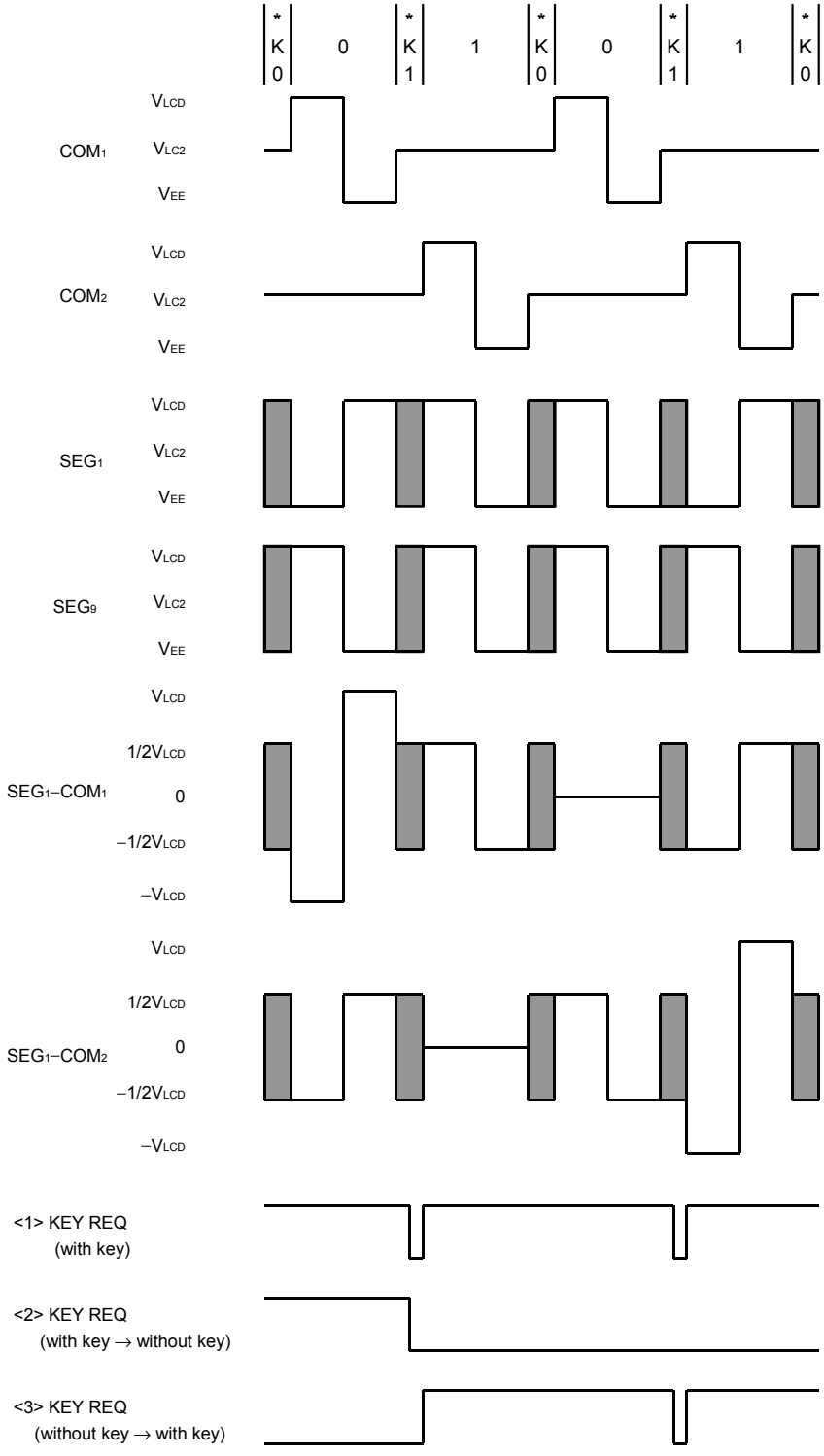
Parameter	Power supply	+	–	Bias
When selected	Internal	V_{LCD}	GND	1/2 bias
	External	V_{LCD}	GND	
When not selected	Internal	$1/2V_{LCD}$	$1/2V_{LCD}$	
	External	V_{LC2}	V_{LC2}	
When key scanned	Internal	$1/2V_{LCD}$	$1/2V_{LCD}$	
	External	V_{LC2}	V_{LC2}	
When selected	Internal	V_{LCD}	GND	1/3 bias
	External	V_{LCD}	GND	
When not selected	Internal	$1/3V_{LCD}$	$2/3V_{LCD}$	
	External	V_{LC3}	V_{LC1}	
When key scanned	Internal	$1/2V_{LCD}$	$1/2V_{LCD}$	
	External	V_{LC2}	V_{LC2}	

(2) SEG

Parameter	Power supply	+	–	Bias
When selected	Internal	GND	V_{LCD}	1/2 bias
	External	GND	V_{LCD}	
When not selected	Internal	V_{LCD}	GND	
	External	V_{LCD}	GND	
When key scanned	Internal	GND	V_{LCD}	
	External	GND	V_{LCD}	
When key not scanned	Internal	V_{LCD}	GND	
	External	V_{LCD}	GND	
When selected	Internal	GND	V_{LCD}	1/3 bias
	External	GND	V_{LCD}	
When not selected	Internal	$2/3V_{LCD}$	$1/3V_{LCD}$	
	External	V_{LC1}	V_{LC3}	
When key scanned	Internal	GND	V_{LCD}	
	External	GND	V_{LCD}	
When key not scanned	Internal	V_{LCD}	GND	
	External	V_{LCD}	GND	

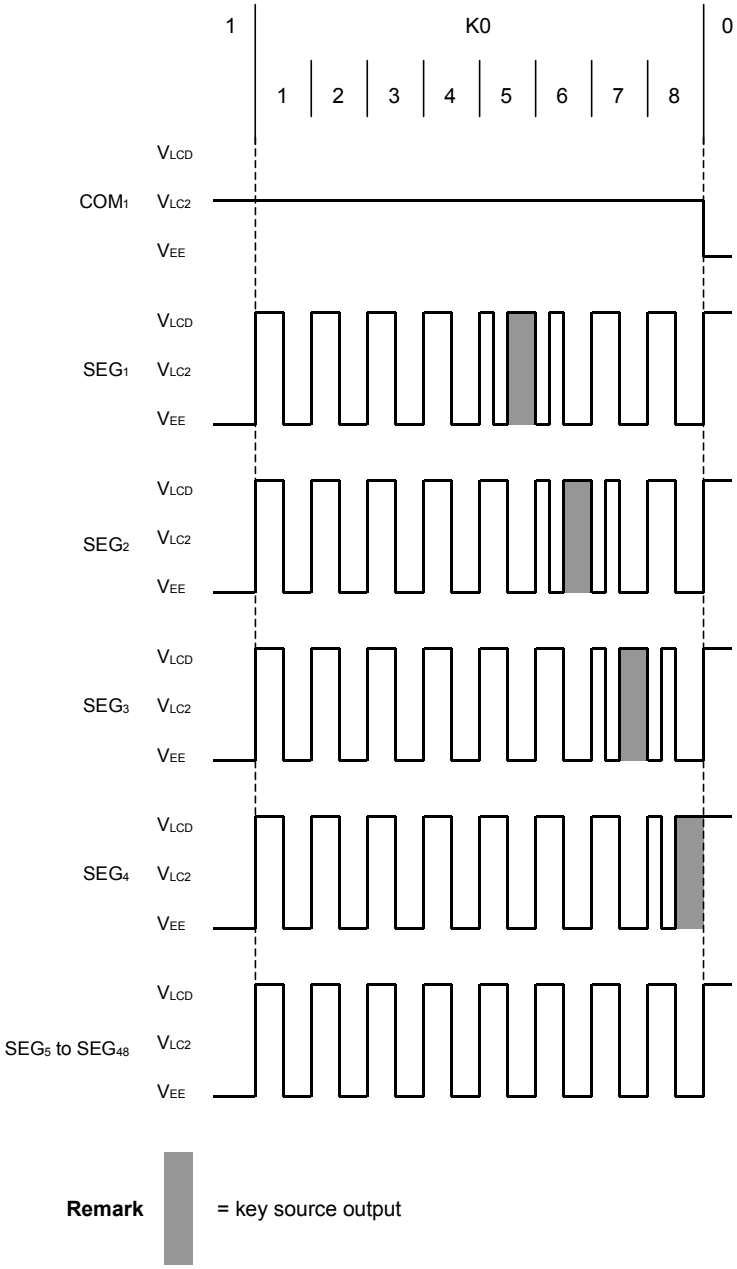
7. OUTPUT WAVEFORM

7.1 1/2 Duty (1/2 bias)

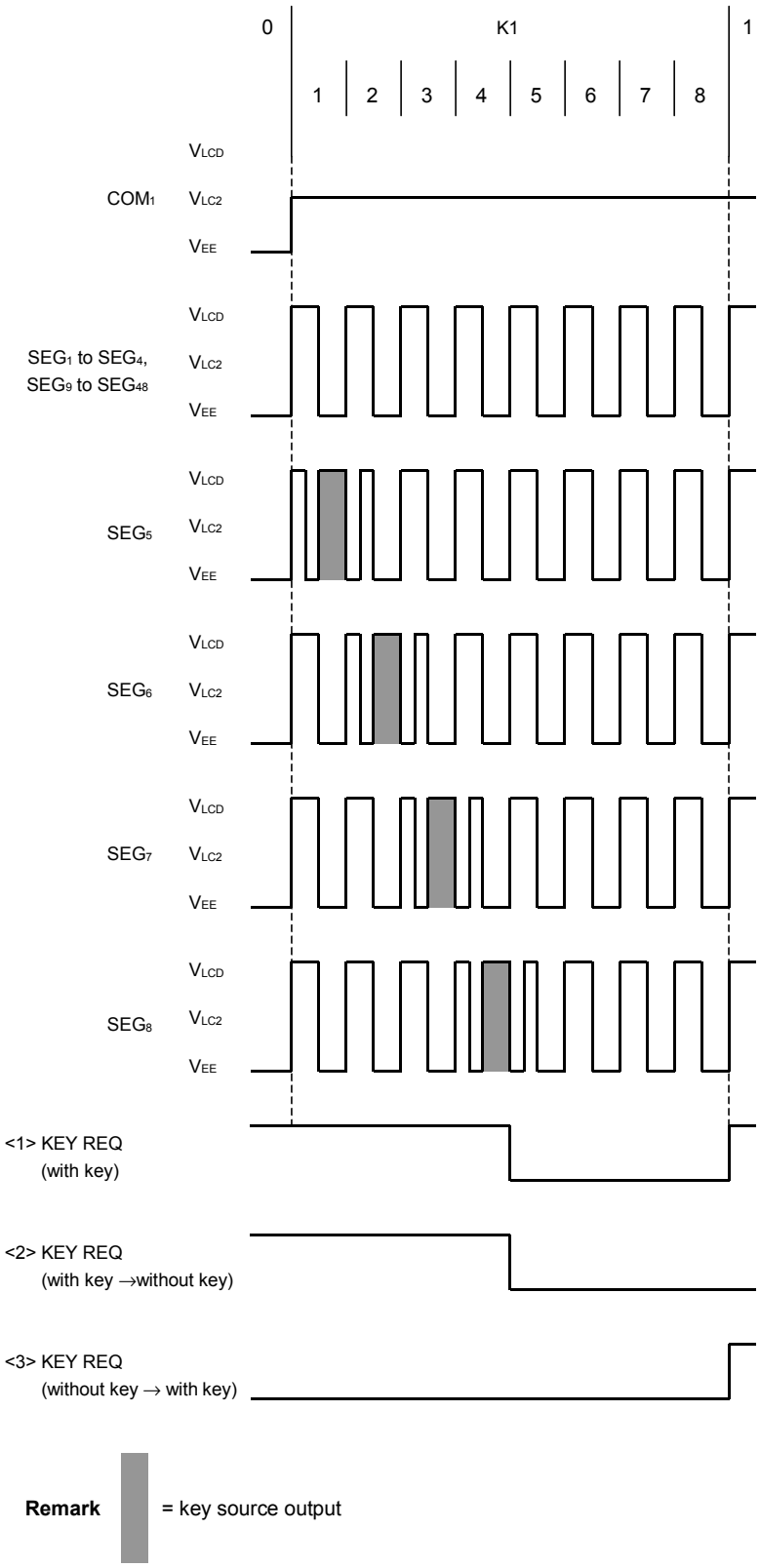


Remark *: Key scan period (16/fC)

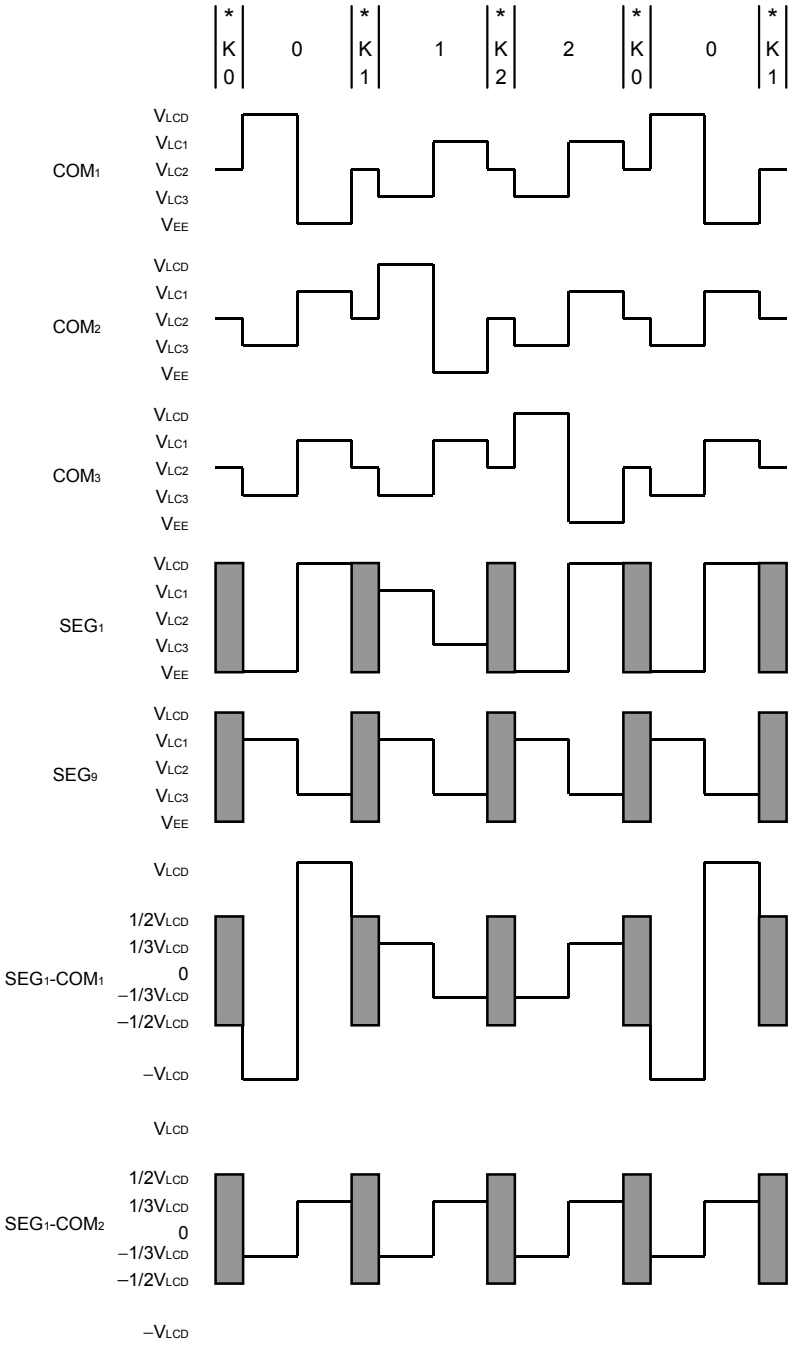
(1) Key scan period (K0) expansion



(2) Key scan period (K1) expansion

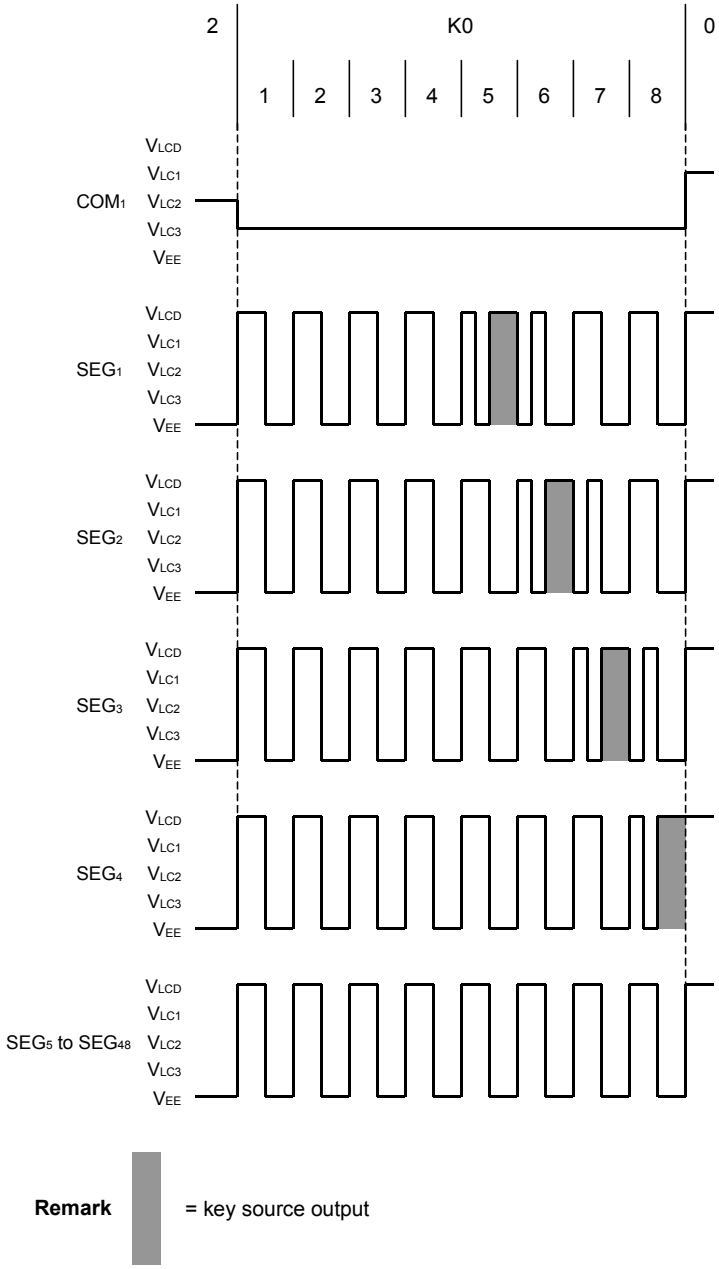


7.2 1/3 Duty (1/3 bias)



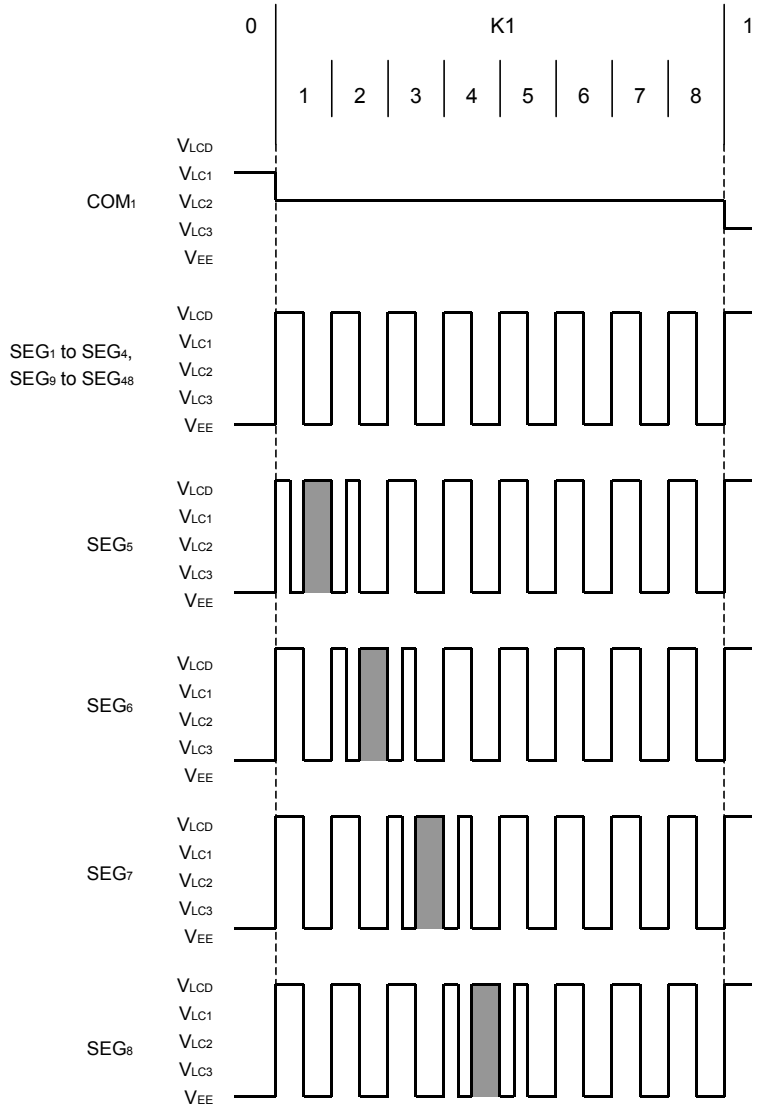
Remark * = key scan period (16/fc)

(1) Key scan period (K0) expansion



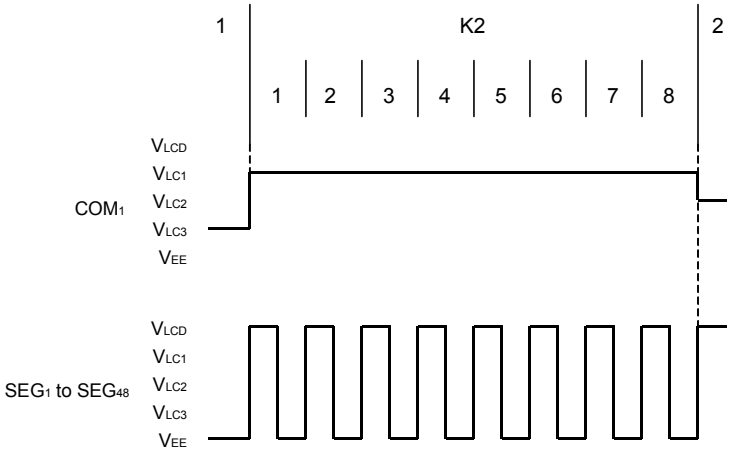
Remark = key source output

(2) Key scan period (K1) expansion

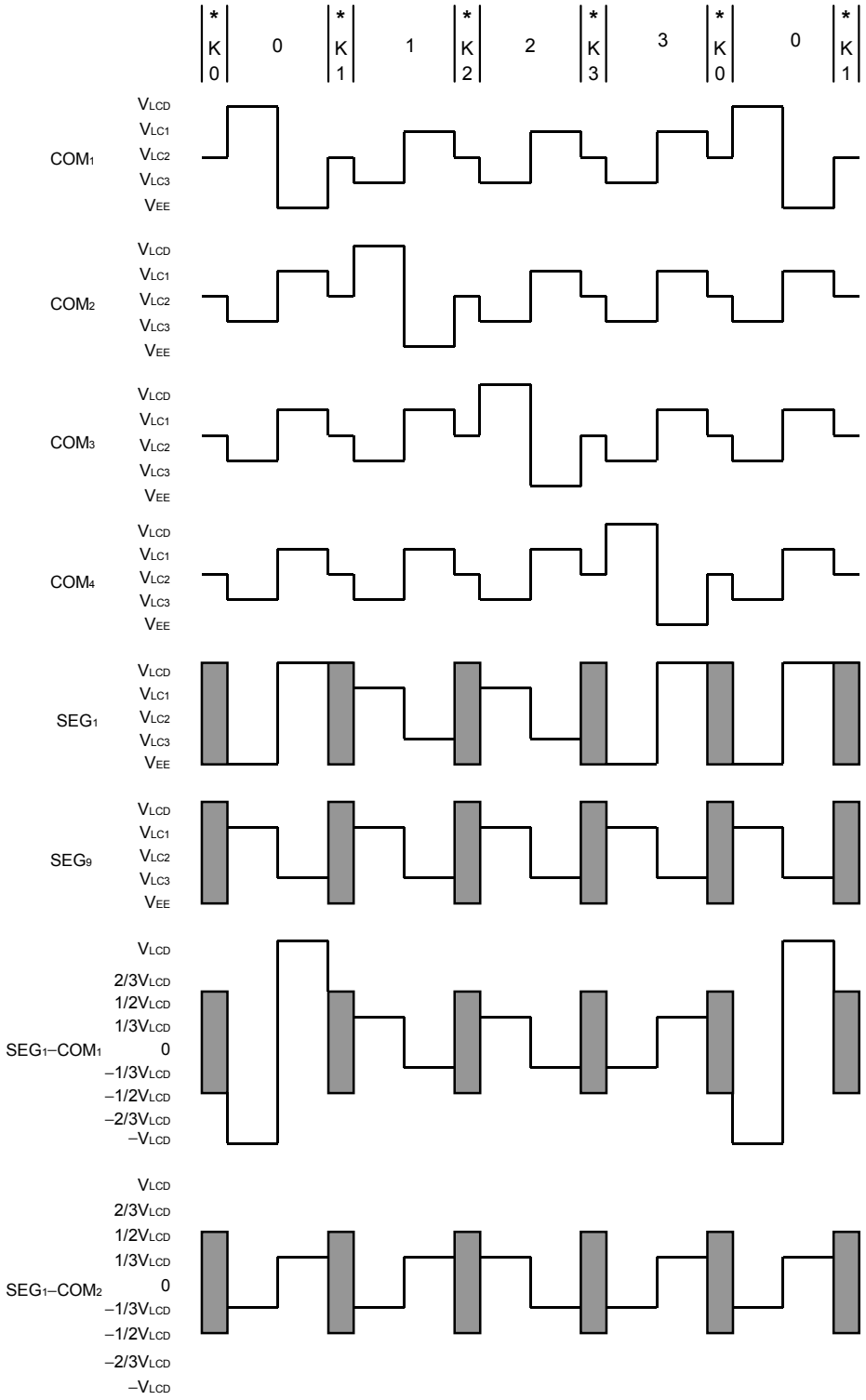


Remark = key source output

(3) Key scan period (K2) expansion

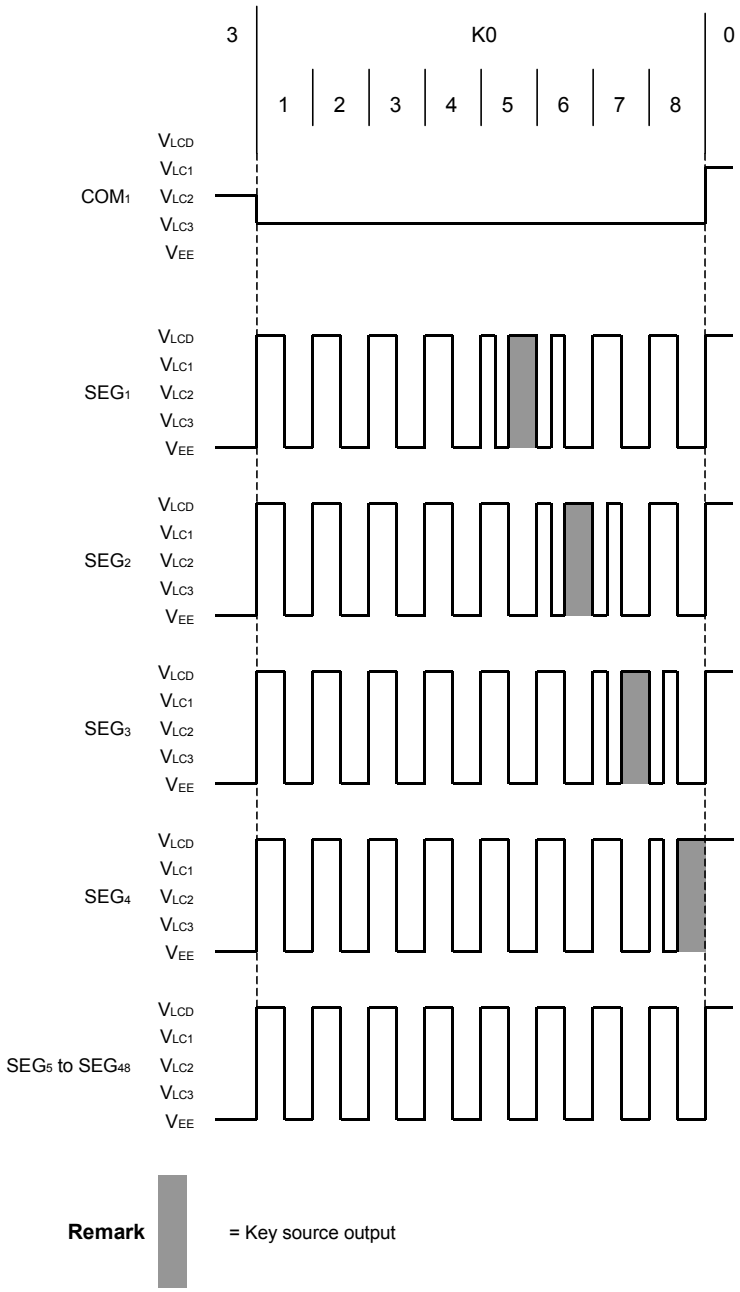


7.3 1/4 Duty (1/3 bias)



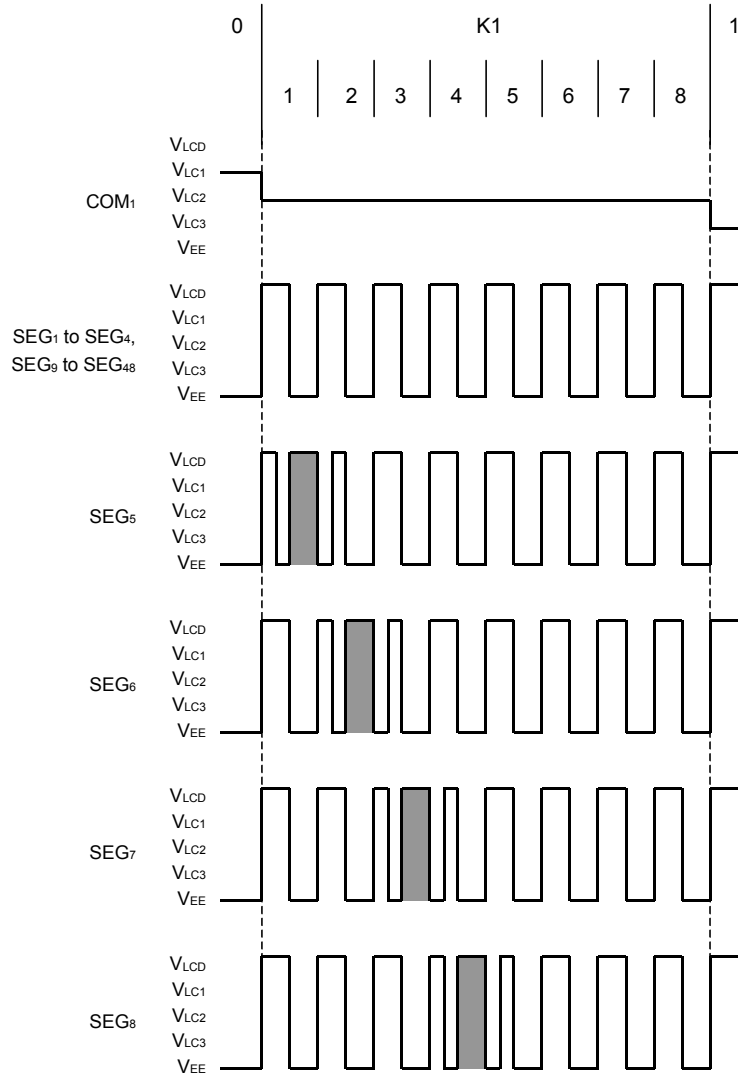
Remark * : Key scan period (16/fC)

(1) Key scan period (K0) expansion



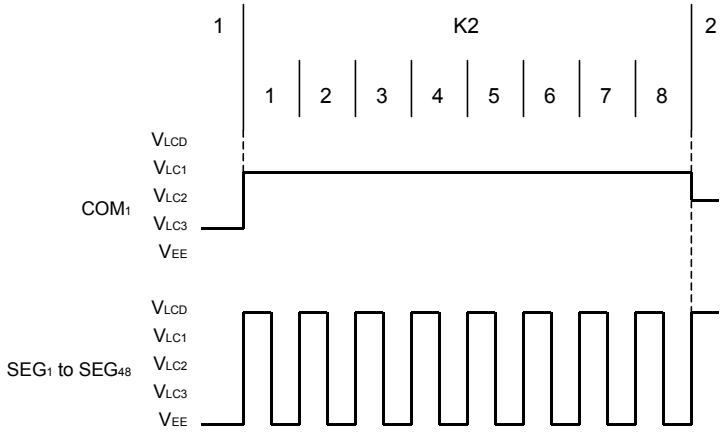
Remark = Key source output

(2) Key scan period (K1) expansion

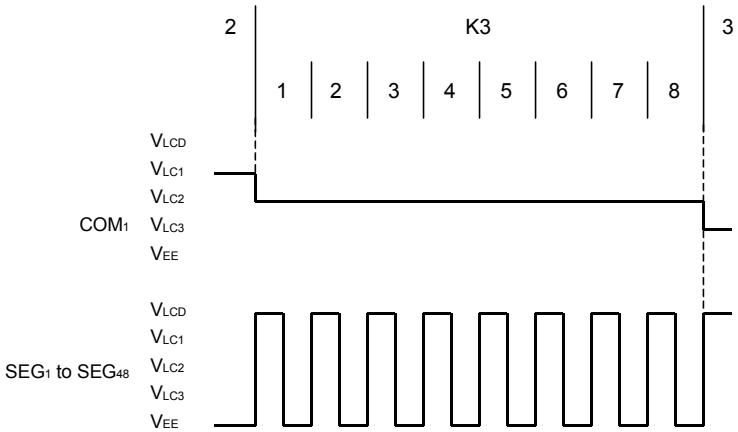


Remark = Key source output

(3) Key scan period (K2) expansion

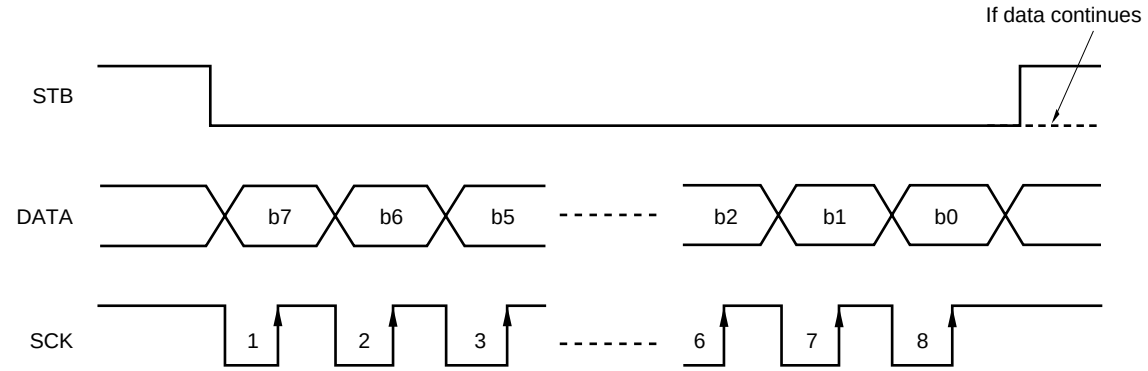


(4) Key scan period (K3) expansion

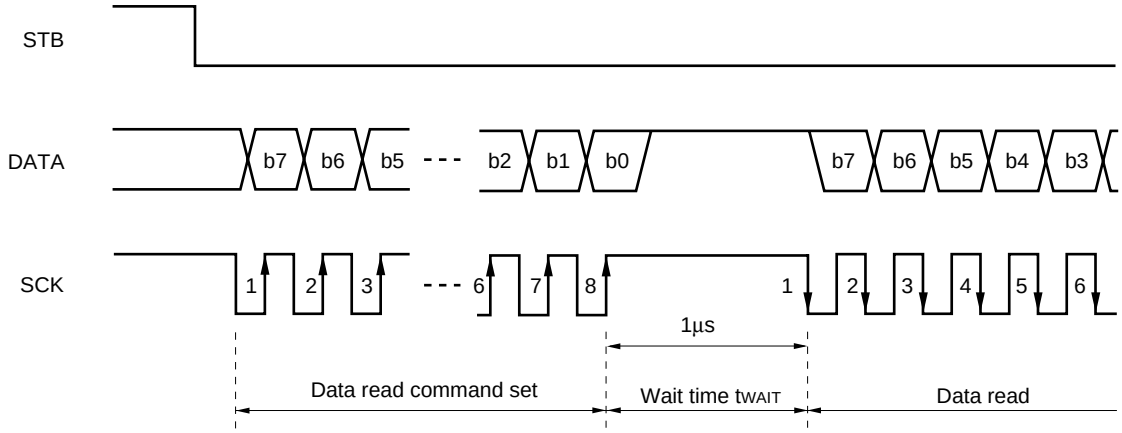


7.4 Serial Communication Format

(1) Receive (command/data write)



(2) Transmit (command/data read)



8. APPLICATION

8.1 Example of Initial Setting + Display Data Write

Parameter	STB	Command/data								Remarks
		b7	b6	b5	b4	b3	b2	b1	b0	
Start	H									
Set display command	L	0	0	0	0	0	0	0	0	1/4duty, frame frequency = fOSC/128 x 1/4, internal drive voltage, master
	H									
Status command	L	1	0	0	0	0	0	0	0	Display data write, display OFF, latch address: COM_1
Display data 1 : Display data 7	L : L	x x	x x	x x	x x	x x	x x	x x	x x	} COM_1 data (7bytes)
	H									
Status command	L	1	0	0	0	1	0	0	0	Display data write, display OFF, latch address: COM_2
Display data 1 : Display data 7	L : L	x x	x x	x x	x x	x x	x x	x x	x x	} COM_2 data (7 bytes)
	H									
Status command	L	1	0	0	1	0	0	0	0	Display data write, display OFF, latch address: COM_3
Display data 1 : Display data 7	L : L	x x	x x	x x	x x	x x	x x	x x	x x	} COM_3 data (7 bytes)
	H									
Status command	L	1	0	0	1	1	0	0	0	Display data write, display OFF, latch address: COM_4
Display data 1 : Display data 7	L : L	x x	x x	x x	x x	x x	x x	x x	x x	} COM_4 data (7 bytes)
	H									
Status command	L	1	0	0	0	0	1	0	0	Display data write, display ON
End	H									

8.2 Example of Display Data Write (Rewrite, 1/4)

Parameter	STB	Command/data								Remarks
		b7	b6	b5	b4	b3	b2	b1	b0	
Start	H									
Status command	L	1	0	0	0	0	1	0	0	Display data write, display ON, latch address: COM_1
Display data 1	L	x	x	x	x	x	x	x	x	} COM_1 data (7bytes)
:	:									
Display data 7	L	x	x	x	x	x	x	x	x	
	H									
Status command	L	1	0	0	0	1	1	0	0	Display data write, display ON, latch address: COM_2
Display data 1	L	x	x	x	x	x	x	x	x	} COM_2 data (7 bytes)
:	:									
Display data 7	L	x	x	x	x	x	x	x	x	
	H									
Status command	L	1	0	0	1	0	1	0	0	Display data write, display ON, latch address: COM_3
Display data 1	L	x	x	x	x	x	x	x	x	} COM_3 data (7 bytes)
:	:									
Display data 7	L	x	x	x	x	x	x	x	x	
	H									
Status command	L	1	0	0	1	1	1	0	0	Display data write, display ON, latch address: COM_4
Display data 1	L	x	x	x	x	x	x	x	x	} COM_4 data (7 bytes)
:	:									
Display data 7	L	x	x	x	x	x	x	x	x	
End	H									

8.3 Example of Display Data Read

Parameter	STB	Command/data								Remarks
		b7	b6	b5	b4	b3	b2	b1	b0	
KEY REQ check										KEY REQ = H: Key data exists → Start reading. KEY REQ = L: Key data does not exist (reading is inhibited). → Check KEY REQ again.
Start	H									
Status command	L	1	0	0	0	0	1	0	1	Data read, display ON
Wait time	L									1 μs
Key data 1	L	x	x	x	x	x	x	x	x	} 4 bytes
:	:									
Key data 4	L	x	x	x	x	x	x	x	x	
End	H									

9. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic supply voltage	V_{DD}	−0.3 to + 7.0	V
Logic input voltage	V_{IN}	−0.3 to + V_{DD} + 0.3	V
Logic output voltage (DATA)	V_{OUT}	−0.3 to + 7.0	V
LCD drive supply voltage	V_{LCD}	−0.3 to + 7.0	V
LCD drive supply input voltage	V_{LC1} to V_{LC3}	−0.3 to V_{LCD} + 0.3	V
Drive output voltage (segment, common, LED)	V_{OUT2}	−0.3 to V_{LCD} + 0.3	V
LED output current	I_O	20	mA
Package allowable dissipation	P_T	1000	mW
Operating ambient temperature	T_A	−40 to + 85	°C
Storage temperature range	T_{stg}	−55 to + 150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V_{DD}		2.7	5.0	5.5	V
LCD drive supply voltage	V_{LCD}		V_{DD}	5.0	6.5	V
Logic input voltage	V_{IN}		0		V_{DD}	V
Drive output voltage	V_{LC1} to V_{LC3}		0		V_{LCD}	V

Electrical Characteristics (Unless otherwise specified, T_A = –40 to +85°C, V_{DD} = V_{LCD} = 5 V ± 10%)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}		0.7 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL}		0		0.3 V_{DD}	V
Input current, high	I_{IH}	SCK, STB, LCD/$\overline{\text{LED}}$, OE			1	μA
Input current, low	I_{IL}	SCK, STB, LCD/$\overline{\text{LED}}$, OE			−1	μA
Output voltage, low	V_{OL1}	LED_1 to LED_8, I_{OL1} = 15 mA			1.0	V
Output voltage, high	V_{OH2}	OSC_{OUT}, I_{OH2} = −1 mA	0.9 V_{DD}			V
Output voltage, low	V_{OL2}	DATA, OSC_{OUT}, SYNC, I_{OL2} = 4 mA			0.1 V_{DD}	V
Leakage current, high	I_{LOH2}	DATA, SYNC, $V_{IN/OUT}$ = V_{DD}			1	mA
Leakage current, low	I_{LOL2}	DATA, SYNC, $V_{IN/OUT}$ = V_{SS}			−1	mA
Common output ON resistance	R_{COM}	COM_1 to COM_4, $\lvert I_O \rvert$ = 100 μA			2.4	kΩ
Segment output ON resistance	R_{SEG}	SEG_1 to SEG_{56}, $\lvert I_O \rvert$ = 100 μA			4.0	kΩ
Logic current dissipation	I_{DD}	f_{OSC} = 250 kHz			250	μA
LCD drive current consumption	I_{LCD}	With internal bias and no load			500	μA

Remark TYP. values are reference values at T_A = 25°C.

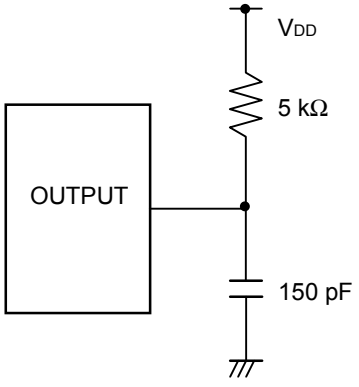
Switching Characteristics (Unless otherwise specified, T_A = –40 to +85°C, V_{DD} = V_{LCD} = 5 V ± 10%, R_L = 5 kΩ, C_L = 150 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{OSC}	R = 100 kΩ	175	250	325	kHz
		R = 200 kΩ	105	150	195	kHz
Propagation delay time	t_{PZL}	SCK↓→DATA↓			100	ns
	t_{PLZ}	SCK↓→DATA↑			300	ns
SYNC delay time	t_{DSYNC}				1.5	μs

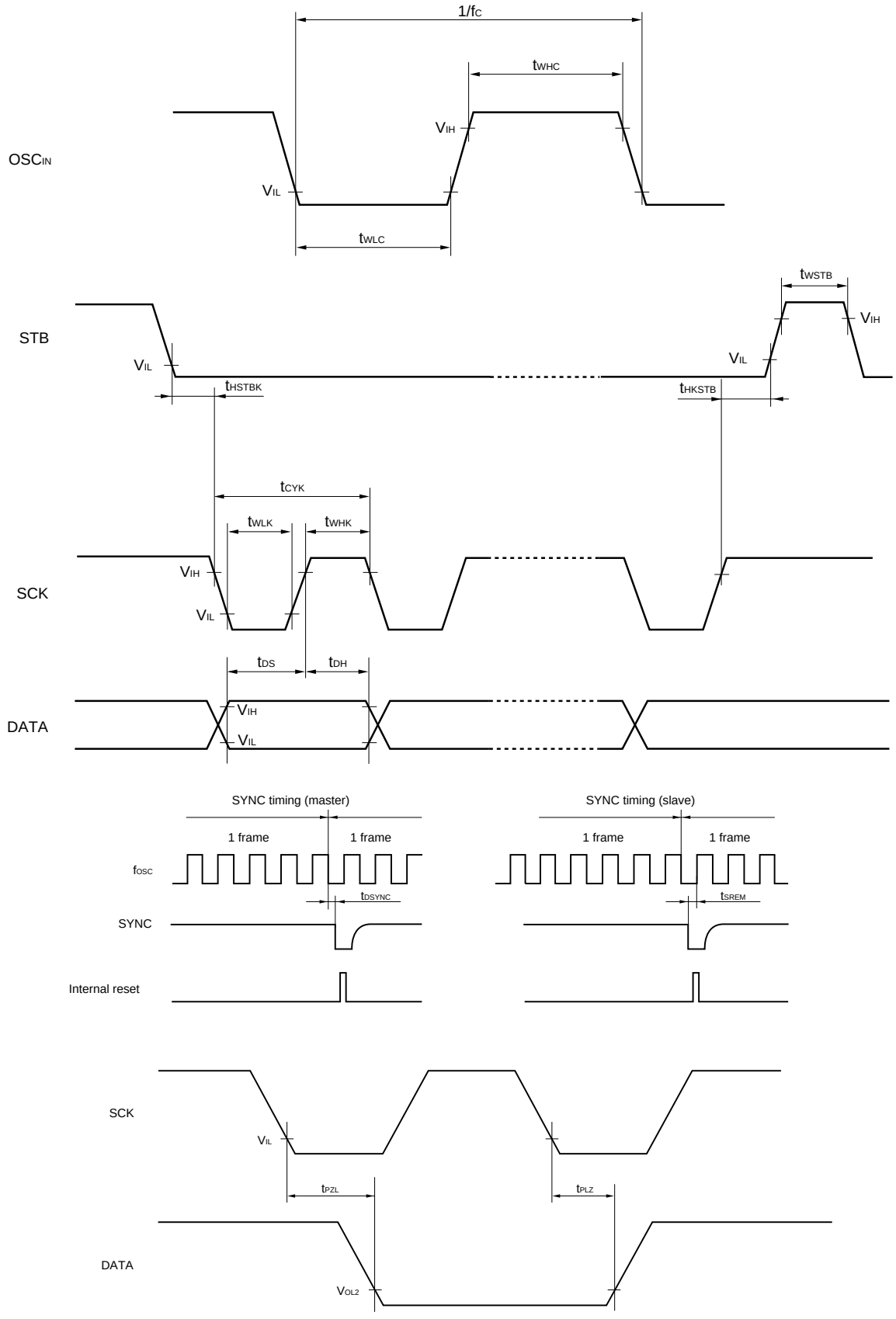
Timing Requirements (Unless otherwise specified, T_A = –40 to +85°C, V_{DD} = V_{LCD} = 5 V ± 10%, R_L = 5 kΩ, C_L = 150 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock frequency	f_C	OSC_{IN} external clock	50		325	kHz
High-level clock pulse width	t_{WHC}	OSC_{IN} external clock	1.5		16	μs
Low-level clock pulse width	t_{WLC}	OSC_{IN} external clock	1.5		16	μs
Shift clock cycle	t_{CYK}	SCK	900			ns
High-level shift clock pulse width	t_{WHK}	SCK	400			ns
Low-level shift clock pulse width	t_{WLK}	SCK	400			ns
Shift clock hold time	t_{HSTBK}	STB↓→SCK↓	1.5			μs
Data setup time	t_{DS}	DATA→SCK↑	100			ns
Data hold time	t_{DH}	SCK↑→DATA	200			ns
STB hold time	t_{HKSTB}	SCK↑→STB↑	1			μs
STB pulse width	t_{WSTB}		1			μs
Wait time	t_{WAIT}	CLK↑→CLK↓	1			μs
SYNC removal time	t_{SREM}		250			ns

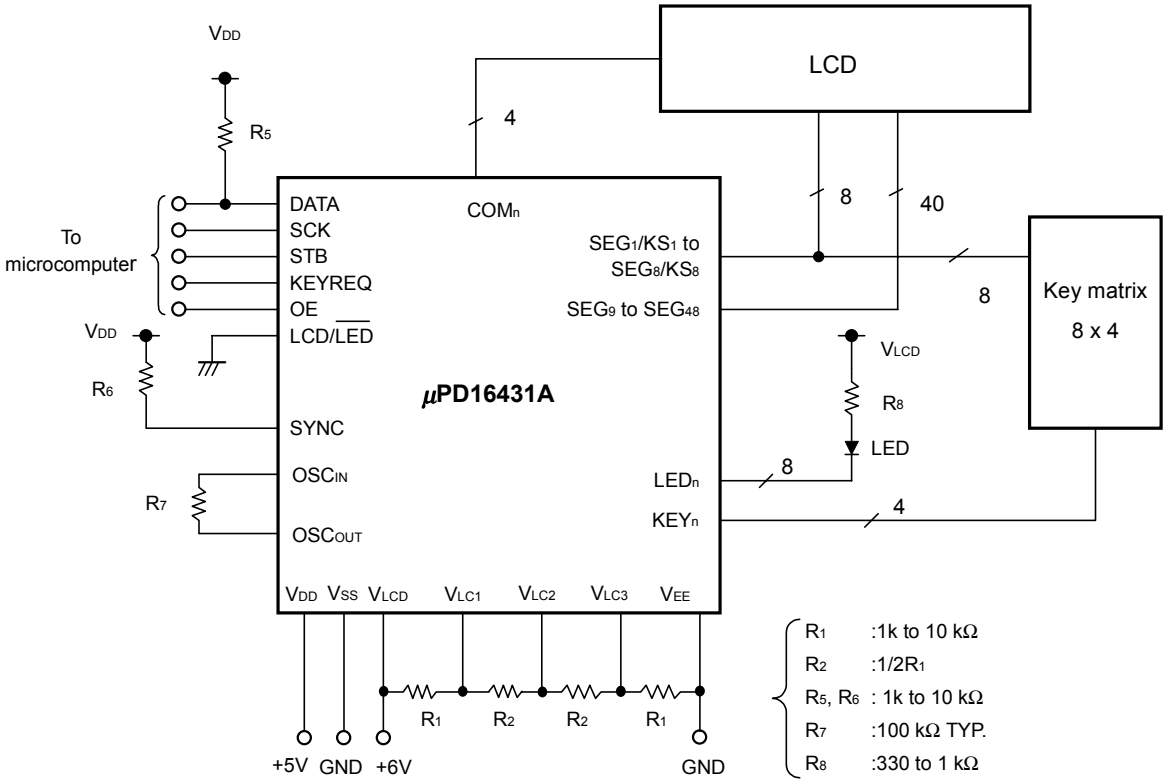
Output road



Switching Characteristic Waveform

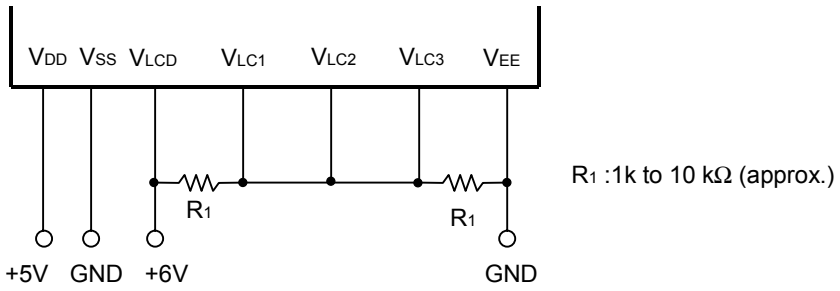


10. APPLICATION CIRCUIT EXAMPLE (with LED, 1/4 duty, 1/3 bias)



R1 and R2 are not necessary when the internal drive voltage is selected (VLC1 to VLC3 are open).

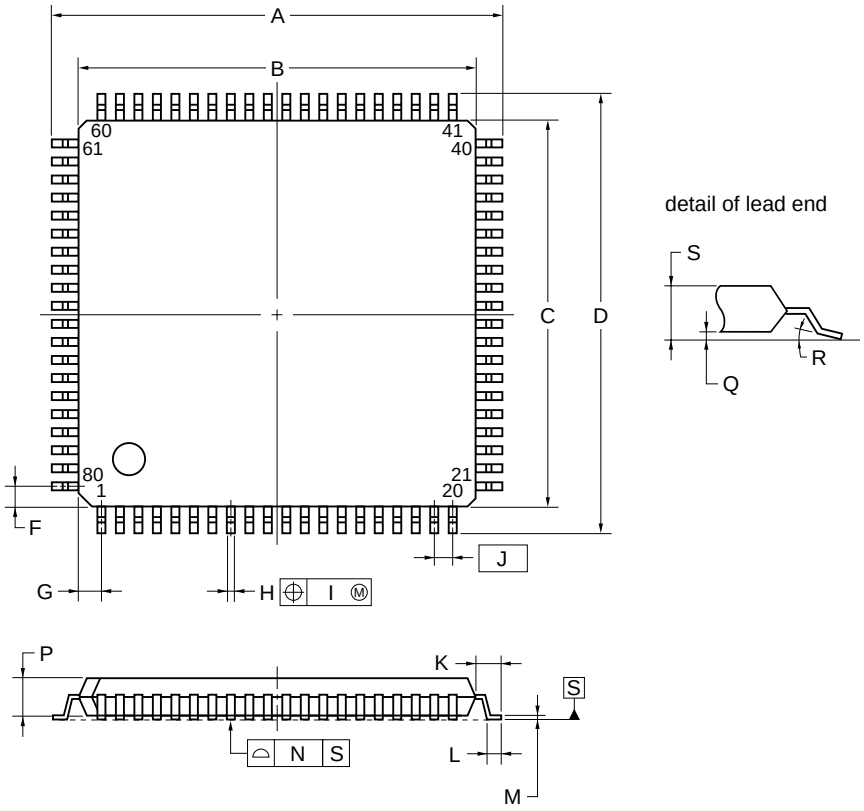
Note Example of external source circuit (when 1/2 bias)



R1 :1k to 10 kΩ (approx.)

11. PACKAGE DRAWING

80-PIN PLASTIC LQFP (14x14)



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.0±0.2
B	14.0±0.1
C	14.0±0.1
D	16.0±0.2
F	0.825
G	0.825
H	0.30±0.10
I	0.13
J	0.65 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.125^{+0.10}_{-0.05}$
N	0.10
P	1.4±0.1
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.7 MAX.

S80GC-65-7ET-3

12. RECOMMENDED SOLDERING CONDITIONS

The μPD16431A should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document Semiconductor Device Mounting Technology Manual(C10535E).

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

μPD16431AGC-7ET : 80-PIN PLASTIC LQFP (14 × 14)

Soldering Method	Soldering Conditions	Recommended Soldering Condition Symbol
Infrared reflow	Package peak temperature : 235°C, Time : 30 sec. MAX. (at 210 or higher), Count : 2 times or less. Exposure limit: 7 days Note (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature : 215°C, Time : 40 sec. MAX. (at 210 or higher), Count : 2 times or less. Exposure limit: 7 days Note (after that, prebake at 125°C for 10 hours).	VP15-107-2
Wave soldering	Solder bath temperature : 260°C MAX., Time : 10 sec. MAX., Count : once, Preheating temperature: 120°C MAX. (package surface temperature) Exposure limit: 7 days Note (after that, prebake at 125°C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 300°C MAX., Time: 3 seconds MAX. (per side of device)	–

Note After opening the dry pack, store it at 25°C ro less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except the partial heating).

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

REFERENCE DOCUMENTS

NEC Semiconductor Device Reliability/Quality Control System	(IEI-1212)
Semiconductor Device Mounting Technology Manual	(C10535E)