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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

μPD6450

12 LINE × 24 COLUMN ON-SCREEN CHARACTER DISPLAY CMOS LSI FOR VTR

DESCRIPTION

The μPD6450 is on-screen character display CMOS LSI which is combined with microcomputers and used for VTR and video disks to display program reserved information, chapter numbers, etc. on monitor screens.

Character format is 12 x 18 dots, and one character enables displaying numbers kanji and hiragana. Since this LSI has built-in video switches, video signals can be input and output by composite video signals, and video signals can be generated internally so that characters can be displayed with no external signals.

NEC provides two standard types — μPD6450CX-002 and μPD6450GT-102.

Using same characters, μPD6450CX-002 is 18-pin DIP and μPD6450GT-102 is a 20-pin SOP package.

FEATURES

- Number of displayed character : 12 lines 24 columns
- Kinds of character : 128 (ROM)
- Character size : 1 dot — 1H, 2H, 3H, or 4H
- Dot matrix : 12 x 18 dots — with no clearance between neighboring characters
- Blinking ratio : 1 : 1, 3 : 1, or 1 : 3
- Input/Output of image signal : Composite video signal
- Background : No background, black fringe, black square background, or black solid background
- Internal video signals : Characters can be displayed on internal simplified video signal (white, black, red, green or blue) by commands. Internal video signal is noninterlaced video signal.
- Mask pulse : Vertical direction for each row (This pulse is available with mask code option.)
- Character signal output : It is possible to output only character signal will mix with video signal. (This function is available with mask code option.)
- Interface with microcomputer : 8-bit serial input format with BUSY signal
- Power supply : +5 V single power supply
- Structure : Low-power-consumption CMOS

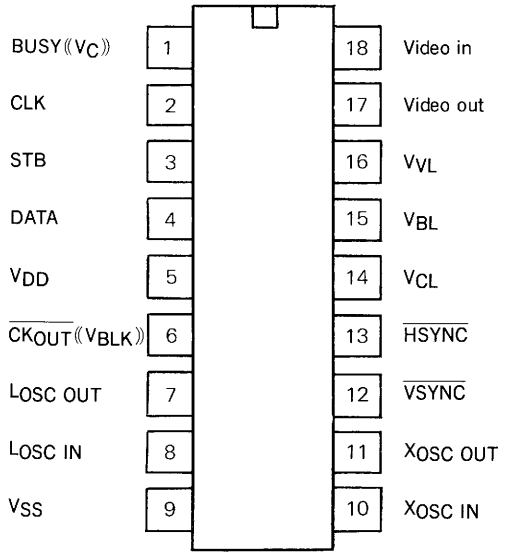
ORDERING INFORMATION

PART NUMBER	PACKAGE
μPD6450CX-002	18-pin plastic DIP (300 mil)
μPD6450GT-102	20-pin plastic SOP (375 mil)

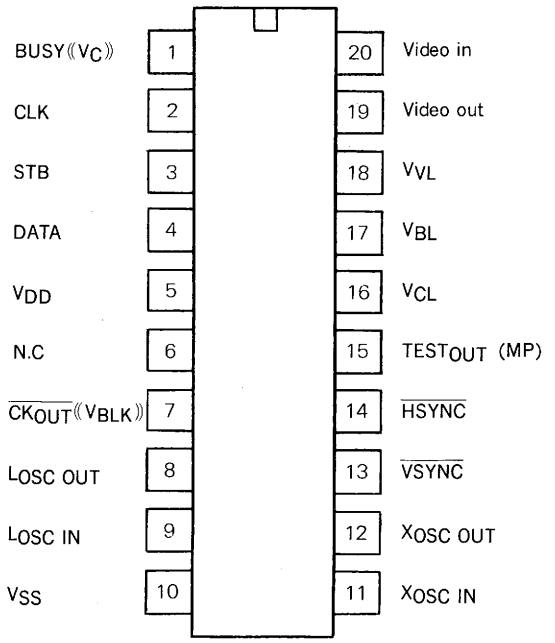
Document No. IC-2320A
(O.D.No. IC-7748)
Date Published March 1990 M
Printed in Japan

CONNECTION DIAGRAM (Top View)

(1) μPD6450CX-002



(2) μPD6450GT-102



Note: This single bracket shows terminal arrangement for the mask code option when terminal 15 of μPD6450GT-xxx is used for mask pulse. And this double bracket shows terminals arrangement for the mask code option when terminal 1 is used for character signal output, terminal 6 of μPD6450CX-xxx and terminal 7 of μPD6450GT-xxx are used for blanking signal output.
It is possible to select 3 ways of mask code option with μPD6450CX and 4 ways of mask code option with μPD6450GT and select one way at the following table.

Mask Code Option Selection Table

	Combination of mask code option	Selection posibility	Note
μPD6450CX	Non mask pulse function and BUSY signal output	○	The functions are similar to standard type. (terminal 1 : BUSY, terminal 6 : $\overline{CK_{OUT}}$)
	Mask pulse function and BUSY signal output	X	—
	Non mask pulse function and BUSY signal output	○	All character signal and all blanking signal are outed at V_C (terminal 1) and V_{BLK} (terminal 6).
	Mask pulse function and BUSY signal output	○	Character signal and blanking signal of lines without mask pulse are outed at V_C (terminal 1) and V_{BLK} (terminal 6).
μPD6450GT	Non mask pulse function and BUSY signal output	○	The functions are similar to standard type. (terminal 1 : BUSY, terminal 7 : CK_{OUT}, terminal 15 : TEST OUT)
	Mask pulse function and BUSY signal output	○	Mask pulse output : terminal 15 (terminal 1 : BUSY, terminal 7 : $\overline{CK_{OUT}}$)
	Non mask pulse function and BUSY signal outut	○	All character signal and all blanking signal are outed at V_C (terminal 1) and V_{BLK} (terminal 7, terminal 15 : TEST OUT)
	Mask pulse function and BUSY signal output	○	Character signal and blanking signal of line without mask pulse are outed at V_C (terminal 1) and V_{BLK} (terminal 7). (mask pulse output : terminal 15)

Note: As using mask pulse function at μPD6450CX, this product doesn't have mask pulse output terminal. So in this case, please use mask pulse function and character signal output function at same time.

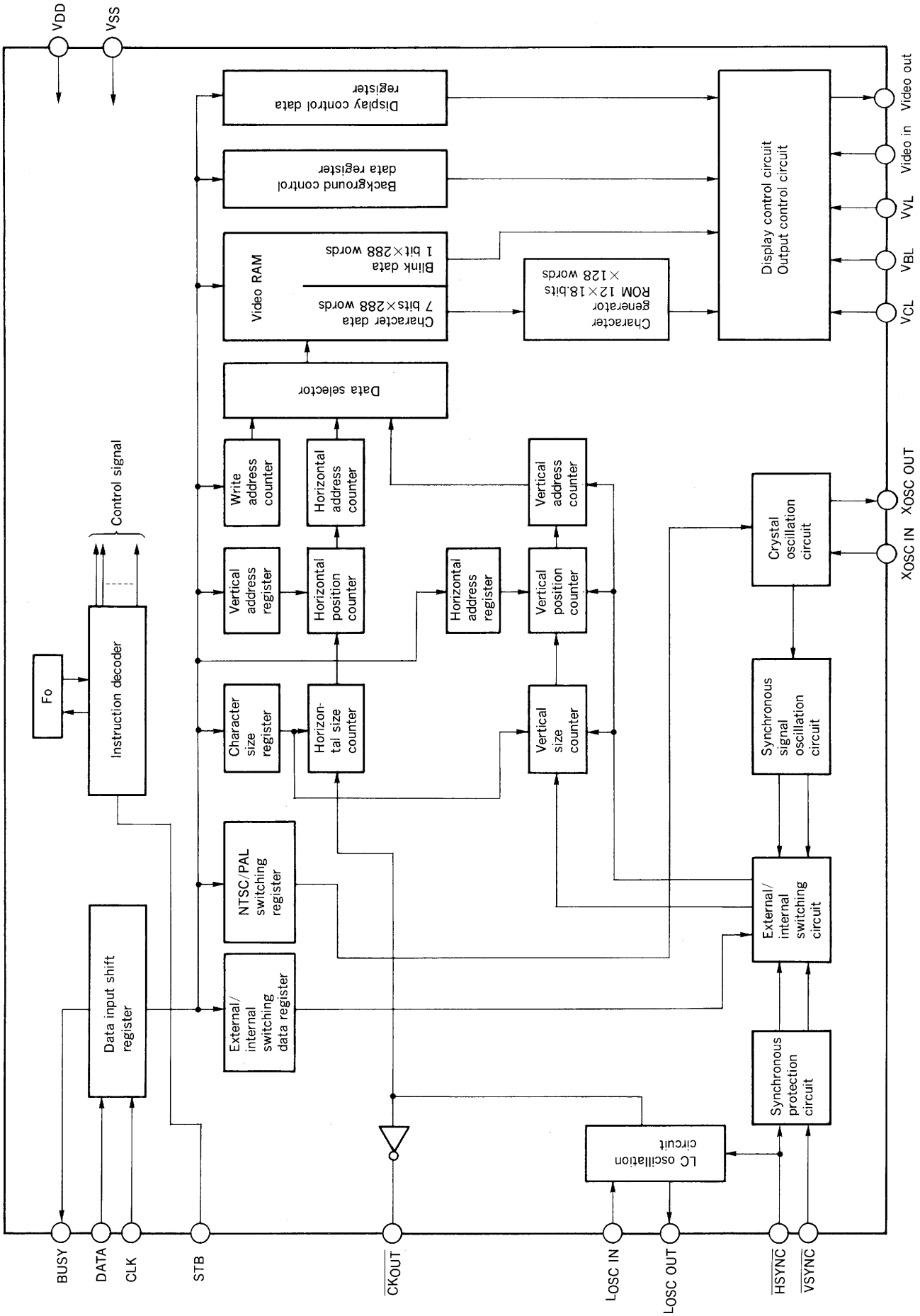
PIN DESCRIPTION

SYMBOL	PIN NAME	FUNCTION
V_{DD}	Power Supply Terminal	Supplies power (+5 V)
V_{SS}	Ground Terminal	Connected to system ground.
DATA	Serial Data Input Terminal	Input terminal for control data. Data is read synchronized with clock pulse at CLK terminal.
CLK	Clock Input Terminal	Input terminal for data reading clock. Data at data terminal is read at rising edge clock pulse.
STB	Strobe Input Terminal	Terminal for strobe input after serial data input. Eight-bit data is read at rising edge of pulse applied to STB terminal. If the eight-bit data is character data, the data address is incremented by 1 at the falling edge of pulse.
BUSY	BUSY Signal Output Terminal	This terminal tells the microcomputer whether or not STB input is ready. Input is feasible at low level.
V_C Note 1)	Character Signal Output Terminal	Output terminal for character signal of rows without mask pulse. Output is feasible at high level.
$\overline{HSYNC}$	Horizontal Synchronization Signal Input Terminal	This is input terminal for horizontal synchronization signal. Oscillation occurs when $\overline{HSYNC}$ is at high level and oscillation synchronizes with the rising edge of $\overline{HSYNC}$. Data is input at Active Low.
$\overline{VSYNC}$	Vertical Synchronization Signal Input Terminal	Input terminal for vertical synchronization signal. Data should be input at Active Low.
$L_{OSC\ IN}$ $L_{OSC\ OUT}$	LC Oscillation Terminal	Connection terminal for coil and capacitor of dot clock generating oscillator.
$X_{OSC\ IN}$ $X_{OSC\ OUT}$	Crystal Oscillation Terminal	Crystal connecting terminal for Oscillator which generates internal synchronization signals.
$V_{video\ in}$	Video Signal Input Terminal	Input terminal for composite video signal. Data is to be input when the synchronization signal is negative and the image signal is positive.
$V_{video\ out}$	Video Signal Output Terminal	Output terminal for composite video signal mixing with character signal.
V_{CL}	Character Level Adjusting Terminal	Input terminal for adjusting character signal level (white level).
V_{BL}	Background Level Adjusting Terminal	Input terminal for adjusting background signal level (black level)
V_{VL}	Simplified Video Signal Level Adjusting Terminal	Input terminal for adjusting signal level of video signal (sync tip level) which is produced in internal mode.
CK_{OUT}	Clock Out Terminal	Inverted OSC OUT terminal. This terminal is used for checking oscillation frequency. This terminal is a test input terminal as well, so it should be used after format reset.
V_{BLK} Note 1)	Blanking Signal Output Terminal	Output terminal for the blanking signal to cut the video signal of rows without mask pulse. Output is feasible at high level.
$TEST_{OUT}$ Note 2)	Test Out Terminal	Test out terminal. (This terminal is usually open.)

Note 1 : In case of selected character signal output function in mask code option.

Note 2 : This terminals can be covered to mask pulse output terminal in mask code option only for μPD6450GT. The μPD6450CX-002 and μPD6450GT-102 don't use a mask pulse and character signal output, and terminal 15 of μPD6450GT-102 is "TEST OUT." This terminal is usually open.

BLOCK DIAGRAM



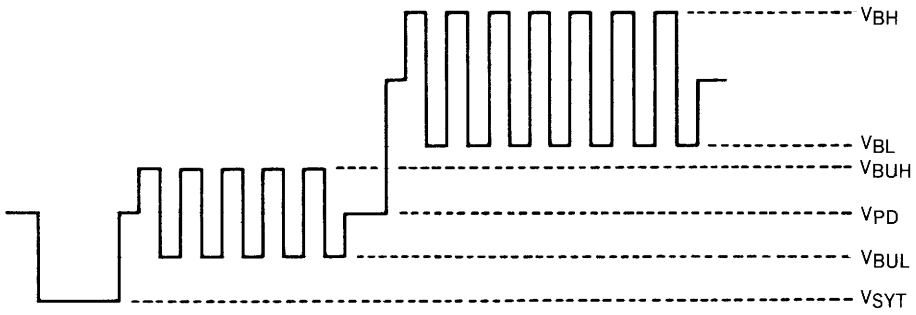
ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	$V_{DD}-V_{SS}$	7	V
Input Voltage	V_{IN}	$V_{DD}+0.3 > V_{IN} > V_{SS}-0.3$	V
Output Voltage	V_{OUT}	$V_{DD}+0.3 > V_{OUT} > V_{SS}-0.3$	V
Operation Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C
Output Current	I_D	±5	mA

RECOMMENDED OPERATION RANGE

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	$V_{DD}-V_{SS}$	4.5	5.0	5.5	V
LC Oscillation Frequency	f_{osc}	4	7	10	MNz
Control Input High-level Voltage	V_{IH}	2.4			V
Control Input Low-level Voltage	V_{IL}			0.8	V
Synchronization Signal Input High-level Voltage	V_{IH}	2.4			V
Synchronization Signal Input Low-level Voltage	V_{IL}			0.8	V
External Vido Signal Input Voltage	V_i	0		V_{DD}	V
Character Signal Level Set Voltage	V_{CL}	0		V_{DD}	V
Background Signal Level Set Voltage	V_{BL}	0		V_{DD}	V
Internal Video Signal Level Set Voltage	V_{VL}	2.5		V_{DD}	V

INTERNAL SIMPLIFIED VIDEO SIGNAL



Type of Command

Control commands are eight-bit serial input types. Commands are executed by STB pulse input after serial input of eight-bit data. Before executing a program always issue a format reset command (format assignment command "FR = 1") to release the test mode.

COMMAND LIST FOR μPD6450

CONTENT	F_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display Character Data	0	0	C_6	C_5	C_4	C_3	C_2	C_1	C_0
Blink Data for Each Character	0	1	0	0	0	Blink	0	0	0
Character Display Line Address	0	1	0	0	1	AR_3	AR_2	AR_1	AR_0
Character Display Column Address	0	1	0	1	AC_4	AC_3	AC_2	AC_1	AC_0
Color Assignment for Background/ Internal Video Signal	0	1	1	0	BS_4	BS_3	R_V	G_V	B_V
Display ON/OFF, Blink, LC Oscillation Control	0	1	1	1	0	DO	BL_2	BL_1	L_{OSC}
NTSC/PAL Switching, External/Internal Video Switching, Crystal Oscillation Control	0	1	1	1	1	0	N/P	Ex/In	X_{OSC}
Format Assignment	X	1	1	1	1	1	1	F_0	FR
Display Position Vertical Address	1	0	1	0	V_4	V_3	V_2	V_1	V_0
Display Position Horizontal Address	1	1	1	0	H_4	H_3	H_2	H_1	H_0
Character Size Assignment Note	1	1	0	S_5	S_4	AR_3	AR_2	AR_1	AR_0
Test Mode Set	1	1	1	1	0	T_3	T_2	T_1	T_0

Note: Change of command because of mask pulse.
In case of selecting mask pulse function in mask code option at μPD6450CX/GT, the command of character size is changed as shown below and this command is used some command with the command of mask pulse.
(The kind of character sizes is changed from 4 to 2.)
As using mask pulse function at μPD6450CX, this product doesn't have mask pulse output terminal. So in this case, please use mask pulse function and character signal output function at same time.

CONTENT	F_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Character Size/Mask Pulse Assignment	1	1	0	MP	S_4	AR_3	AR_2	AR_1	AR_0

Format Assignment and Format Reset (Test Mode Release)

Although commands for μPD6450 consist of nine bits, they are separated into two banks because serial interface shift register uses eight bits. Switching of banks is made by bit 1 (F_0) of the format assignment command.

Command for bank '0' (F_0 = 0)

- Displayed character data
- Blink data for each character
- Character display line address
- Character display column address
- Color assignment for background/internal video signal
- Display ON/OFF, Blink, LC Oscillation Control
- NTSC/PAL Switching, External/Internal Video Switching, Crystal Oscillation Control

Command for bank '1' (F_0 = 1)

- Display position vertical address
- Display position horizontal address
- Character size assignment
- Test mode set

Format Reset (Test Mode Release)

Setting bit 0 (F_R) of format assignment command to "1" releases the test command mode and resets the following command. Since the test command mode stops normal commands from being received, always perform format reset to release test command mode before program execution.

Reset Command

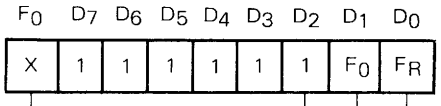
Size register ($AR_{0\text{-}3}$) on every line is set to "(S_5, S_4) = (0, 0)."
(Minimum size is assigned on every line.)

In case of selecting mask pulse function in mask code option at μPD6450CX/GT, size register ($AR_{0\text{-}3}$) is set to (S_4) = (0) on every lines and no mask pulse is output on any line (MP = (0)).

To release the test command mode without resetting the command above, use the test command mode release statement (F_0, D_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0) = (1, 1, 1, 1, 0, 0, 0, 0, 0).

Note: As using mask pulse function at μPD6450CX, this product doesn't have mask pulse output terminal. So in this case, please use mask pulse function and character signal output function at same time.

Format Assignment Command

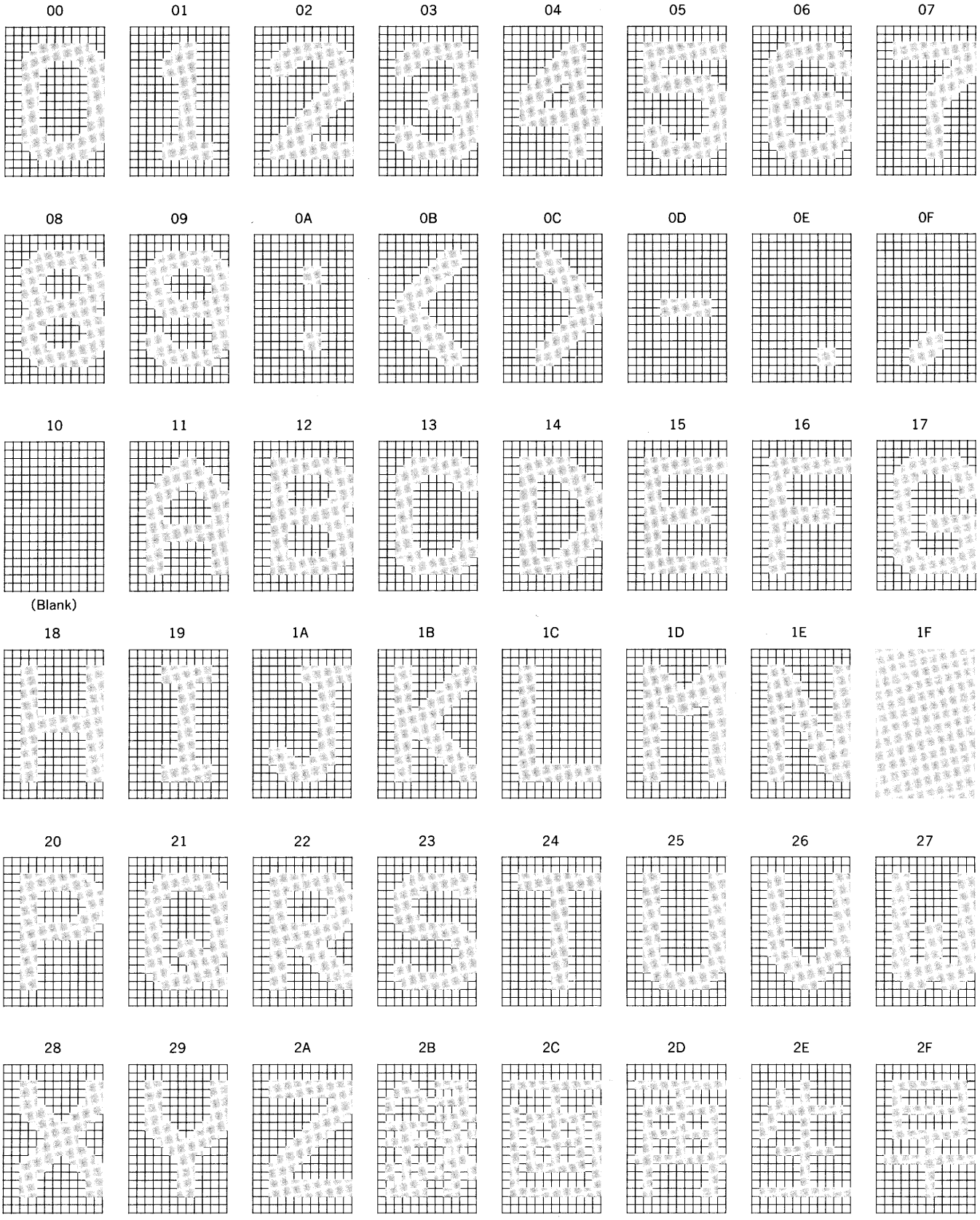


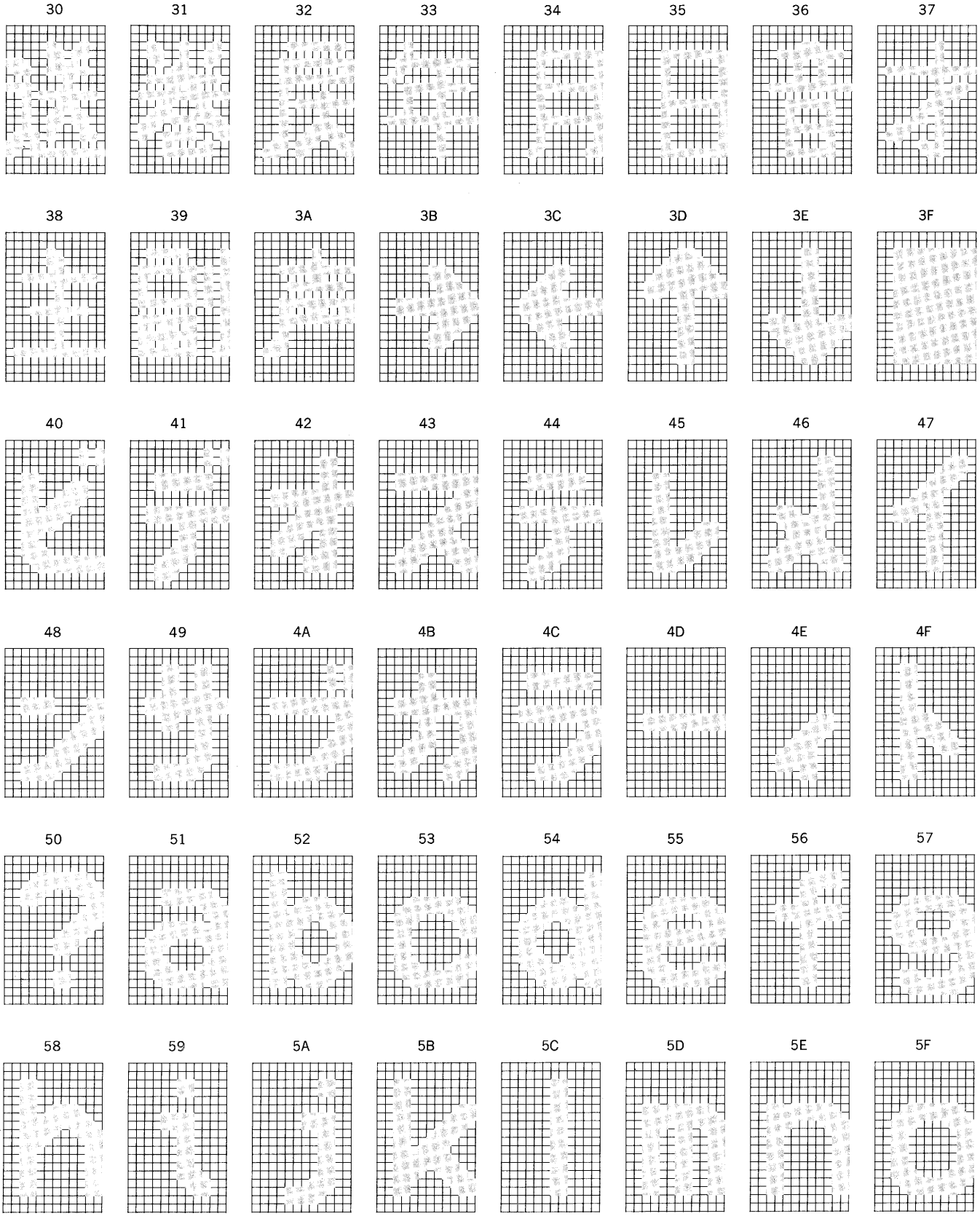
Format reset bit (Not latched)	
F_R	Function
1	Test mode is released and character size assignment command is reset.

BANK switching bit	
F_0	Function
0	Every command in Bank-0 can be used.
1	Every command in Bank-1 can be used.

These indicate that this command is the format assignment command.

Character Patterns of μPD6450CX-002 & 6450GT-102

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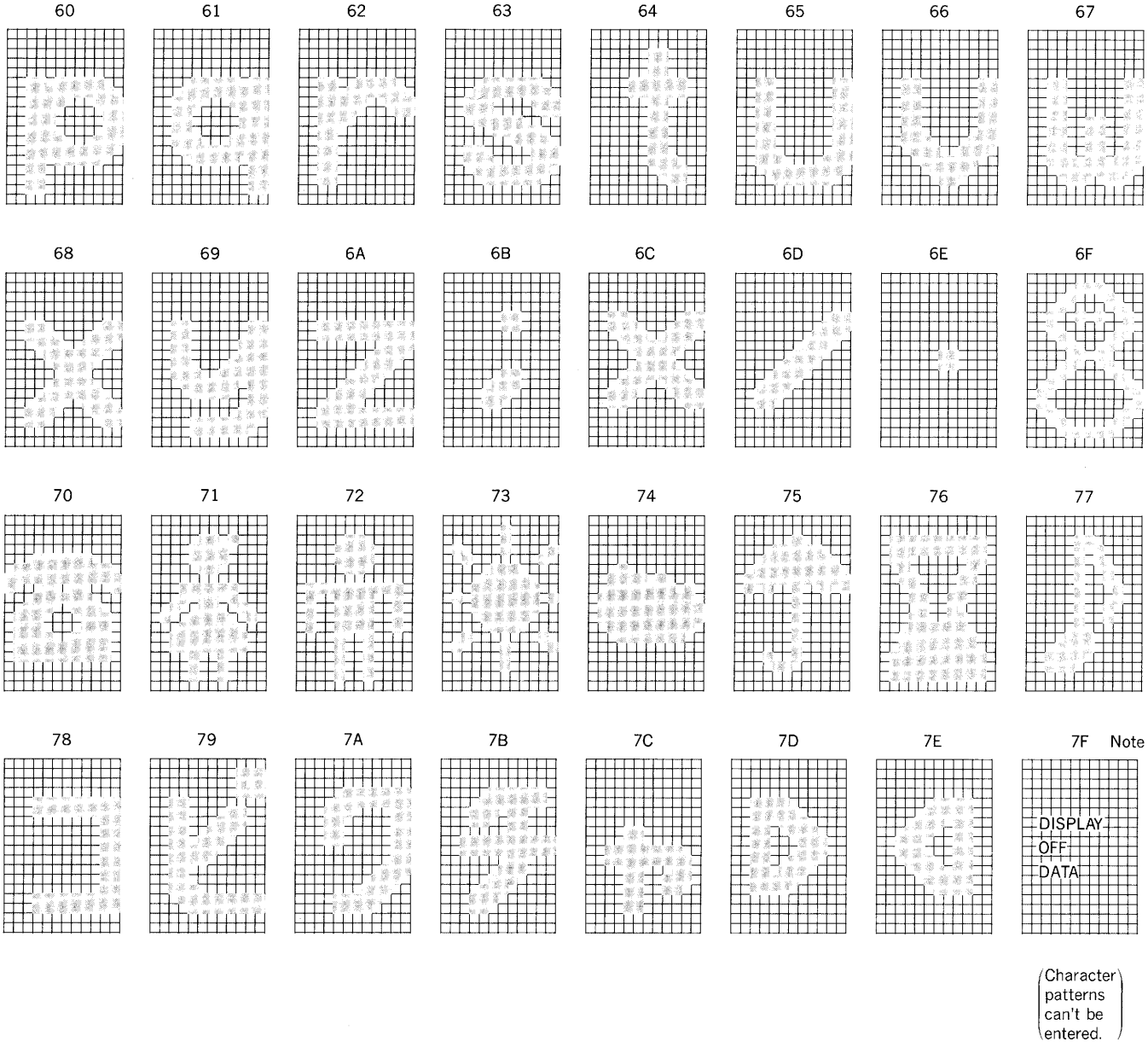

Note: In black block background and total black background mode, blank data (10H) generates background but no characters. DISPLAY OFF DATA (7FH) doesn't generate background or characters. If no-background or black trimmed character background mode is selected, BLANK DATA (10H) and DISPLAY OFF DATA (7FH) don't generate background or characters.

Character Display

There 12 lines by 24 columns of characters displayed (288 characters in all) as follows:

AC4, AC3, AC2, AC1, AC0	00000	00001	00010	00011	00100	00101	00110	00111	01000	01001	01010	01011	01100	01101	01110	01111	10000	10001	10010	10011	10100	10101	10110	10111
AR3 AR2 AR1 AR0 0000																								
0001																								
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0111																								
1000																								
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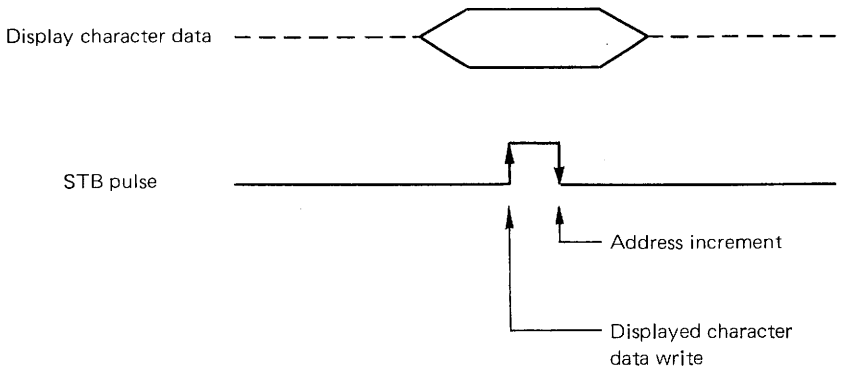
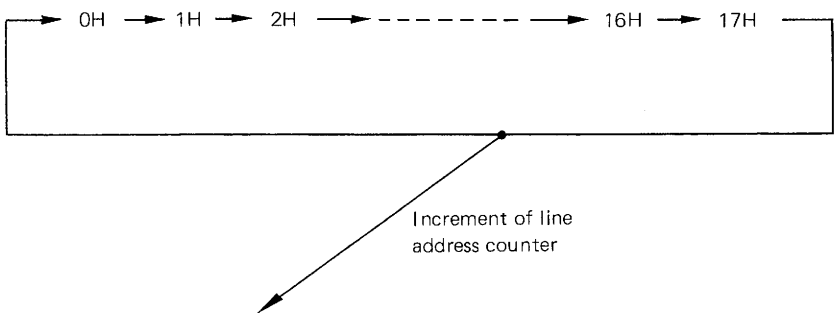
Writing Displayed Character Data and Blink Data for Each Character

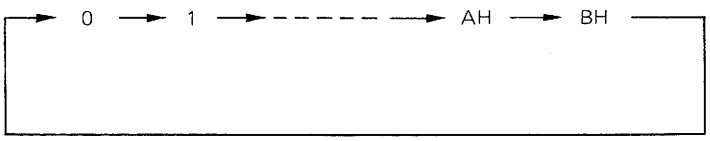
The data write address can be set directly into the address counter by the character display line address command and character display column address command. After setting write address, feed blink data for each character with the blink data command. Blink data is stored by character in an internal register. After that, input displayed character data with the displayed character data command. Blink data and displayed character data which has been stored in an internal register is written in video RAM at the rise of the STB pulse input at the end of displayed character data command. The write address is incremented as follows at rising edge of the STB pulse generated when displayed character data is input. To continue to write displayed character data without changing blink data, input the displayed character data command.



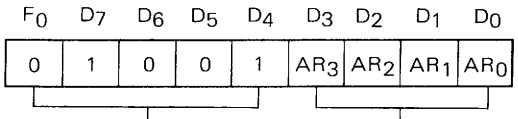
Column address counter $AC_4, AC_3, AC_2, AC_1, AC_0$



Line address counter AR_3, AR_2, AR_1, AR_0



Character Display Line Address Command

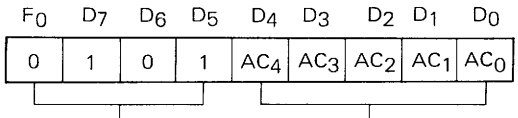


Line address assignment bit				
AR_3	AR_2	AR_1	AR_0	Function
0	0	0	0	The first line is set.
0	0	0	1	The second line is set.
⌇		⌇		⌇
1	0	1	1	The 12th line is set.

Enter only addresses OH — BH.

These show that this command is the character display line address command.

Character Display Column Address Command

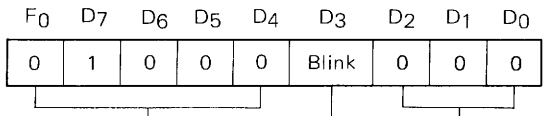


Column address assignment bit					
AC_4	AC_3	AC_2	AC_1	AC_0	Function
0	0	0	0	0	The first column is set.
0	0	0	0	1	The second column is set.
⌇		⌇		⌇	⌇
1	0	1	1	1	The 24th column is set.

Set only address 0H — 17H.

These show that this command is the character display column address command.

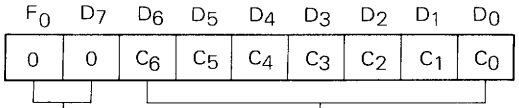
Blink Data Command for Each Character



Blink assignment bit for each character	
Blink	Function
0	No blinking
1	Blinking

These show that this command is the blink data command according to character.

Displayed Character Data Command



Character assignment bit							
C_6	C_5	C_4	C_3	C_2	C_1	C_0	Function
0	0	0	0	0	0	0	Data of character code 00H is output.
0	0	0	0	0	0	1	Data of character code 01H is output.
			⌇				⌇
1	1	1	1	1	1	0	Data of character code 7EH is output.
1	1	1	1	1	1	1	Display OFF data.

These show that this command is the displayed character data command.

Turning Total Display ON or OFF

The display can be partially turned off with Blank data or display off data. The total display turned off with display ON/OFF, blink, and LC oscillation control commands. When display OFF is set with this command, characters and backgrounds are not output.

Character Blinking

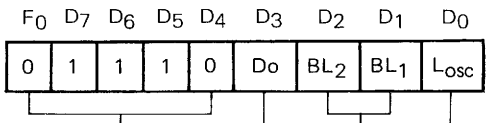
This IC enables blinking for each character with display ON/OFF, blink, and LC oscillation control commands. Blinking characters are determined with the character blink data command. The blinking period is about 1 second (64 times longer than 1 vertical cycle), and three blinking ratios (1 : 1, 3 : 1, and 1 : 3) are available.

LC Oscillation Control

Since this IC enables control of LC oscillation with display ON/OFF, blink, and LC oscillation control commands, oscillation can be suspended while characters aren't displayed, so that power can be saved. Since character output isn't reliable after suspension of oscillation, set the display ON/OFF control bit (Do) to "0" (display OFF).

Note: When display is ON, the oscillation synchronizes $\overline{H_{SYNC}}$, so the oscillation is stopping at the low level term of $\overline{H_{SYNC}}$. When display is OFF, the oscillation keeps on irrespective of $\overline{H_{SYNC}}$.

Display ON/OFF, Blink, and LC Oscillation Commands



LC oscillation control bit	
L_{osc}	Function
0	LC oscillation OFF
1	LC oscillation ON

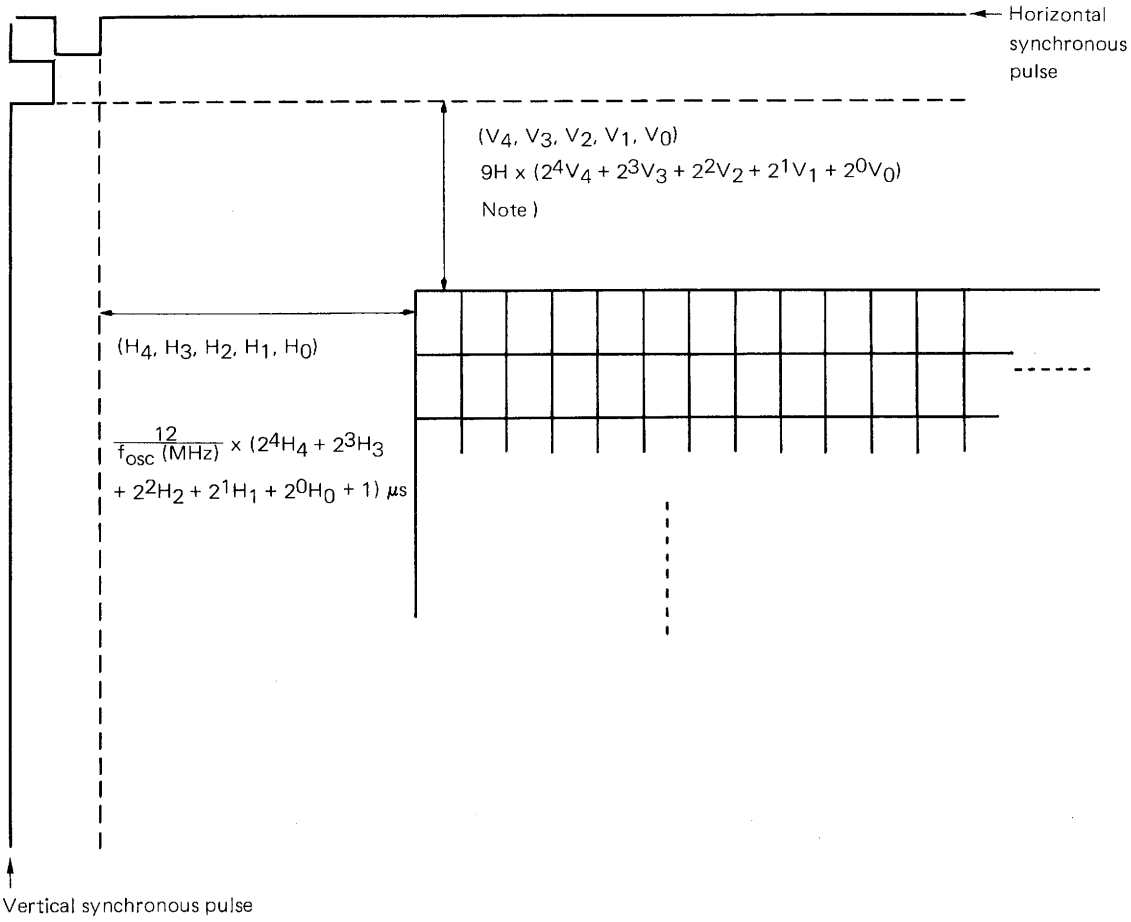
Blink control bit		
BL_2	BL_1	Function
0	0	Blink OFF
0	1	Blink ratio 1 (ON) : 3 (OFF)
1	0	Blink ratio 3 (ON) : 1 (OFF)
1	1	Blink ratio 1 (ON) : 1 (OFF)

Display ON/OFF control bit	
Do	Function
0	Display OFF
1	Display ON

These show that this command is the display ON/OFF, blink and LC oscillation command.

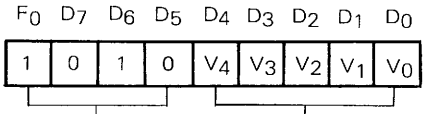
Character Display Address

Character display starting address is determined as follows with values assigned by both the display position vertical address command (F_0, D_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0) = (1, 0, 1, 1, V_4, V_3, V_2, V_1, V_0) and the display position horizontal address command (F_0, D_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0) = (1, 1, 1, 0, H_4, H_3, H_2, H_1, H_0).



Note: Vertical address counter is incremented by the leading edge of the horizontal synchronous pulse.

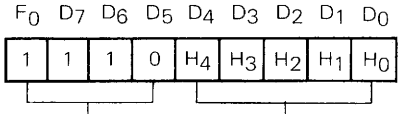
Assignment Command for Display Position Vertical Address



Vertical address assignment bits					
V_4	V_3	V_2	V_1	V_0	Start address
0	0	0	0	0	From the trailing edge of the vertical synchronous pulse 9 x 0H
0	0	0	0	1	From the trailing edge of the vertical synchronous pulse 9 x 1H
⋮					⋮
1	1	1	1	1	From the trailing edge of the vertical synchronous pulse 9 x 31H

These show the this command is the assignment command for the display position address.

Assignment Command for Display Position Horizontal Address



Horizontal address assignment bits					
H_4	H_3	H_2	H_1	H_0	Start address
0	0	0	0	0	From the trailing edge of the horizontal synchronous pulse $12/f_{osc}$(MHz) x 1 [μs]
0	0	0	0	1	From the trailing edge of the horizontal synchronous pulse $12/f_{osc}$(MHz) x 2 [μs]
⋮					⋮
1	1	1	1	1	From the trailing edge of the horizontal synchronous pulse $12/f_{osc}$(MHz) x 32 [μs]

These show that this command is the assignment command for the display position horizontal address.

Assignment of Character Size

Character size for each line can be selected from 1H, 2H, 3H or 4H of 1 dot. Line and character size is assigned with the character size assignment command. Note that there are two character sizes (1H or 2H of 1 dot) when the mask pulse function is selected in mask code option

Character Size Assignment Command

F_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	S_5	S_4	AR_3	AR_2	AR_1	AR_0

Row address selection bit

AR_3	AR_2	AR_1	AR_0	Function
0	0	0	0	The first line is selected.
0	0	0	1	The second line is selected.
		⟩		⟨
1	0	1	1	The 12th line is selected.

Enter only addresses OH to BH.

Character size specification bit

S_5	S_4	Character dot size		
0	0	Longitudinal	1 H	Lateral t_{dot}
0	1		2 H	$2 \cdot t_{dot}$
1	0		3 H	$3 \cdot t_{dot}$
1	1		4 H	$4 \cdot t_{dot}$

$$t_{dot} = \frac{1}{f_{osc}(MHz)}\ \mu s$$

These show that this command is the character size assignment command.

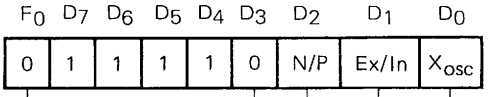
External/Internal Video Switching

When TV broadcasting signal can't be received or when unprerecorded tape is being played, synchronization is poor and mixing of the character signal results in poor character display. In such cases an internal video signal (raster signal of one color out of white, black, red, green and blue) should be generated with NTSC/PAL switching, external/internal video switching, or crystal oscillation control command, so that mixing of the character signal becomes possible. When an external video signal is used, crystal oscillation can be stopped by setting the crystal oscillation control bit (X_{osc}) to "0." This reduces power consumption. Internal video signal is noninterlaced video signal.

NTSC/PAL Switching

The internal video signal shown above can be used in both NTSC and PAL systems by changing NTSC/PAL switching bit with the NTSC/PAL switching, external/internal video switching, or crystal oscillation control command and by changing the external X'tal (14.318 18 MHz for NTSC, 17.734 476 MHz for PAL).

External/Internal Video Switching, X'tal Oscillation Control Command



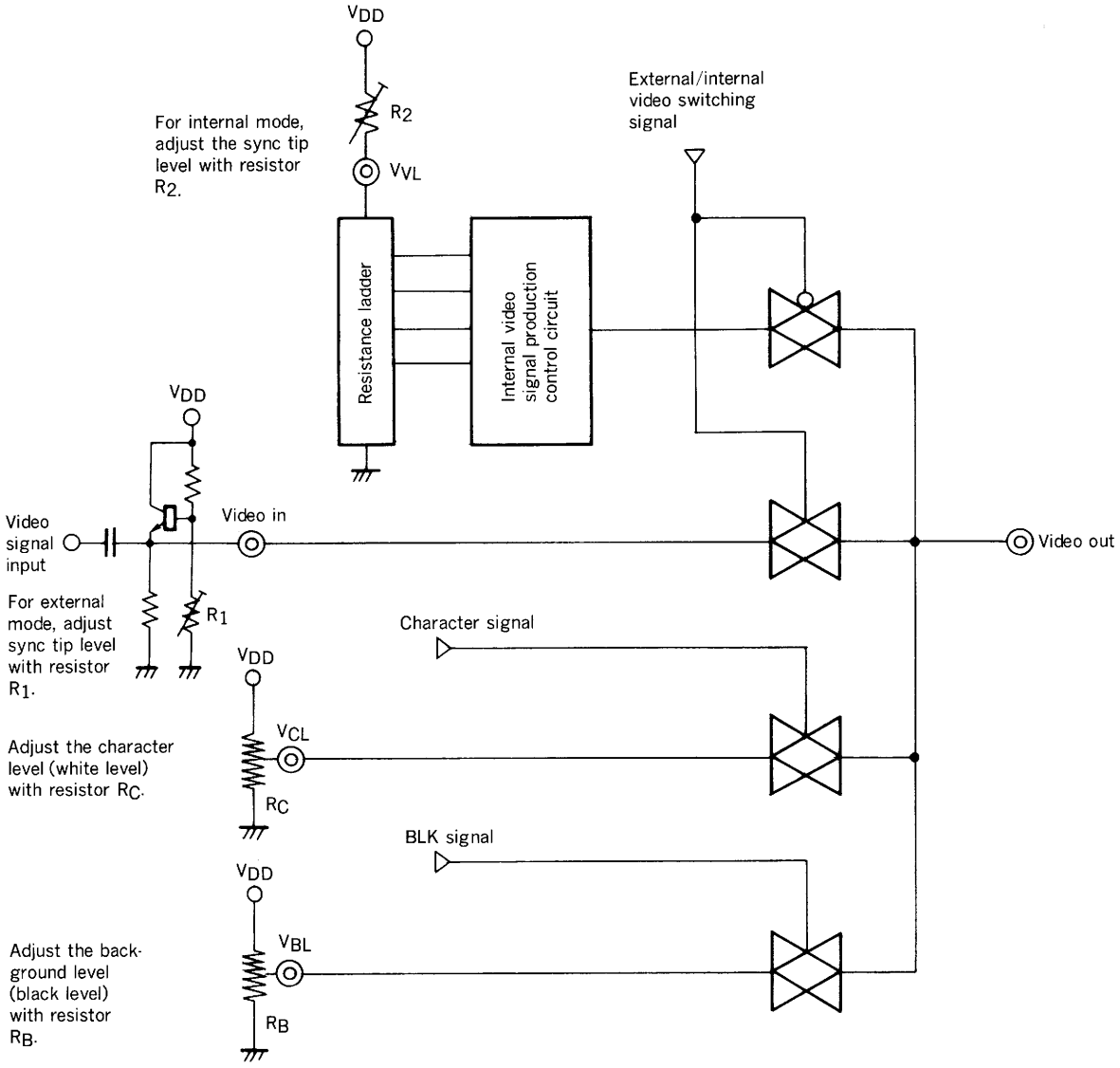
X'tal oscillation control bit	
X_{osc}	Function
0	X'tal oscillation OFF
1	X'tal oscillation ON

Externat/Internal video switching bit	
Ex/In	Function
0	External video signal mode
1	Internal video signal

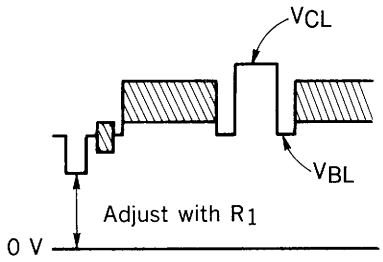
NTSC/PAL switching bit	
N/P	Function
0	NTSC mode
1	PAL mode

These show that this command is the NTSC/PAL switching, external/internal video switching, crystal oscillation control command.

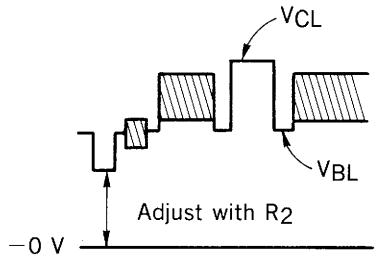
Adjusting Sync tip level, Character level, and Background level



In external mode



In internal mode



Note: Since there is no built-in pedestal clamp circuit for external video signal, connect direct current clamp circuit in front of "video in."

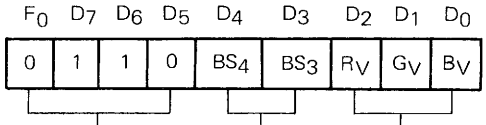
Background Assignment and Color Changing of Internal Video Signal

The background can be selected for each screen image from no-background, black-fringe, black square background, and black-solid background by the background internal video signal color assignment command. The background color is black.

When an internal video signal is used because of NTSC/PAL switching, external/internal video switching, and X'tal oscillation control command, raster color is switched by this background internal video signal color assignment command as well. In this case, white, black, red, green, or blue can be selected. Internal video signal is noninterlaced video signal.

- ○ No background . . . . . Character is totally surrounded by image or internal video signal.
- ○ Black fringe . . . . . Characters are trimmed with 1 dot-minimum character (1H/1 dot).
- ○ Black square background . . . . . The 12 line x 24 column block displaying characters has a black background.
- ○ Black solid background . . . . . Image signal or internal video signal is totally omitted and whole screen has a black background.

Background Internal Video Signal Color Assignment Command



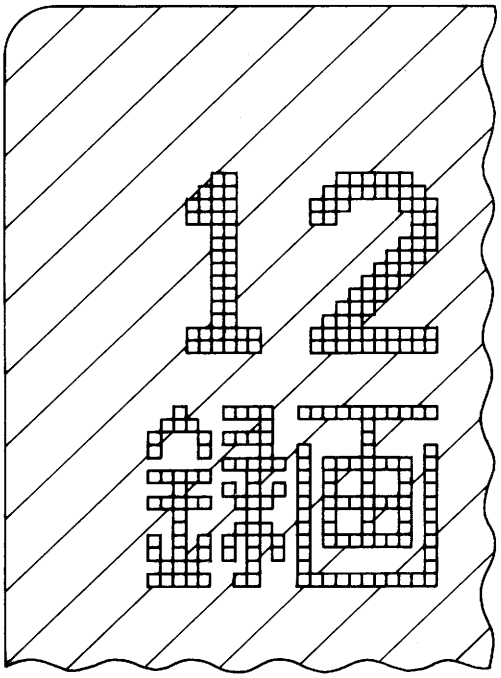
Internal simplified video signal color assignment bit			
R_V	G_V	B_V	Function
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Setting impossible
1	0	0	Red
1	0	1	Setting impossible
1	1	0	Setting impossible
1	1	1	White

Background assignment bit		
BS_4	BS_3	Function
0	0	No background
0	1	Black fringe
1	0	Black square background
1	1	Black solid background

These show that this command is the background/internal video signal color assignment command.

Display in Various Background Modes

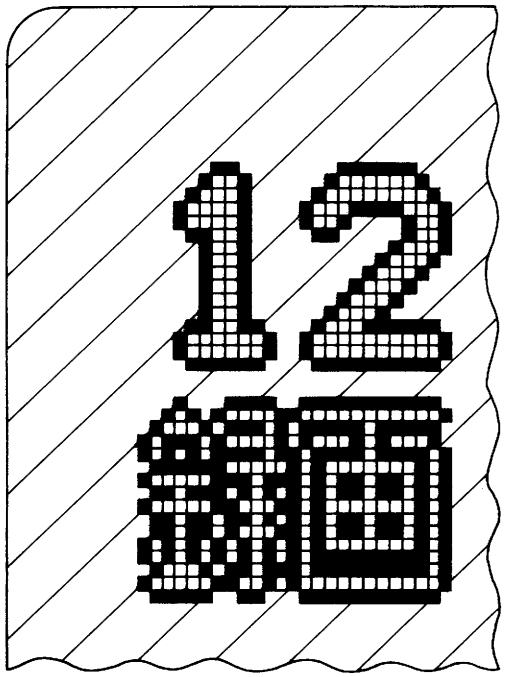
No background



White (character)

Color of image or internal video signal

Black fringe

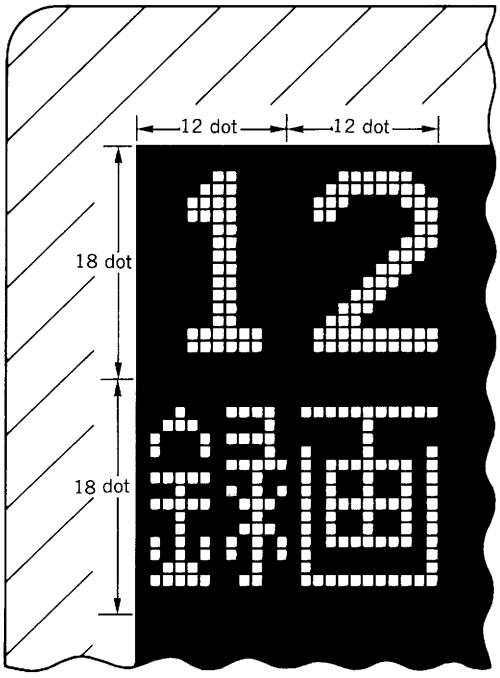


White (character)

Black (background)

Color of image or internal video signal

Black Square background

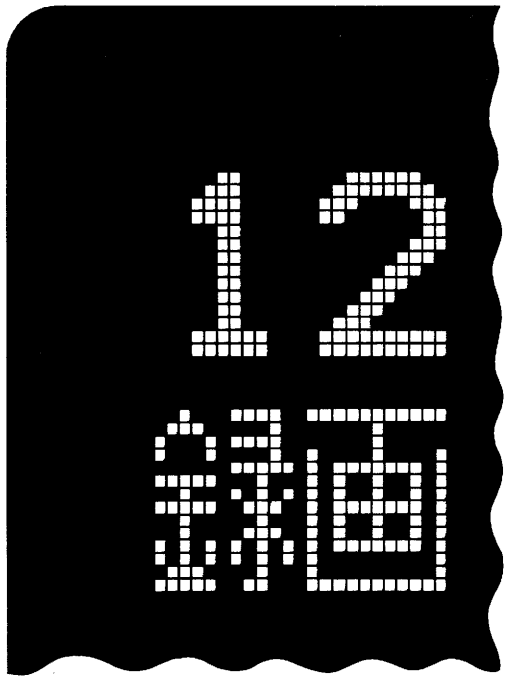


White (character)

Black (background)

Color of image or internal video signal

Black solid background

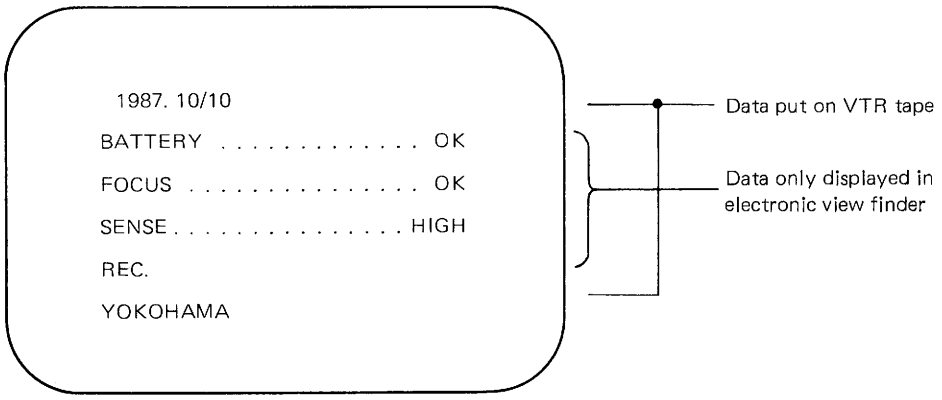


White (character)

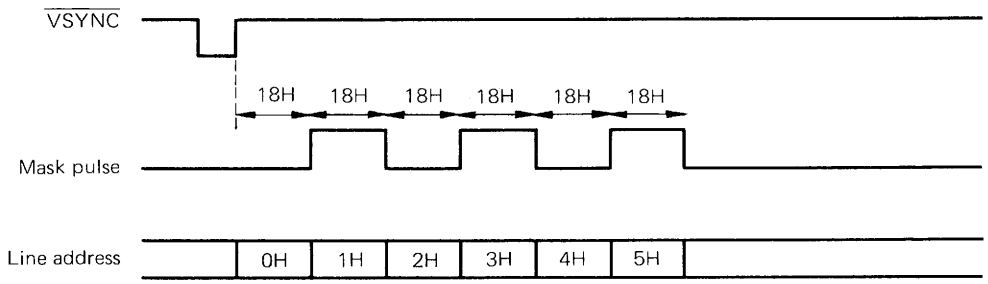
Black (background)

Mask Pulse Function

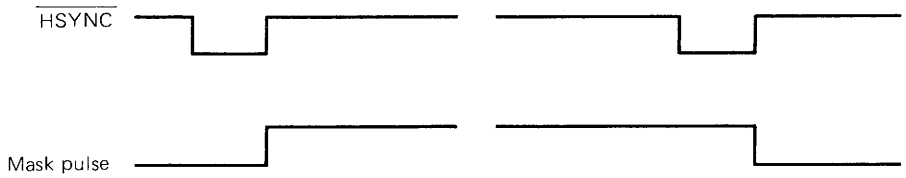
If an on-screen IC is used for VTR cameras, there are two types of data such as dates and titles to be put onto the VTR tapes and data such as battery, focus, sensitivity, and mode to be displayed in the electronic view finder. To sort these two data, this product can out character signal and blanking signal of lines without mask pulse (character signal output function: mask code option). And μPD6450GT is possible to use '15' terminal as mask pulse output terminal in mask code option.



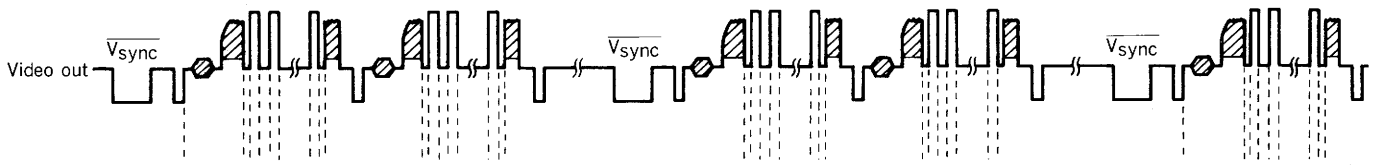
When the mask pulse is generated at line addresses 1H, 3H, and 5H with vertical address "0H" and with character size in all lines "2H/dot".



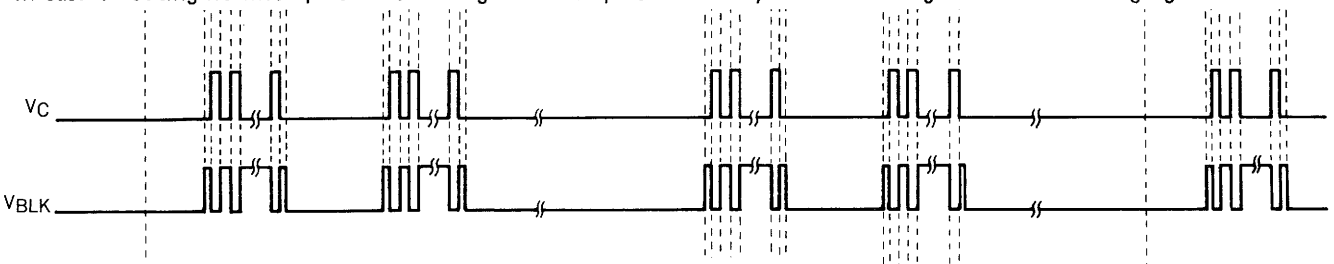
Leading and trailing edges of mask pulse are synchronized with trailing edge of $\overline{\text{HSYNC}}$.



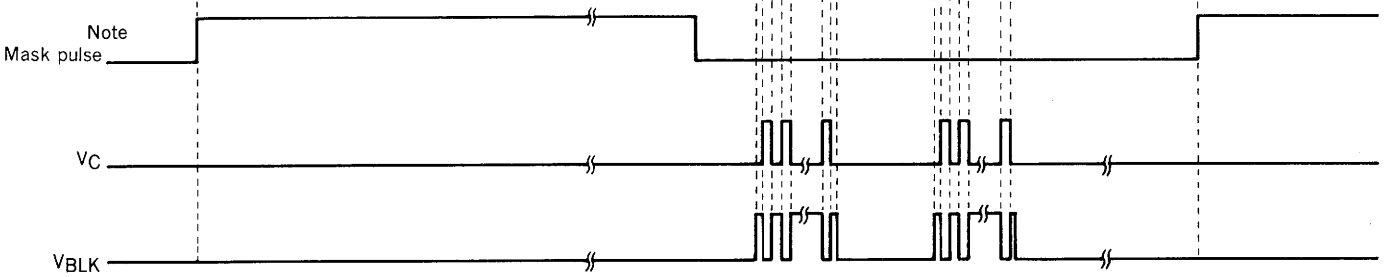
Outputs of V_C, V_{BLK} terminals, in case of selected character signal output function in mask code option.



(1) In case of outing no mask pulse or selecting non mask pulse function, all character signal and all blanking signal are outed.



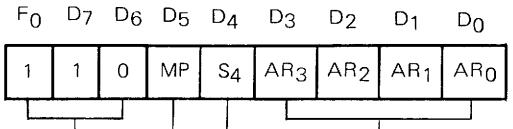
(2) In case of outing mask pulse signal.
Character signal and blanking signal of lines without mask pulse are outed.



Note: As using mask pulse function at μPD6450CX, this product doesn't have mask pulse output terminal. So in this case, please use mask pulse function and character signal output function at same time.

Mask Pulse, Character Size Assignment Command

(Used only when mask pulse function is selected for μPD6450GT by mask code option.)



Row address selection bit				
AR_3	AR_2	AR_1	AR_0	Function
0	0	0	0	The first line is selected.
0	0	0	1	The second line is selected.
⋮				⋮
1	0	1	1	The 12th line is selected.

Enter only addresses OH to BH.

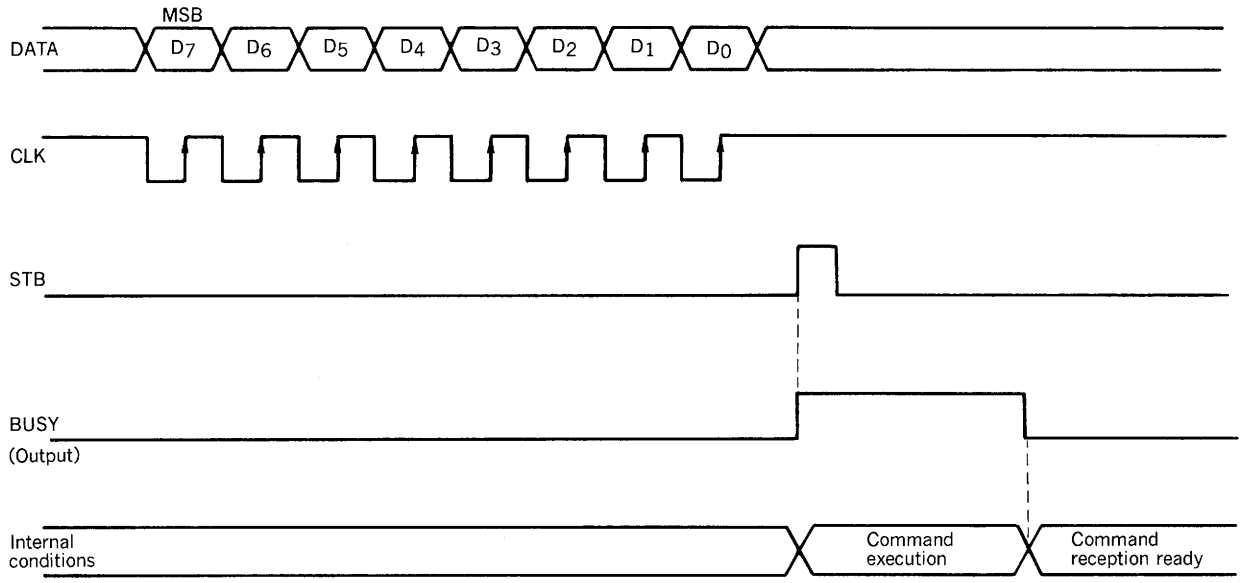
Character size assignment bit	
S_4	Character dot size
0	Longitudinal 1 H Lateral t_{dot}
1	2 H $2 \cdot t_{dot}$

$$t_{dot} = \frac{1}{f_{osc}(MHz)} \mu s$$

Mask pulse assignment bit	
MP	Function
0	No mask pulse is input.
1	Mask pulse is input.

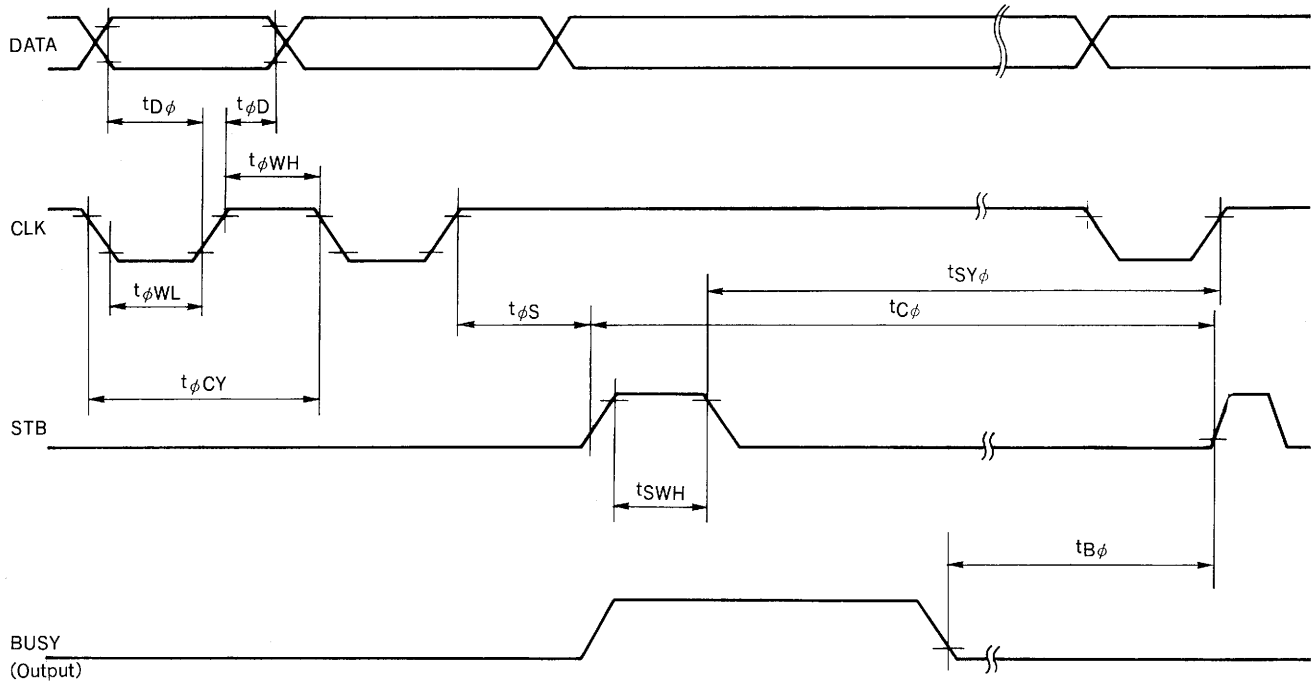
These show that this command is the mask pulse character size assignment command.

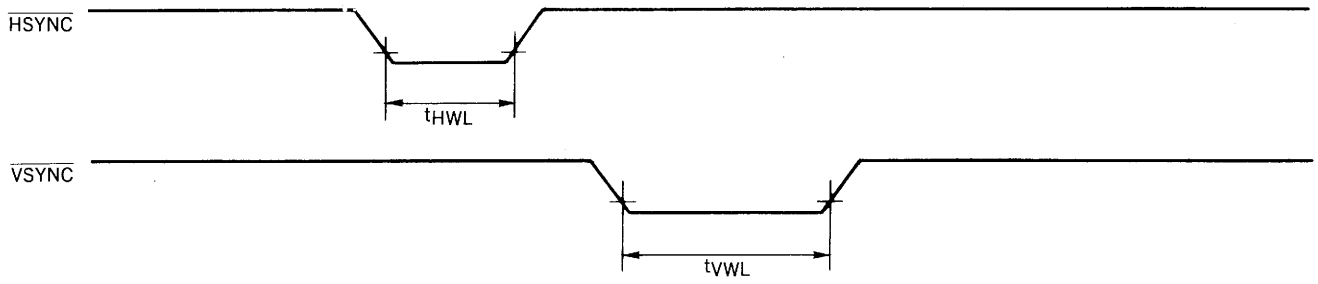
Note: μPD6450CX-002 and μPD6450GT-102 don't use the mask pulse and character signal output, and this command can't be used for it. As using mask pulse function at μPD6450CX, this product doesn't have mask pulse output terminal. So in this case, please use mask pulse function and character signal output function at same time.



For format data, a busy signal is generated after the internal conditions are completely determined. When writing data in VRAM, a busy signal is generated after the completion of writing in VRAM. When the VRAM write period extends into the horizontal retrace line period, the busy signal becomes longer than usual, so be careful. (This is because oscillation is suspended during the horizontal retrace line period, so writing in VRAM becomes impossible.)

Note: As the character signal output function is selected in mask code option, the 1st-terminal can't output the BUSY-signal. Please take care of the data transmitting and keep the recommended operation timing.





RECOMMENDED OPERATION TIMING (T_a = 25 °C, V_{DD} – V_{SS} = 5.0 V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Min. Setup Time	$t_{D\phi}$	200			ns	
Min. Hold Time	$t_{\phi D}$	200			ns	
Min. Clock Low-level Width	$t_{\phi WL}$	700			ns	
Min. Clock High-level Width	$t_{\phi WH}$	700			ns	
Min. Clock → Strobe Time	$t_{\phi S}$	400			ns	
Min. Strobe High-level Width	t_{SWH}	1			μs	
Clock Cycle	$t_{\phi CY}$	1.6			μs	
Min. Busy → Strobe Time	$t_{B\phi}$	100			ns	
Min. $\overline{\text{VSYNC}}$ Low-level Width	t_{VWL}	4			μs	
Min. $\overline{\text{HSYNC}}$ Low-level Width	t_{HWL}	4			μs	
Max. Strobe → Strobe Time	$t_{C\phi}$	14.4			μs	Displayed Character Data Command transmits at display ON with following conditions. Strobe high-level Width: 1 μs $\overline{H_{sync}}$ low-level Width: 5 μs f_{osc} : 6 MHz Character size : 2H/dot
		11.1			μs	Displayed Character Data Command transmits at display OFF with following conditions. Strobe high-level Width: 1 μs $\overline{H_{sync}}$ low level Width: 5 μs f_{osc}: 6 MHz Character size: 2H/dot
Min. Strobe → Clock Time	$t_{SY\phi}$	4			μs	Commands except Displayed Character Data Command transmit.

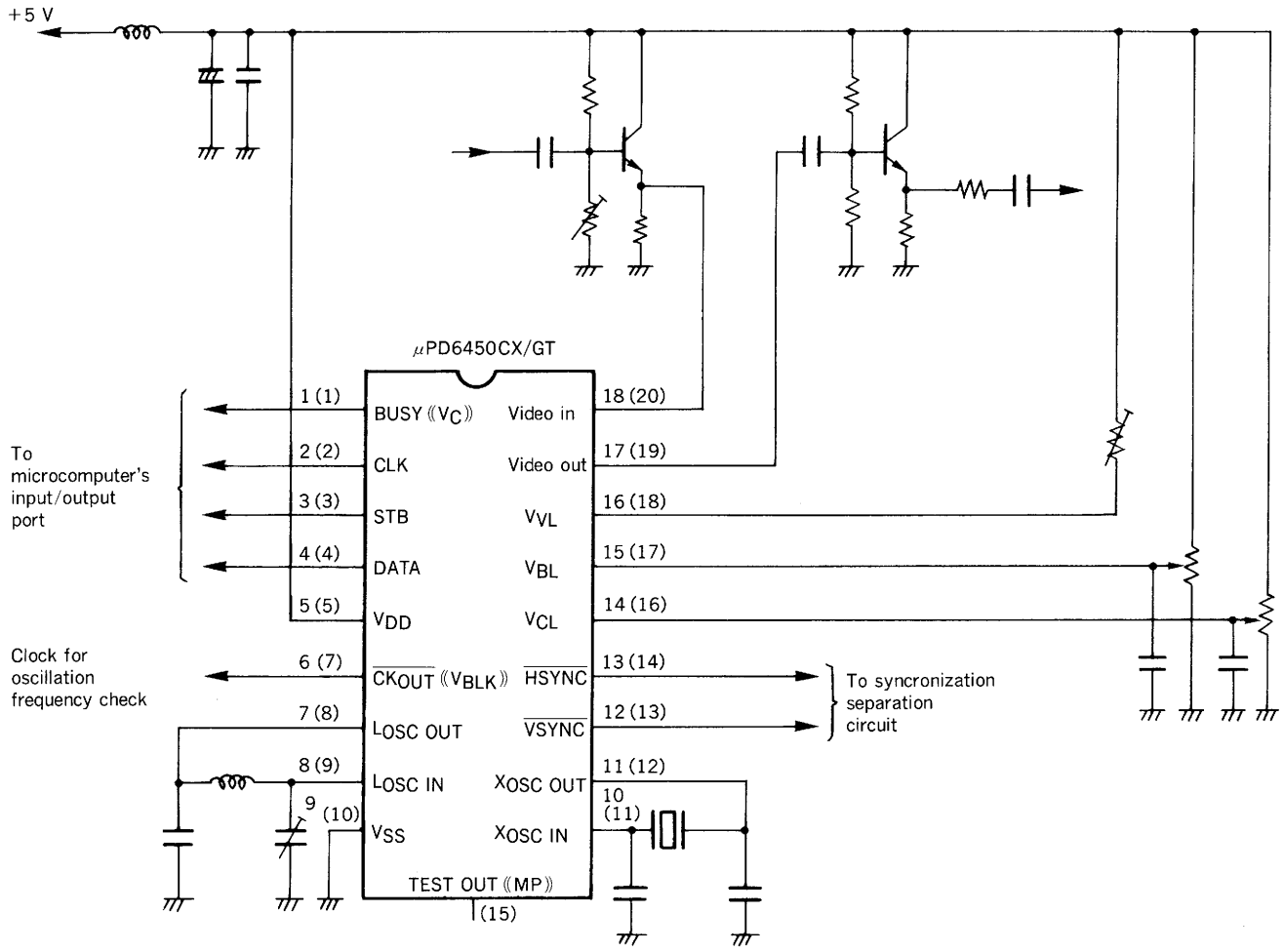
Note: The calculate expression of Max. Strobe → Strobe Time

$BUSY_{tc\phi} = STB_{High} + \overline{H_{sync}}$ Low + (25/f_{osc}) x (character size) + 100 ns

$\overline{H_{sync}}$: When the display is off : 15

When the display is off : 0

ADOPTED CIRCUIT

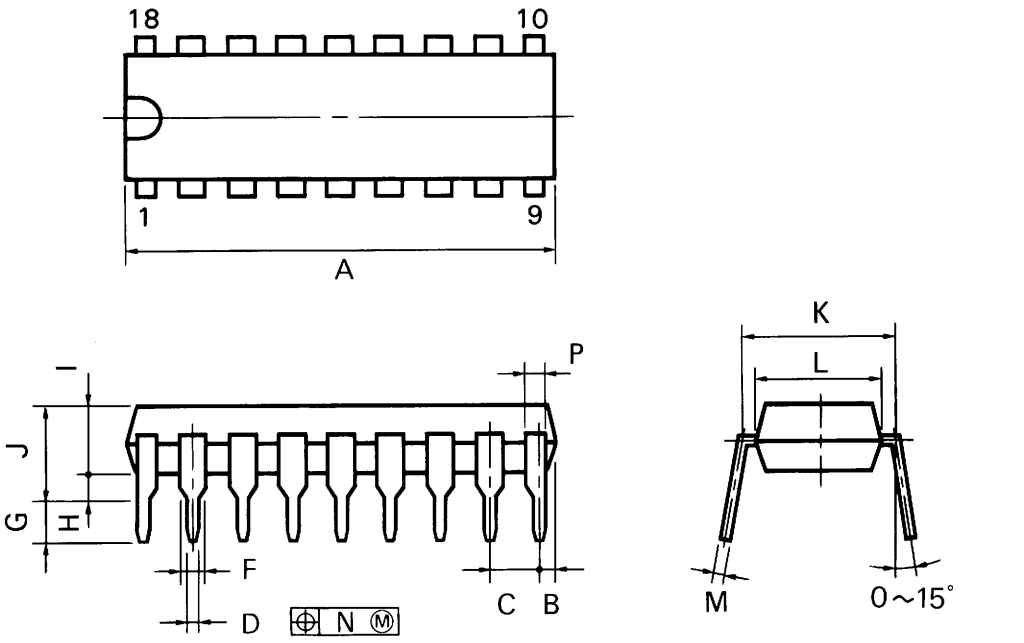


Numbers in single brackets are terminal numbers for μPD6450GT and don't connect 6th and 15th terminals for code products which don't use the mask pulse.

This double brackets shows terminal arrangement for the mask code option when selecting Mask pulse function and Character signal output function. Take care of connection of this terminals.

μPD6450CX-002

18PIN PLASTIC DIP (300 mil)



P18C-100-300B

NOTES

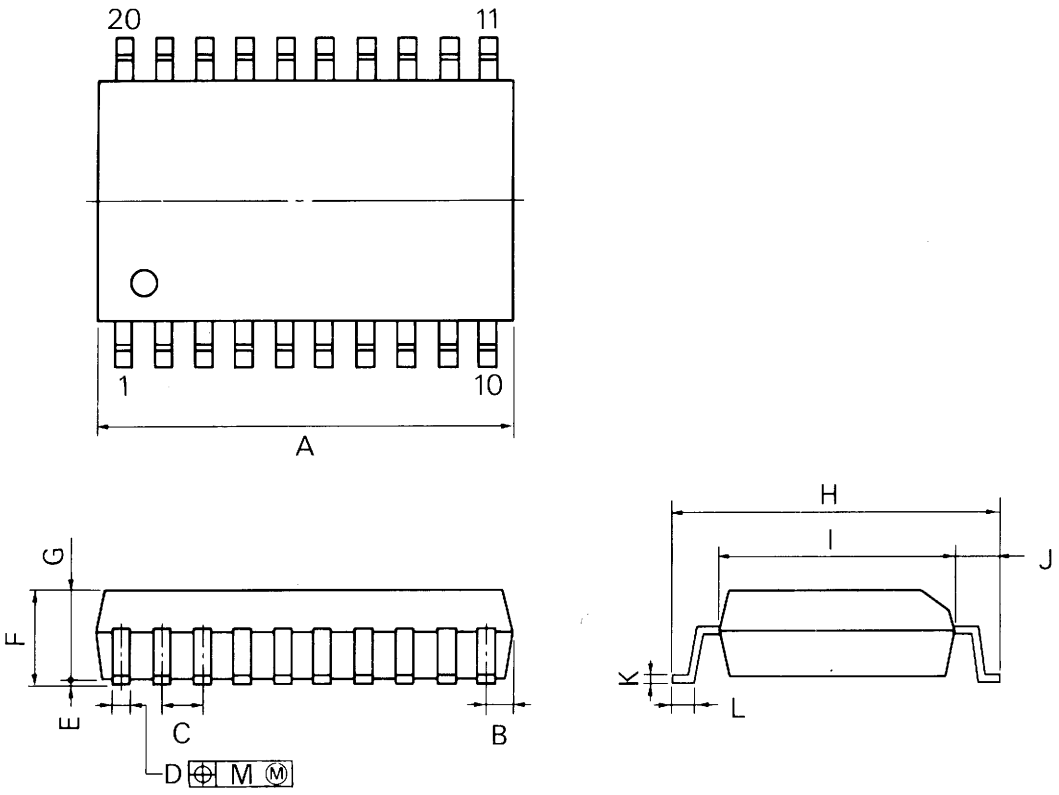
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	22.86 MAX.	0.900 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	1.0 MIN.	0.039 MIN.

μPD6450GT-102

20PIN PLASTIC SOP (375 mil)



P20GM-50-375B-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.00 MAX.	0.512 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{0.05}$	$0.016^{+0.004}_{-0.003}$
E	$0.1^{+0.2}_{0.1}$	$0.004^{+0.008}_{0.004}$
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	$10.3^{\pm0.3}$	$0.406^{+0.012}_{0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{0.05}$	$0.006^{+0.004}_{-0.002}$
L	$0.8^{+0.2}$	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005

[MEMO]