

# MC10178

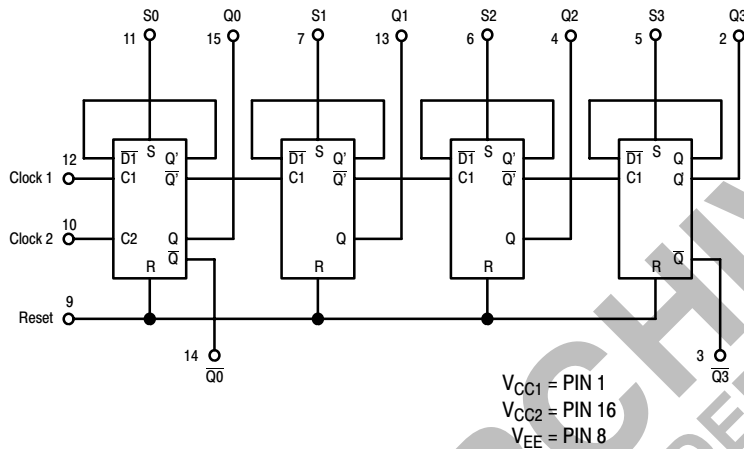
## Binary Counter

The MC10178 is a four-bit counter capable of divide-by-two, divide-by-four, divide-by-eight or a divide-by-sixteen function.

Clock inputs trigger on the positive going edge of the clock pulse. Set and Reset inputs override the clock, allowing asynchronous "set" or "clear." Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

- $P_D = 370 \text{ mW typ/pkg (No Load)}$
- $f_{\text{toggle}} = 150 \text{ MHz (typ)}$
- $t_r, t_f = 2.7 \text{ ns typ (20\%–80\%)}$

### LOGIC DIAGRAM



### TRUTH TABLE

INPUTS							OUTPUTS			
R	S0	S1	S2	S3	C1	C2	Q0	Q1	Q2	Q3
H	L	L	L	L	X	X	L	L	L	L
L	H	H	H	H	X	X	H	H	H	H
L	L	L	L	L	H	X	No Count			
L	L	L	L	L	X	H	No Count			
L	L	L	L	L	**	**	L	L	L	L
L	L	L	L	L	**	**	H	L	L	L
L	L	L	L	L	**	**	L	H	L	L
L	L	L	L	L	**	**	H	H	L	L
L	L	L	L	L	**	**	L	L	H	L
L	L	L	L	L	**	**	H	L	H	L
L	L	L	L	L	**	**	L	L	L	H
L	L	L	L	L	**	**	H	L	L	H
L	L	L	L	L	**	**	L	H	L	H
L	L	L	L	L	**	**	H	L	H	H
L	L	L	L	L	**	**	L	H	H	H
L	L	L	L	L	**	**	H	H	H	H

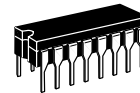
\*\* Clock transition from  $V_{IL}$  to  $V_{IH}$  may be applied to C1 or C2 or both for same effect.



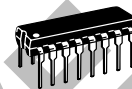
ON Semiconductor

<http://onsemi.com>

### MARKING DIAGRAMS



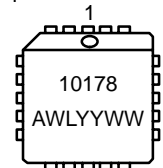
CDIP-16  
L SUFFIX  
CASE 620



PDIP-16  
P SUFFIX  
CASE 648

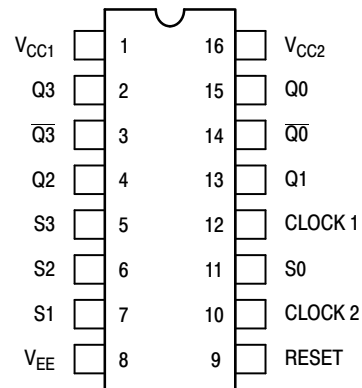


PLCC-20  
FN SUFFIX  
CASE 775



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

### DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.  
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).

### ORDERING INFORMATION

Device	Package	Shipping
MC10178L	CDIP-16	25 Units / Rail
MC10178P	PDIP-16	25 Units / Rail
MC10178FN	PLCC-20	46 Units / Rail

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## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits						Unit		
			-30°C		+25°C			+85°C			
			Min	Max	Min	Typ	Max	Min		Max	
Power Supply Drain Current	$I_E$	8		97			88		97	mAdc	
Input Current	$I_{inH}$	12		390			245		245	$\mu$ Adc	
		11		350			220		220		
9			650			410		410			
	$I_{inL}$	*	0.5		0.5			0.3		$\mu$ Adc	
Output Voltage Logic 1	$V_{OH}$	14	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc	
		15	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700		
Output Voltage Logic 0	$V_{OL}$	14	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	
		15	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615		
Threshold Voltage Logic 1	$V_{OHA}$	3	-1.080		-0.980			-0.910		Vdc	
		14	-1.080		-0.980			-0.910			
		15	-1.080		-0.980			-0.910			
Threshold Voltage Logic 0	$V_{OLA}$	3		-1.655			-1.630		-1.595	Vdc	
		14		-1.655			-1.630		-1.595		
		15		-1.655			-1.630		-1.595		
Switching Times (50 $\Omega$ Load)										ns	
Propagation Delay	Clock Input	$t_{12+15+}$	15	1.4	5.0	1.5	3.5	4.8	1.5	5.3	
		$t_{12-13-}$	13	1.9	9.4	2.0	6.0	9.2	2.0	9.8	
		$t_{12+4-}$	4	2.9	12.3	3.0	8.5	12.0	3.0	12.8	
		$t_{12-3+}$	3	3.9	14.9	4.0	11.0	14.5	4.0	15.5	
Rise Time (20 to 80%)		$t_{15+}$	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0	
Fall Time (20 to 80%)		$t_{15-}$	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0	
Set Input		$t_{11-15+}$	15	1.4	5.2	1.5		5.0	1.5	5.5	
Reset Input		$t_{9-15+}$	15	1.4	5.2	1.5		5.0	1.5	5.5	
Counting Frequency		$f_{count}$	15	125		125	150		125		MHz

\* Individually test each input applying  $V_{IL}$  to input under test.

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## ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature -30°C +25°C +85°C			TEST VOLTAGE VALUES (Volts)					(V <sub>CC</sub> ) Gnd
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>	
			-0.890	-1.890	-1.205	-1.500	-5.2	
			-0.810	-1.850	-1.105	-1.475	-5.2	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>	
Power Supply Drain Current	I <sub>E</sub>	8	9				8	1, 16
Input Current	I <sub>inH</sub>	12	12				8	1, 16
		11	11				8	1, 16
		9	9				8	1, 16
	I <sub>inL</sub>	*		*			8	1, 16
Output Voltage Logic 1	V <sub>OH</sub>	14	9				8	1, 16
		15	11				8	1, 16
Output Voltage Logic 0	V <sub>OL</sub>	14	11				8	1, 16
		15	9				8	1, 16
Threshold Voltage Logic 1	V <sub>OHA</sub>	3			5		8	1, 16
		14			11		8	1, 16
		15			9		8	1, 16
Threshold Voltage Logic 0	V <sub>OLA</sub>	3			5		8	1, 16
		14			11		8	1, 16
		15			9		8	1, 16
Switching Times (50Ω Load)					Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay Data Input	t <sub>12+15+</sub> t <sub>12-13-</sub> t <sub>12+4-</sub> t <sub>12-3+</sub>	15			12	15	8	1, 16
		13			12	13	8	1, 16
		4			12	4	8	1, 16
		3			12	3	8	1, 16
Rise Time (20 to 80%)	t <sub>+</sub>	15			12	15	8	1, 16
Fall Time (20 to 80%)	t <sub>-</sub>	15			12	15	8	1, 16
Set Input	t <sub>11-15+</sub>	15			11	15	8	1, 16
Reset Input	t <sub>9-15+</sub>	15			9	15	8	1, 16
Counting Frequency	f <sub>count</sub>	15			12	15	8	1, 16

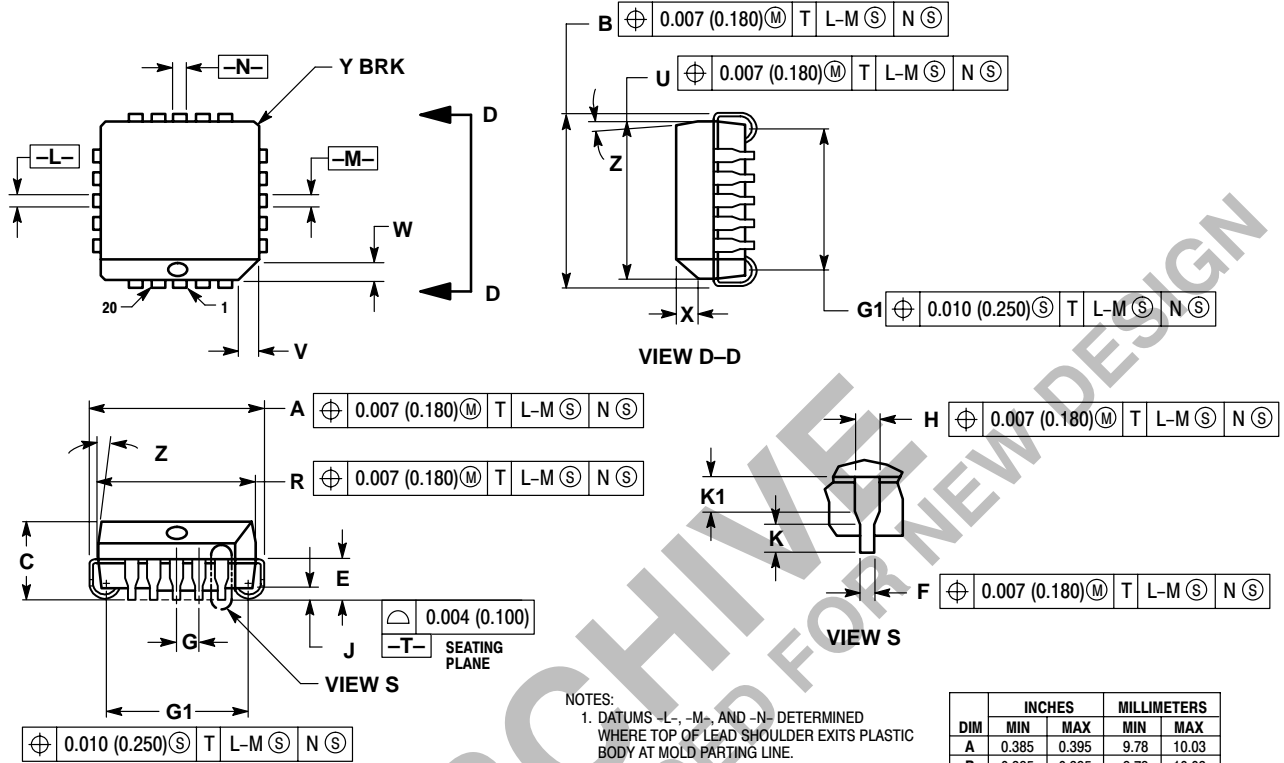
\* Individually test each input applying V<sub>IL</sub> to input under test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

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## PACKAGE DIMENSIONS

PLCC-20  
FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 775-02  
ISSUE C



### NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

# MC10178

## PACKAGE DIMENSIONS

### CDIP-16 L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

### PDIP-16 P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

**Notes**

ARCHIVE  
DEVICE NOT RECOMMENDED FOR NEW DESIGN

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RECOMMENDED FOR NEW DESIGN

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