

AT59C11/12/13

T-46-13-27

Features

- Low Voltage and Standard Voltage Operation
 - 5.0 V (V_{CC} = 4.5 V to 5.5 V)
 - 3.0 V (V_{CC} = 2.7 V to 5.5 V)
- User Selectable Internal Organization
 - 1K: 128 x 8 or 64 x 16
 - 2K: 256 x 8 or 128 x 16
 - 4K: 512 x 8 or 256 x 16
- Four-Wire Serial Interface
- Self-Timed Write Cycle (10 ms Max)
- High Reliability
 - Endurance: 100,000 Cycles
 - Data Retention: 100 Years
- 8-Pin PDIP and JEDEC SOIC Packages

Description

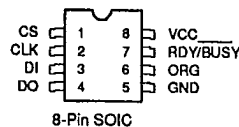
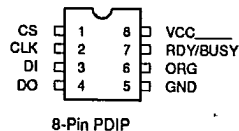
The AT59C11/12/13 provides 1024/2048/4096 bits of serial E²PROM (Electrically Erasable Programmable Read Only Memory) organized as 64/128/256 words of 16 bits each, when the ORG Pin is connected to V_{CC} and 128/256/512 words of 8 bits each when it is tied to ground. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT59C11/12/13 is available in space saving 8-pin PDIP and 8-pin JEDEC and SOIC packages.

The AT59C11/12/13 is enabled through the Chip Select pin (CS), and accessed via a 4-wire serial interface consisting of Data Input (DI), Data Output (DO), and Clock (CLK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO, the WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. Ready/Busy status can be monitored upon completion of a programming operation by polling the Ready/Busy pin.

Atmel's E²PROMs are designed and tested for applications requiring extended endurance. Devices in this family are guaranteed for 100,000 ERASE/WRITE cycles and 100-year data retention. The AT59C11/12/13 is available in 5.0 V ± 10% and 2.7 V to 5.5 V versions. Data retention is specified to be greater than 100 years.

Pin Configurations

Pin Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V _{CC}	Power Supply
ORG	Internal Organization
RDY/BUSY	Status Output

4-Wire
Serial CMOS
E²PROMs

1K (128 x 8 or 64 x 16)

2K (256 x 8 or 128 x 16)

4K (512 x 8 or 256 x 16)

Preliminary

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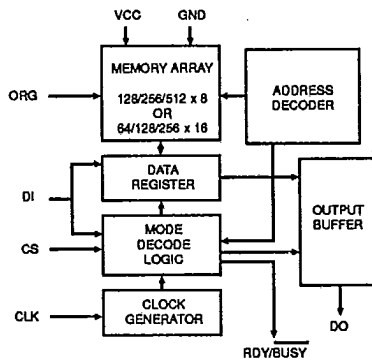


Absolute Maximum Ratings*

Operating Temperature.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.25 V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram ⁽¹⁾



Note:

1. When the ORG pin is connected to Vcc, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x 16 organization.

D.C. Characteristics

Applicable over recommended operating range from: T_A = -40°C to +85°C, V_{CC} = +2.7 V to +5.5 V, T_{AC} = 0°C to +70°C, V_{CC} = +2.7 V to +5.5 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Max	Units
I _{CC1}	Operating Current CMOS Input Levels	CS = V _{IH} , CLK = 1.0 MHz ⁽¹⁾ CLK = 0.5 MHz ⁽¹⁾		2	mA
I _{CC2}	Operating Current TTL Input Levels	CS = V _{IH} , CLK = 1.0 MHz ⁽¹⁾ CLK = 0.5 MHz ⁽¹⁾		3	mA
I _{CC3}	Standby Current	CS = 0 V, CLK = 1.0 MHz ⁽¹⁾ CLK = 0.5 MHz ⁽¹⁾		100	μA
I _{IL}	Input Leakage	V _{IN} = 0 V to V _{CC}	-2.5 -10	2.5 10	μA
I _{OL}	Output Leakage	V _{IN} = 0 V to V _{CC}	-2.5 -10	2.5 10	μA
V _{IL1} V _{IH1}	Input Low Voltage Input High Voltage	4.5 V ≤ V _{CC} ≤ 5.5 V	2	0.8	V
V _{IL2} V _{IH2}	Input Low Voltage Input High Voltage	2.7 V ≤ V _{CC} ≤ 5.5 V	-0.1 2	0.6 V _{CC} + 1	V
V _{OL1} V _{OH1}	Output Low Voltage Output High Voltage	4.5 V ≤ V _{CC} ≤ 5.5 V I _{OL} = 2.1 mA I _{OH} = -400 μA	2.4	0.4	V V
V _{OL2} V _{OH2}	Output Low Voltage Output High Voltage	2.7 V ≤ V _{CC} ≤ 5.5 V I _{OL} = 10 μA I _{OH} = -10 μA	V _{CC} - 0.2	0.2	V V

Note: 1. Devices operate at 1.0 MHz at V_{CC} = 5.0 V ± 10% at commercial temperature. All low voltage and industrial parts operate at 0.5 MHz.

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A.C. Characteristics

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Applicable over recommended operating range from $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +2.7\text{ V}$ to $+5.5\text{ V}$, $CL = 1\text{ TTL Gate}$ and 100 pF (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Max	Units
tCLK	CLK Clock Frequency		0 0	1 0.5	MHz
tCKH	CLK High Time	Note 1 Note 2	500 500		ns
tCKL	CLK Low Time	Note 1 Note 2	250 500		ns
tCS	Minimum CS Low Time	Note 3 Note 4	250 500		ns
tCSS	CS Setup Time	Relative to CLK	50 100		ns
tDIS	DI Setup Time	Relative to CLK	100 200		ns
tCSH	CS Hold Time	Relative to CLK	0		ns
tDIH	DI Hold Time	Relative to CLK	100 200		ns
tPD	Output Delay	AC Test		500 1000	ns
tRSD	CS to Status Valid	AC Test		500 1000	ns
tOZ	CS to DO in High Impedance	AC Test CS = V_{IL}		100 200	ns
tWC	Write Cycle Time			10	ms
	Endurance	Number of Data Changes per Bit	Typical 100,000		Cycles

Notes:

- The CLK frequency specification for Commercial parts specifies a minimum CLK clock period of $1\ \mu\text{s}$, therefore in an CLK clock cycle $t_{CKH} + t_{CKL}$ must be greater than or equal to $2\ \mu\text{s}$. For example if $t_{CKL} = 250\text{ ns}$ then the minimum $t_{CKH} = 750\text{ ns}$ in order to meet the CLK frequency specification.
- The CLK frequency specification for extended Temperature parts specifies a minimum CLK clock period of $2\ \mu\text{s}$, therefore in an CLK clock cycle $t_{CKH} + t_{CKL}$ must be greater than or equal to $2\ \mu\text{s}$. For example, if the $t_{CKL} = 500\text{ ns}$ then the minimum $t_{CKH} = 1.5\ \mu\text{s}$ in order to meet the CLK frequency specification.
- For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.
- For Extended Temperature parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Pin Capacitance ⁽¹⁾

Applicable over recommended operating range from $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$, $V_{CC} = +5.0\text{ V}$ (unless otherwise noted)

Test Conditions		Max	Units	Conditions
COUT	Output Capacitance (DO)	5	pF	$V_{OUT} = 0\text{ V}$
CIN	Input Capacitance (CS, CLK, DI, RDY/BUSY)	5	pF	$V_{IN} = 0\text{ V}$

Note: 1. This parameter is characterized and is not 100% tested.





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Functional Description

The AT59C11/12/13 are accessed via a simple and versatile 4-wire serial communication interface. Device operation is controlled by 6 instructions issued by the host processor. A valid instruction consists of a Start Bit (logic '1') followed by the appropriate Op Code and the desired memory Address location.

READ (READ): The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock CLK. It should be noted that a dummy bit (logic '0') precedes the 8- or 16-bit data output string.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or Vcc power is removed from the part.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle starts after the last bit of data is received at serial data input pin DI. The

Ready/Busy status of the AT59C11/12/13 can be determined by polling the RDY/BUSY pin. A logic '0' at DO indicates that programming is still in progress. A logic '1' indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions.

ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic '1' state and is primarily used for testing purposes. The Ready/Busy status of the AT59C11/12/13 can be determined by polling the RDY/BUSY pin. The ERAL instruction is valid only at Vcc = 5.0 V ± 10%.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The Ready/Busy status of the AT59C11/12/13 can be determined by polling the RDY/BUSY pin. The WRAL instruction is valid only at Vcc = 5.0 V ± 10%.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Instruction Set for the AT59C11

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10XX	A ₆ -A ₀	A ₅ -A ₀			Reads data stored in memory, at specified address.
EWEN	1	0011	0000000	0000000			Write enable must precede all programming modes.
WRITE	1	X1XX	A ₆ -A ₀	A ₅ -A ₀	D ₇ -D ₀	D ₁₅ -D ₀	Writes memory location A _n - A ₀ .
ERAL	1	0010	0000000	0000000			Erases all memory locations. Valid only at Vcc = 4.5 V to 5.5 V.
WRAL	1	0001	0000000	0000000	D ₇ -D ₀	D ₁₅ -D ₀	Writes all memory locations. Valid only at Vcc = 4.5 V to 5.5 V.
EWDS	1	0000	0000000	0000000			Disables all programming instructions.

AT59C11/12/13

Instruction Set for the AT59C12 and AT59C13

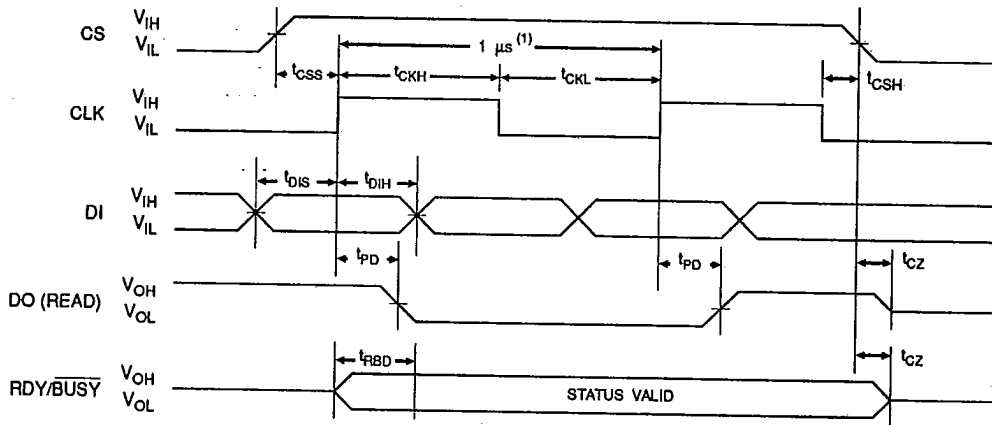
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Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10XX	A ₈ -A ₀	A ₇ -A ₀			Reads data stored in memory, at specified address.
EWEN	1	0011	00000000	00000000			Write enable must precede all programming modes.
WRITE	1	X1XX	A ₈ -A ₀	A ₇ -A ₀	D ₇ -D ₀	D ₁₅ -D ₀	Writes memory location A _n - A ₀ .
ERAL	1	0010	00000000	00000000			Erases all memory locations. Valid only at V _{CC} = 4.5 V to 5.5 V.
WRAL	1	0001	00000000	00000000	D ₇ -D ₀	D ₁₅ -D ₀	Writes all memory locations. Valid when V _{CC} = 5.0 V ± 10% and Disable Register cleared.
EWDS	1	0000	00000000	00000000			Disables all programming instructions.



Timing Diagrams

Synchronous Data Timing



Note: 1. This is the minimum CLK period.

Organization Key for Timing Diagrams

I/O	Density 1K		Density 2K		Density 4K	
	x 8	x 16	x 8	x 16	x 8	x 16
A _N	A ₆	A ₅	A ₈	A ₇	A ₈	A ₇
D _N	D ₇	D ₁₅	D ₇	D ₁₅	D ₇	D ₁₅

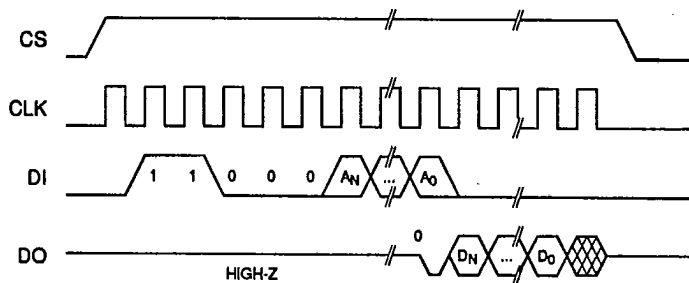




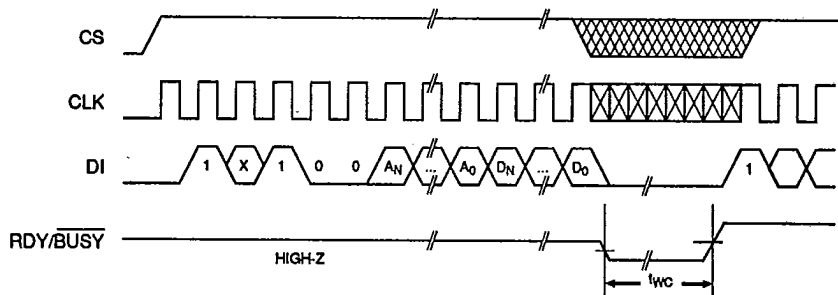
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Timing Diagrams (Continued)

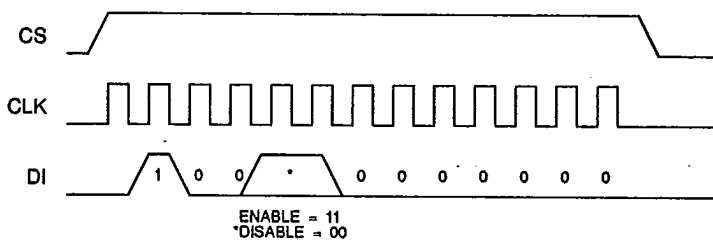
READ Timing



WRITE Timing



EWEN/EWDS Timing





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Ordering Information

t _{wc} (ms)	I _{cc} (mA)	f _{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3.0	1000	AT59C11-10PC (-2.7)	8P3	Commercial (0°C to 70°C)
			AT59C11-10SC (-2.7)	8S1	
			AT59C11-10PI (-2.7)	8P3	Industrial (-40°C to 85°C)
AT59C11-10SI (-2.7)	8S1				
			AT59C11-10PM	8P3	Military (-55°C to 125°C)

10	3.0	1000	AT59C12-10PC (-2.7)	8P3	Commercial (0°C to 70°C)
			AT59C12-10SC (-2.7)	8S1	
			AT59C12-10PI (-2.7)	8P3	Industrial (-40°C to 85°C)
AT59C12-10SI (-2.7)	8S1				
			AT59C12-10PM	8P3	Military (-55°C to 125°C)

10	3.0	1000	AT59C13-10PC (-2.7)	8P3	Commercial (0°C to 70°C)
			AT59C13-10SC (-2.7)	8S1	
			AT59C13-10PI (-2.7)	8P3	Industrial (-40°C to 85°C)
AT59C13-10SI (-2.7)	8S1				
			AT59C13-10PM	8P3	Military (-55°C to 125°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 5.5 V)