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April 1st, 2010 Renesas Electronics Corporation

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HD74LS166A

8-bit Shift Register

REJ03D0450-0400 Rev.4.00 May 10, 2006

The inputs are buffered to lower the drive requirements to one series 74 or 74LS standard load, respectively. Input clamping diodes minimize switching transients and simplify system design. This parallel in or serial-in, serial-out shift register has a complexity of 77 equivalent gates on a monolithic chip. This device features gated clock inputs and an overriding clear input.

The parallel-in or serial-in modes are established by the shift / load input.

When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse, during parallel loading, serial data flow is inhibited.

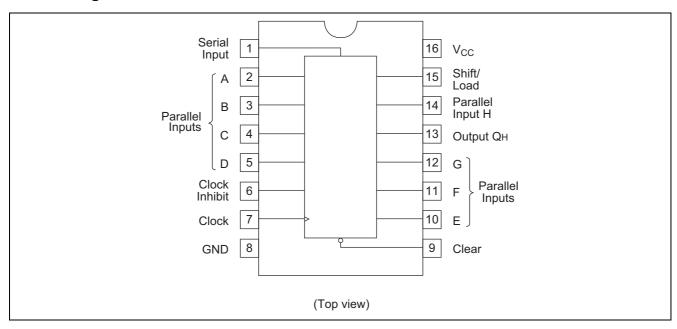
This, of course, allows the system clock to be free running and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

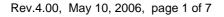
Features

• Ordering Information

| Part Name | Package Type | Package Code (Previous Code) | Package Abbreviation | Taping Abbreviation (Quantity) |
|-------------|--------------|---------------------------------|-------------------------|--------------------------------|
| HD74LS166AP | DILP-16 pin | PRDP0016AE-B (DP-16FV) | Р | _ |

Pin Arrangement







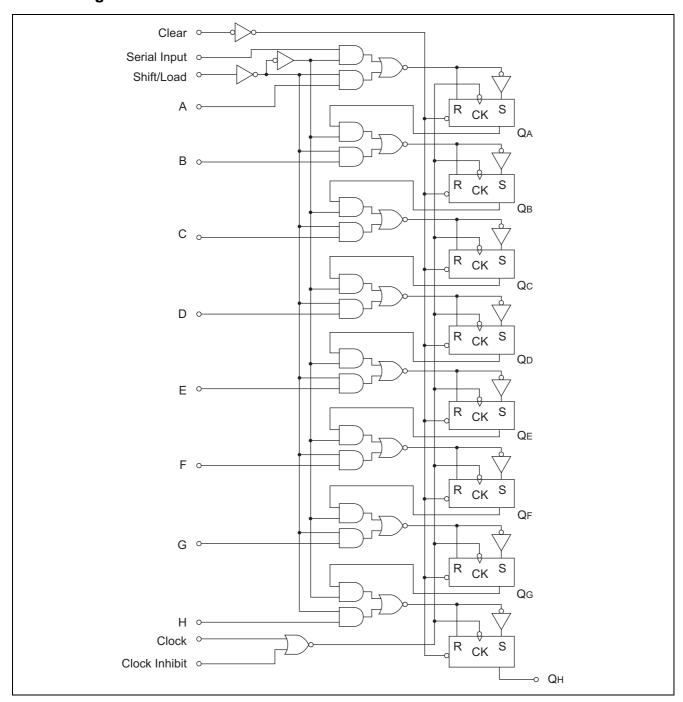
Function Table

| Inputs | | | | | | Internal outputs | | Outroot |
|--------|-------|---------|-------|--------|----------|------------------|-----------------|--------------------------|
| Clear | Shift | Clock | Clock | Serial | Parallel | internal outputs | | Output Q _H |
| Clear | Load | Inhibit | CIOCK | | AH | Q_A | Q _B | ≪ H |
| L | X | Х | X | Х | Х | L | L | L |
| Н | X | L | L | Х | Х | Q_{A0} | Q_{B0} | Q _{H0} |
| Н | L | L | 1 | Х | ah | а | b | h |
| Н | Н | L | 1 | Н | Х | Н | Q _{An} | Q_{Gn} |
| Н | Н | L | 1 | L | Х | L | Q _{An} | Q_{Gn} |
| Н | Х | Н | 1 | Х | Х | Q_{A0} | Q _{B0} | Q _{H0} |

Notes: 1. H; high level, L; low level, X; irrelevant

- 2. ↑; transition from low to high level
- 3. a to h; the level of steady-state input at inputs A to H respectively
- 4. Q_{A0} to Q_{H0} ; the level of Q_A to Q_H , respectively, before the indicated steady-state input conditions were established.
- 5. Q_{An} to Q_{Gn} ; the level of Q_A to Q_G , respectively, before the most recent \uparrow transition of the clock.

Block Diagram



Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit |
|---------------------|-----------------|-------------|------|
| Supply voltage | V _{CC} | 7 | V |
| Input voltage | V _{IN} | 7 | V |
| Power dissipation | P _T | 400 | mW |
| Storage temperature | Tstg | -65 to +150 | °C |

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

| Item | Symbol | Min | Тур | Max | Unit |
|-----------------------------|------------------|------|------|------|------|
| Supply voltage | V _{CC} | 4.75 | 5.00 | 5.25 | V |
| Output current | I _{OH} | _ | _ | -400 | μΑ |
| Output current | I _{OL} | _ | _ | 8 | mA |
| Operating temperature | T _{opr} | -20 | 25 | 75 | °C |
| Clock frequency | f_{clock} | 0 | _ | 25 | MHz |
| Clock and clear pulse width | t _w | 20 | _ | _ | ns |
| Mode control setup time | t _{su} | 30 | _ | _ | ns |
| Data setup time | t _{su} | 20 | _ | _ | ns |
| Hold time | t _h | 0 | _ | _ | ns |

Electrical Characteristics

 $(Ta = -20 \text{ to } +75 \text{ }^{\circ}\text{C})$

| Item | Symbol | min. | typ.* | max. | Unit | Condition |
|----------------------|-----------------|------|-------|------|------|--|
| lanut valta sa | V _{IH} | 2.0 | _ | _ | V | |
| Input voltage | V _{IL} | _ | _ | 0.8 | V | |
| | V _{OH} | 2.7 | _ | | V | $V_{CC} = 4.75 \text{ V}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V},$ |
| Output voltage | V OH | 2.1 | | _ | V | $I_{OH} = -400 \mu\text{A}$ |
| Output voltage | V _{OL} | _ | _ | 0.4 | V | $I_{OL} = 4 \text{ mA}$ $V_{CC} = 4.75 \text{ V}, V_{IH} = 2 \text{ V},$ |
| | | _ | _ | 0.5 | V | $I_{OL} = 8 \text{ mA}$ $V_{IL} = 0.8 \text{ V}$ |
| | I _{IH} | _ | _ | 20 | μΑ | $V_{CC} = 5.25 \text{ V}, V_{I} = 2.7 \text{ V}$ |
| Input current | I _{IL} | _ | _ | -0.4 | mA | $V_{CC} = 5.25 \text{ V}, V_I = 0.4 \text{ V}$ |
| | I _I | _ | _ | 0.1 | mA | $V_{CC} = 5.25 \text{ V}, V_{I} = 7 \text{ V}$ |
| Short-circuit output | I _{OS} | -20 | _ | -100 | mA | V _{CC} = 5.25 V |
| current | ios | -20 | | -100 | ША | VCC = 3.23 V |
| Supply current** | I _{CC} | _ | 20 | 32 | mA | V _{CC} = 5.25 V |
| Input clamp voltage | V_{IK} | _ | _ | -1.5 | V | $V_{CC} = 4.75 \text{ V}, I_{IN} = -18 \text{ mA}$ |

Notes: $V_{CC} = 5 \text{ V}$, $Ta = 25^{\circ}\text{C}$

Switching Characteristics

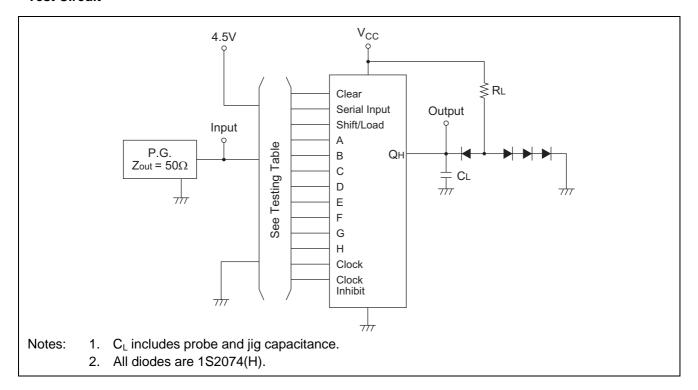
 $(V_{CC} = 5 \text{ V}, \text{ Ta} = 25^{\circ}\text{C})$

| Item | Symbol | Inputs | min. | typ. | max. | Unit | Condition |
|-------------------------|------------------|--------|------|------|------|------|--|
| Maximum clock frequency | $f_{\sf max}$ | | 25 | 35 | | MHz | |
| | t _{PHL} | Clear | _ | 19 | 30 | ns | $C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega$ |
| Propagation delay time | t _{PHL} | Clock | 7 | 14 | 25 | ns | $\frac{1}{2}$ $\frac{1}$ |
| | t _{PLH} | CIOCK | 5 | 11 | 20 | ns | |

^{**} With the outputs open, 4.5 V applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

Testing Method

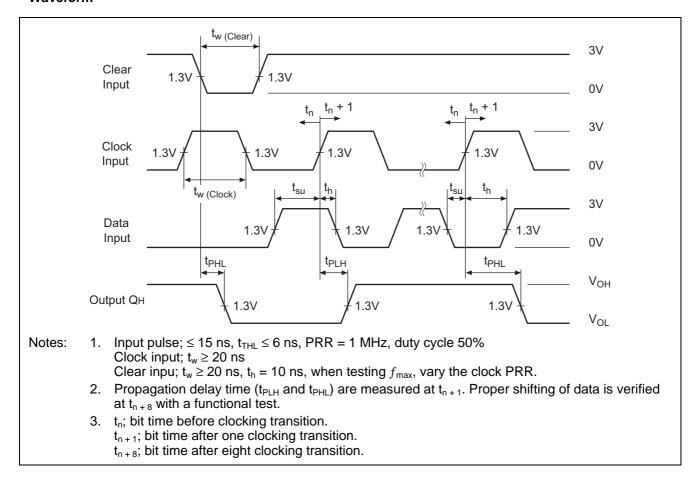
Test Circuit



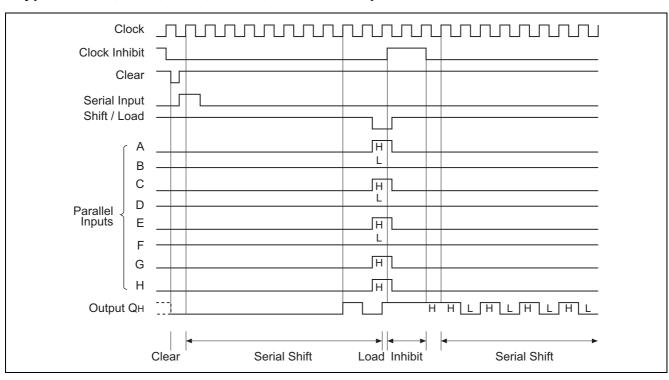
Testing table

| Data inputs | Shift / Load | Output | Bit time |
|-------------|--------------|----------------|--------------------|
| Data H | 0 V | Q _H | t _{n + 1} |
| Serial-in | 4.5 V | Q _H | t _{n + 8} |

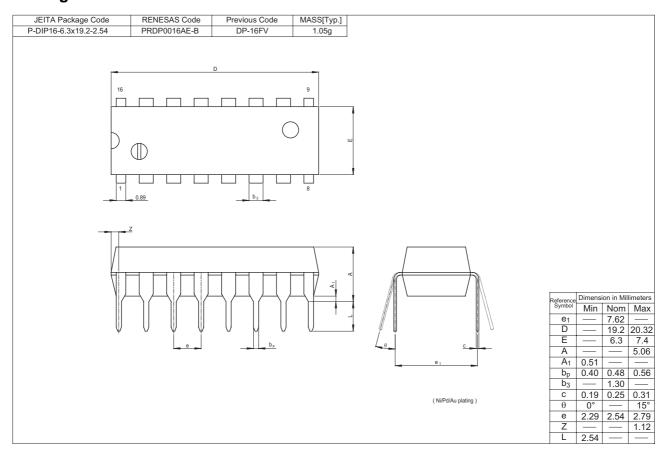
Waveform



Typical Clear, Shift, Load, Inhibit, and Shift Sequences



Package Dimensions



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Renesas Technology Europe Limited
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Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

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Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia Tel: <603> 7955-9390, Fax: <603> 7955-9510