MC14543B

BCD-to-Seven Segment Latch/Decoder/Driver for Liquid Crystals

The MC14543B BCD−to−seven segment latch/decoder/driver is designed for use with liquid crystal readouts, and is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4−bit storage latch and an 8421 BCD−to−seven segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. The outputs of the circuit are connected directly to the segments of the LC readout. For other types of readouts, such as light−emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

Applications include instrument (e.g., counter, DVM etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

Features

- Latch Storage of Code
- Blanking Input
- Readout Blanking on All Illegal Input Combinations
- Direct LED (Common Anode or Cathode) Driving Capability
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving 2 Low−power TTL Loads, 1 Low−power Schottky TTL Load or 2 HTL Loads Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4056A (with Pin 7 Tied to V_{SS}).
- Chip Complexity: 207 FETs or 52 Equivalent Gates
- Pb−Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	−0.5 to +18.0	V
Input Voltage Range, All Inputs	V_{in}	−0.5 to V_{DD} +0.5	V
DC Input Current per Pin	I_{in}	±10	mA
Power Dissipation per Package (Note 1)	P_D	500	mW
Operating Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Maximum Continuous Output Drive Current (Source or Sink)	I_{OHmax} I_{OLmax}	10 (per Output)	mA
Maximum Continuous Output Power (Source or Sink) (Note 2)	P_{OHmax} P_{OLmax}	70 (per Output)	mW

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating: Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C
2. $P_{OHmax} = I_{OH} (V_{OH} - V_{DD})$ and $P_{OLmax} = I_{OL} (V_{OL} - V_{SS})$

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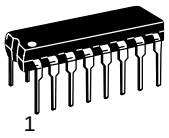
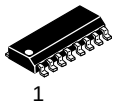
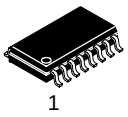
MARKING DIAGRAMS



PDIP−16
P SUFFIX
CASE 648



SOIC−16
D SUFFIX
CASE 751B



SOEIAJ−16
F SUFFIX
CASE 966

A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

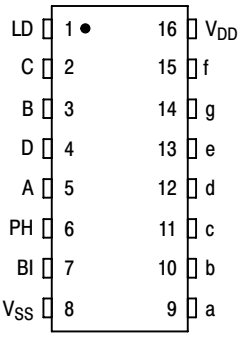
See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PIN ASSIGNMENT



TRUTH TABLE

Inputs							Outputs							
LD	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	1	0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	1	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X	**							**
†	†	†	†				Inverse of Output Combinations Above							Display as above

X = Don't care

† = Above Combinations

* = For liquid crystal readouts, apply a square wave to Ph
For common cathode LED readouts, select Ph = 0
For common anode LED readouts, select Ph = 1

** = Depends upon the BCD code previously applied when LD = 1

ORDERING INFORMATION

Device	Package	Shipping†
MC14543BCP	PDIP−16	25 Units / Rail
MC14543BCPG	PDIP−16 (Pb−Free)	
MC14543BD	SOIC−16	48 Units / Rail
MC14543BDG	SOIC−16 (Pb−Free)	
MC14543BDR2	SOIC−16	2500 / Tape & Reel
MC14543BDR2G	SOIC−16 (Pb−Free)	
MC14543BF	SOEIAJ−16	50 Units / Rail
MC14543BFG	SOEIAJ−16 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (Note 3)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	− − −	0.05 0.05 0.05	− − −	0 0 0	0.05 0.05 0.05	− − −	0.05 0.05 0.05	Vdc
“1” Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	− − −	4.95 9.95 14.95	5.0 10 15	− − −	4.95 9.95 14.95	− − −	Vdc
Input Voltage “0” Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	− − −	1.5 3.0 4.0	− − −	2.25 4.50 6.75	1.5 3.0 4.0	− − −	1.5 3.0 4.0	Vdc
“1” Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	− − −	3.5 7.0 11	2.75 5.50 8.25	− − −	3.5 7.0 11	− − −	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 0.5 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 10 15	− 3.0 − 0.64 − − 1.6 − 4.2	− − − − −	− 2.4 − 0.51 − − 1.3 − 3.4	− 4.2 − 0.88 − 10.1 − 2.25 − 8.8	− − − − −	− 1.7 − 0.36 − − 0.9 − 2.4	− − − −	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 9.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 10 15	0.64 1.6 − 4.2	− − − −	0.51 1.3 − 3.4	0.88 2.25 10.1 8.8	− − − −	0.36 0.9 − 2.4	− − −	mAdc
Input Current	I_{in}	15	−	±0.1	−	±0.00001	±0.1	−	±1.0	μAdc
Input Capacitance	C_{in}	−	−	−	−	5.0	7.5	−	−	pF
Quiescent Current (Per Package) V_{in} = 0 or V_{DD}, I_{out} = 0 μA	I_{DD}	5.0 10 15	− − −	5.0 10 20	− − −	0.005 0.010 0.015	5.0 10 20	− − −	150 300 600	μAdc
Total Supply Current (Note 4, 5) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (1.6 μA/kHz) f + I_{DD} I_T = (3.1 μA/kHz) f + I_{DD} I_T = (4.7 μA/kHz) f + I_{DD}							μAdc

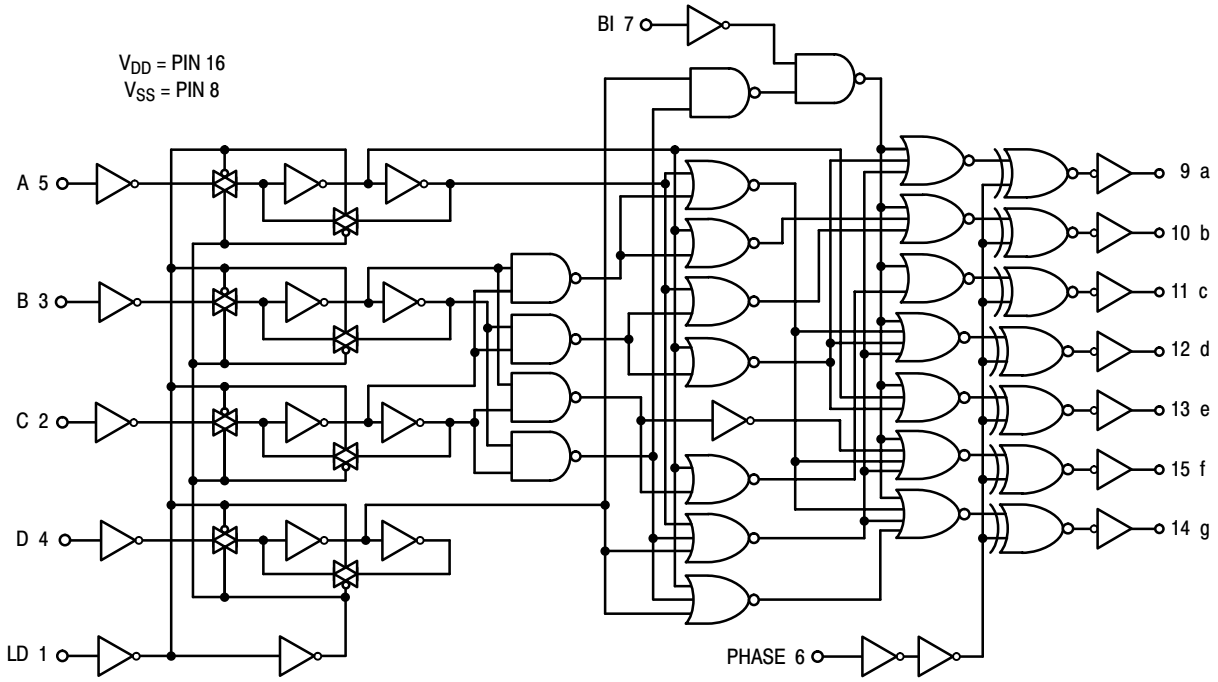
3. Noise immunity specified for worst−case input combination.
   Noise Margin for both “1” and “0” level = 1.0 V min @ V_{DD} = 5.0 V
   2.0 V min @ V_{DD} = 10 V
   2.5 V min @ V_{DD} = 15 V
4. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$ where: I_T is in μA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency.
5. The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS (Note 6) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time t_{TLH} = (3.0 ns/pF) C_L + 30 ns t_{TLH} = (1.5 ns/pF) C_L + 15 ns t_{TLH} = (1.1 ns/pF) C_L + 10 ns	t_{TLH}	 5.0 10 15	 – – –	 100 50 40	 200 100 80	ns
Output Fall Time t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{THL} = (0.55 ns/pF) C_L + 12.5 ns	t_{THL}	 5.0 10 15	 – – –	 100 50 40	 200 100 80	ns
Turn−Off Delay Time t_{PLH} = (1.7 ns/pF) C_L + 520 ns t_{PLH} = (0.66 ns/pF) C_L + 217 ns t_{PLH} = (0.5 ns/pF) C_L + 160 ns	t_{PLH}	 5.0 10 15	 – – –	 605 250 185	 1210 500 370	ns
Turn−On Delay Time t_{PHL} = (1.7 ns/pF) C_L + 420 ns t_{PHL} = (0.66 ns/pF) C_L + 172 ns t_{PHL} = (0.5 ns/pF) C_L + 130 ns	t_{PHL}	 5.0 10 15	 – – –	 505 205 155	 1650 660 495	ns
Setup Time	t_{su}	5.0 10 15	350 450 500		– – –	ns
Hold Time	t_h	5.0 10 15	40 30 20		– – –	ns
Latch Disable Pulse Width (Strobing Data)	t_{WH}	5.0 10 15	250 100 80	125 50 40	– – –	ns

6. The formulas given are for the typical characteristics only.

LOGIC DIAGRAM



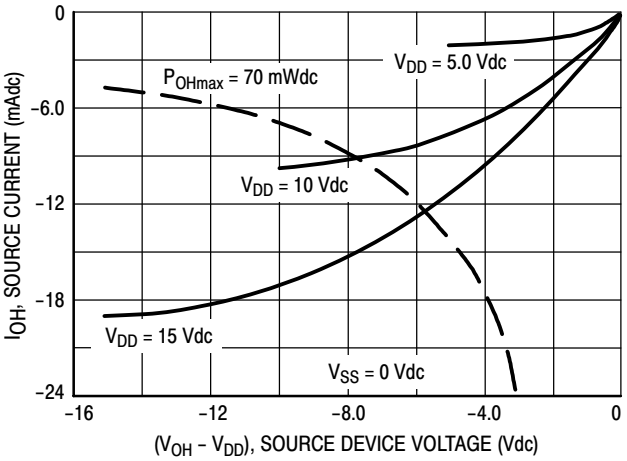


Figure 1. Typical Output Source Characteristics

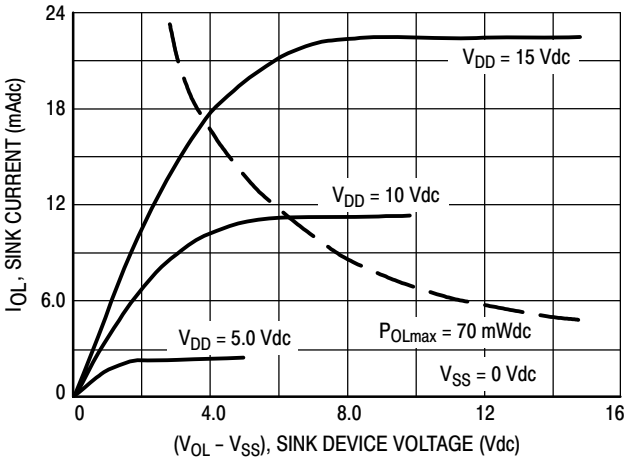


Figure 2. Typical Output Sink Characteristics

Inputs BI and Ph low, and Inputs D and LD high.
f in respect to a system clock.

All outputs connected to respective C_L loads.

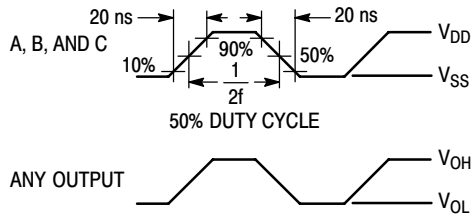
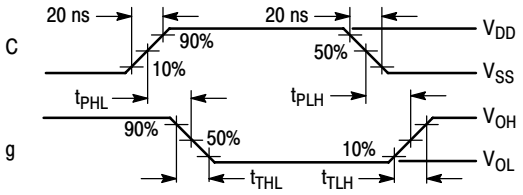
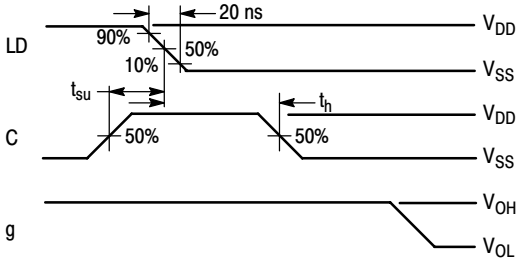


Figure 3. Dynamic Power Dissipation Signal Waveforms

(a) Inputs D, Ph, and BI low, and Inputs A, B, and LD high.



(b) Inputs D, Ph, and BI low, and Inputs A and B high.



(c) Data DCBA strobed into latches

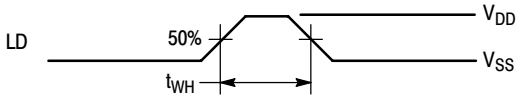
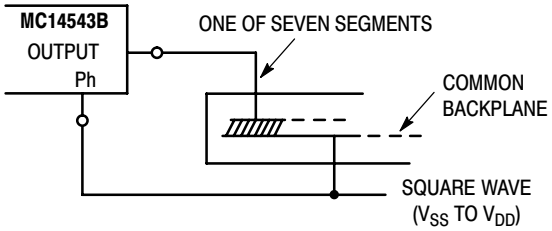


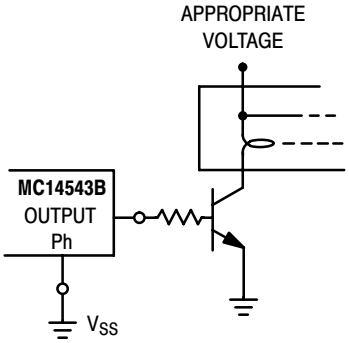
Figure 4. Dynamic Signal Waveforms

CONNECTIONS TO VARIOUS DISPLAY READOUTS

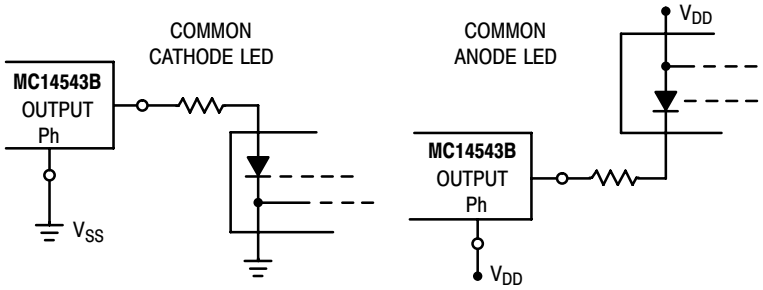
LIQUID CRYSTAL (LC) READOUT



INCANDESCENT READOUT

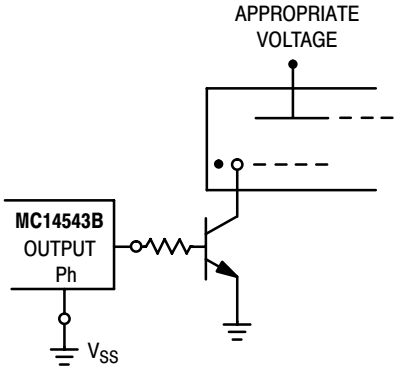


LIGHT EMITTING DIODE (LED) READOUT

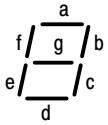


NOTE: Bipolar transistors may be added for gain (for $V_{DD} \leq 10$ V or $I_{out} \geq 10$ mA).

GAS DISCHARGE READOUT

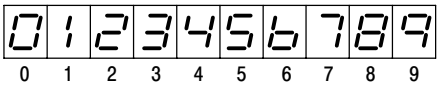


CONNECTIONS TO SEGMENTS



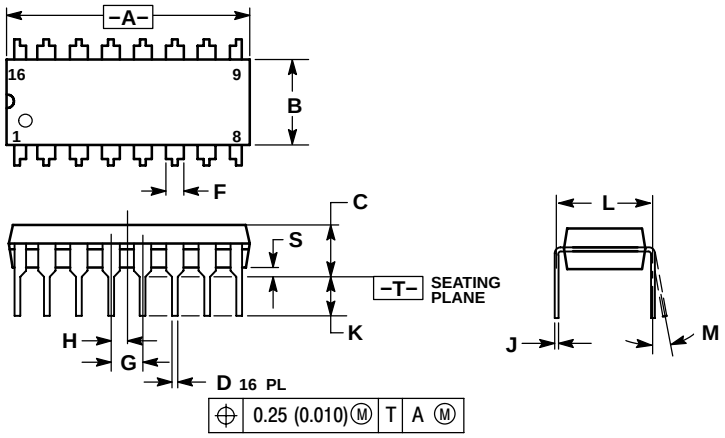
V_{DD} = PIN 16
V_{SS} = PIN 8

DISPLAY



PACKAGE DIMENSIONS

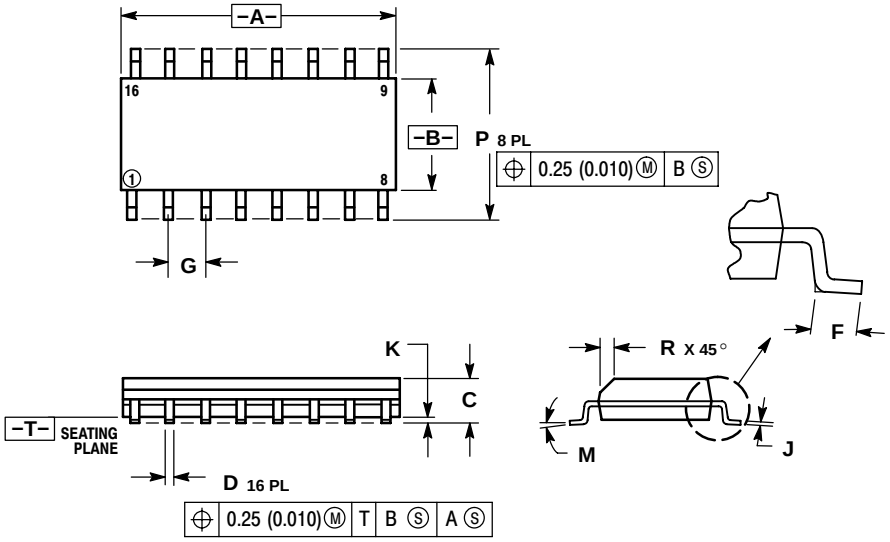
PDIP−16
CASE 648−08
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SOIC−16
CASE 751B−05
ISSUE J

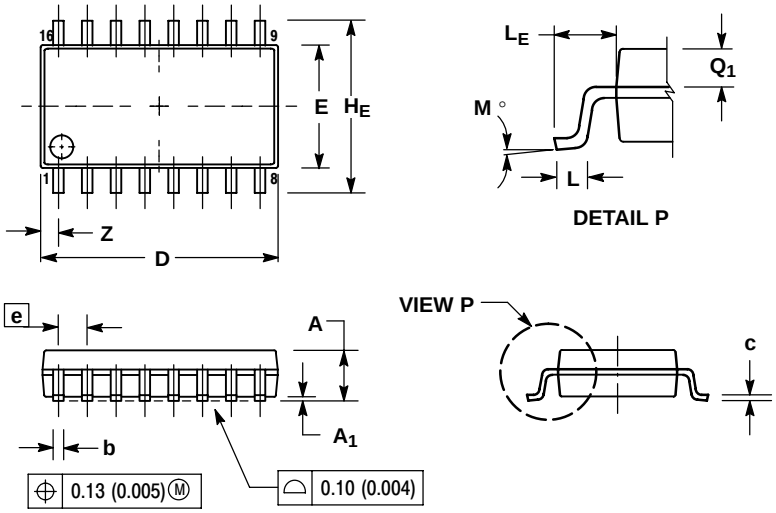


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

SOEIAJ−16
CASE 966−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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