MC145406

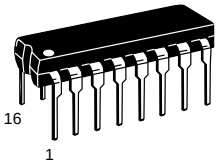
Driver/Receiver

EIA 232–E and CCITT V.28 (Formerly RS–232–D)

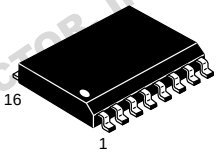
The MC145406 is a silicon–gate CMOS IC that combines three drivers and three receivers to fulfill the electrical specifications of standards EIA 232–E and CCITT V.28. The drivers feature true TTL input compatibility, slew–rate–limited output, 300–Ω power–off source impedance, and output typically switching to within 25% of the supply rails. The receivers can handle up to ±25 V while presenting 3 to 7 kΩ impedance. Hysteresis in the receivers aids reception of noisy signals. By combining both drivers and receivers in a single CMOS chip, the MC145406 provides efficient, low–power solutions for EIA 232–E and V.28 applications.

Drivers
- ± 5 V to ±12 V Supply Range
- 300–Ω Power–Off Source Impedance
- Output Current Limiting
- TTL Compatible
- Maximum Slew Rate = 30 V/µs

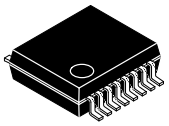
Receivers
- ± 25 V Input Voltage Range When V_{DD} = 12 V, V_{SS} = – 12 V
- 3 to 7 kΩ Input Impedance
- Hysteresis on Input Switchpoint



P SUFFIX
PLASTIC
CASE 648

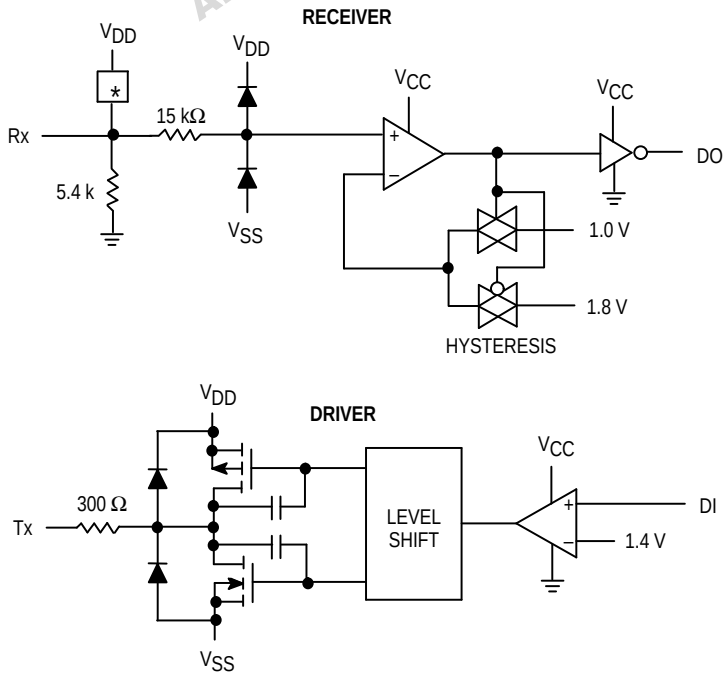


DW SUFFIX
SOG
CASE 751G



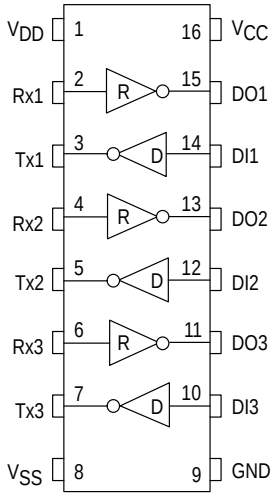
SD SUFFIX
SSOP
CASE 940B

BLOCK DIAGRAM



*Protection circuit

PIN ASSIGNMENT



D = DRIVER
R = RECEIVER

MAXIMUM RATINGS (Voltage polarities referenced to GND)

Rating	Symbol	Value	Unit
DC Supply Voltages ($V_{DD} \geq V_{CC}$)	V_{DD} V_{SS} V_{CC}	– 0.5 to + 13.5 + 0.5 to – 13.5 – 0.5 to + 6.0	V
Input Voltage Range Rx1–3 Inputs DI1–3 Inputs	V_{IR}	 (V_{SS} – 15) to (V_{DD} + 15) – 0.5 to (V_{CC} + 0.5)	V
DC Current Per Pin		± 100	mA
Power Dissipation	P_D	1.0	W
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Rate	T_{stg}	– 85 to + 150	°C

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range $GND \leq V_{DI} \leq V_{CC}$ and $GND \leq V_{DO} \leq V_{CC}$. Also, the voltage at the Rx pin should be constrained to $(V_{SS} – 15\ V) \leq V_{Rx1–3} \leq (V_{DD} + 15\ V)$, and Tx should be constrained to $V_{SS} \leq V_{Tx1–3} \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI and Ground for Rx.)

DC ELECTRICAL CHARACTERISTICS (All polarities referenced to GND = 0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage					V
V_{DD}	V_{DD}	4.5	5 to 12	13.2	
V_{SS}	V_{SS}	– 4.5	– 5 to – 12	– 13.2	
V_{CC} ($V_{DD} \geq V_{CC}$)	V_{CC}	4.5	5.0	5.5	
Quiescent Supply Current (Outputs unloaded, inputs low)					µA
V_{DD} = + 12 V	I_{DD}	—	140	400	
V_{SS} = – 12 V	I_{SS}	—	340	600	
V_{CC} = + 5 V	I_{CC}	—	300	450	

RECEIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V, V_{DD} = + 5 to + 12 V, V_{SS} = – 5 to – 12 V, $V_{DD} \geq V_{CC}$, T_A = – 40 to + 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Turn–on Threshold $V_{DO1–DO3} = V_{OL}$, V_{CC} = 5.0 V ± 5%	Rx1–Rx3	V_{on}	1.35	1.80	2.35	V
Input Turn–off Threshold $V_{DO1–DO3} = V_{OH}$, V_{CC} = 5.0 V ± 5%	Rx1–Rx3	V_{off}	0.75	1.00	1.25	V
Input Threshold Hysteresis V_{CC} = 5.0 V ± 5%	Rx1–Rx3	$V_{on}–V_{off}$	0.6	0.8	—	V
Input Resistance $(V_{SS} – 15\ V) \leq V_{Rx1–Rx3} \leq (V_{DD} + 15\ V)$	Rx1–Rx3	R_{in}	3.0	5.4	7.0	kΩ
High–Level Output Voltage ($V_{Rx1–Rx3}$ = – 3 V to (V_{SS} – 15 V))*	DO1–DO3	V_{OH}				V
I_{OH} = – 20 µA, V_{CC} = + 5.0 V			4.9	4.9	—	
I_{OH} = – 1 mA, V_{CC} = + 5.0 V			3.8	4.3	—	
Low–Level Output Voltage ($V_{Rx1–Rx3}$ = + 3 V to (V_{DD} + 15 V))*	DO1–DO3	V_{OL}				V
I_{OL} = + 20 µA, V_{CC} = + 5.0 V			—	0.01	0.1	
I_{OL} = + 2 mA, V_{CC} = + 5.0 V			—	0.02	0.5	
I_{OL} = + 4 mA, V_{CC} = + 5.0 V			—	0.5	0.7	

* This is the range of input voltages as specified by EIA 232–E to cause a receiver to be in the high or low logic state.

ELECTRICAL SPECIFICATIONS (Voltage polarities referenced to GND = 0 V, V_{CC} = + 5 V ± 5%, T_A = – 40 to + 85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Digital Input Voltage DI1–DI3					V
Logic 0	V_{IL}	—	—	0.8	
Logic 1	V_{IH}	2.0	—	—	
Input Current DI1–DI3	I_{in}	—	—	± 1.0	μA
$V_{DI1–DI3} = V_{CC}$					
Output High Voltage ($V_{DI1–3}$ = Logic 0, R_L = 3.0 kΩ) Tx1–Tx3	V_{OH}				V
V_{DD} = + 5.0 V, V_{SS} = – 5.0 V		3.5	3.9	—	
V_{DD} = + 6.0 V, V_{SS} = – 6.0		4.3	4.7	—	
V_{DD} = + 12.0 V, V_{SS} = – 12.0 V		9.2	9.5	—	
Output Low Voltage* ($V_{DI1–3}$ = Logic 1, R_L = 3.0 kΩ) Tx1–Tx3	V_{OL}				V
V_{DD} = + 5.0 V, V_{SS} = – 5.0 V		– 4.0	– 4.3	—	
V_{DD} = + 6.0 V, V_{SS} = – 6.0 V		– 4.5	– 5.2	—	
V_{DD} = + 12.0 V, V_{SS} = – 12.0 V		– 10.0	– 10.3	—	
Off Source Resistance (Figure 1) Tx1–Tx3		300	—	—	Ω
$V_{DD} = V_{SS}$ = GND = 0 V, $V_{Tx1–Tx3}$ = ± 2.0 V					
Output Short–Circuit Current (V_{DD} = + 12.0 V, V_{SS} = – 12.0 V) Tx1–Tx3	I_{SC}				mA
Tx1–Tx3 shorted to GND**		—	± 22	± 60	
Tx1–Tx3 shorted to ± 15.0 V***		—	± 60	± 100	

* The voltage specifications are in terms of absolute values.

** Specification is for one Tx output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits will be exceeded.

*** This condition could exceed package limitations.

SWITCHING CHARACTERISTICS (V_{CC} = + 5 V ± 5%, T_A = – 40 to + 85°C; See Figures NO TAG and NO TAG)

Drivers

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time Tx1–Tx3					ns
Low–to–High					
R_L = 3 kΩ, C_L = 50 pF	t_{PLH}	—	300	500	
High–to–Low	t_{PHL}				
R_L = 3 kΩ C_L = 50 pF		—	300	500	
Output Slew Rate Tx1–Tx3	SR				V/μs
Minimum Load					
R_L = 7 kΩ, C_L = 0 pF, V_{DD} = + 6 to + 12 V, V_{SS} = – 6 to – 12 V		—	± 9	± 30	
Maximum Load					
R_L = 3 kΩ, C_L = 2500 pF					
V_{DD} = + 12 V, V_{SS} = – 12 V		4	—	—	
V_{DD} = + 5 V, V_{SS} = – 5 V		—	—	—	

Receivers (C_L = 50 pF)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time DO1–DO3					ns
Low–to–High	t_{PLH}	—	150	425	
High–to–Low	t_{PHL}	—	150	425	
Output Rise Time DO1–DO3	t_r	—	250	400	ns
Output Fall Time DO1–DO3	t_f	—	40	100	ns

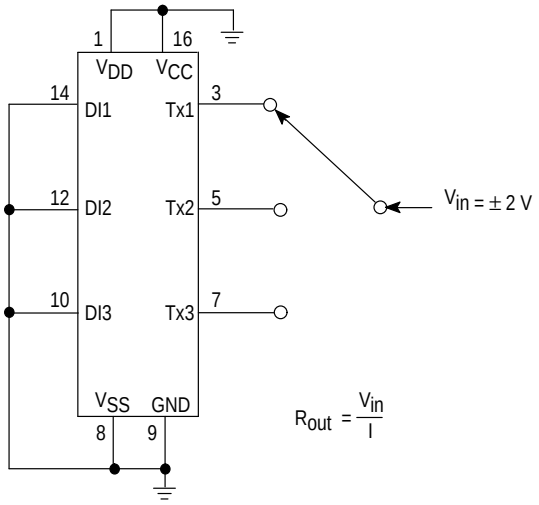


Figure 1. Power–Off Source Resistance (Drivers)

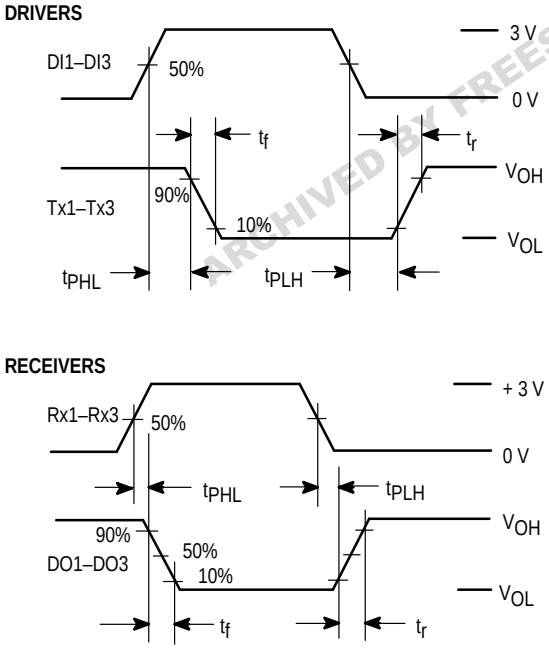


Figure 2. Switching Characteristics

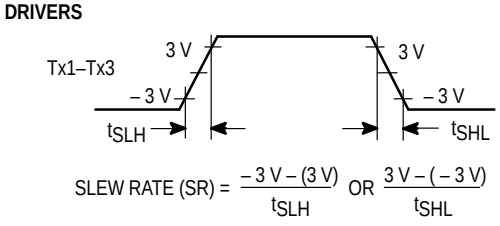


Figure 3. Slew–Rate Characterization

PIN DESCRIPTIONS

V_{DD}
Positive Power Supply (Pin 1)

The most positive power supply pin, which is typically + 5 to + 12 V.

V_{SS}
Negative Power Supply (Pin 8)

The most negative power supply pin, which is typically – 5 to – 12 V.

V_{CC}
Digital Power Supply (Pin 16)

The digital supply pin, which is connected to the logic power supply (maximum + 5.5 V). V_{CC} ***must*** be less than or equal to V_{DD}.

GND
Ground (Pin 9)

Ground return pin is typically connected to the signal ground pin of the EIA 232–E connector (Pin 7) as well as to the logic power supply ground.

Rx1, Rx2, Rx3
Receive Data Input (Pins 2, 4, 6)

These are the EIA 232–E receive signal inputs whose voltages can range from (V_{DD} + 15 V) to (V_{SS} – 15 V). A voltage between + 3 and (V_{DD} + 15 V) is decoded as a space and causes the corresponding DO pin to swing to ground (0 V); a voltage between – 3 and (V_{DD} – 15 V) is decoded as a mark and causes the DO pin to swing up to V_{CC}. The actual turn–on input switchpoint is typically biased at 1.8 V above ground, and includes 800 mV of hysteresis for noise rejection. The nominal input impedance is 5 kΩ. An open or grounded input pin is interpreted as a mark, forcing the DO pin to V_{CC}.

DO1, DO2, DO3
Data Output (Pins 11, 13, 15)

These are the receiver digital output pins, which swing from V_{CC} to GND. A space on the Rx pin causes DO to produce a logic 0; a mark produces a logic 1. Each output pin is capable of driving one LSTTL input load.

DI1, DI2, DI3
Data Input (Pins 10, 12,14)

These are the high–impedance digital input pins to the drivers. TTL compatibility is accomplished by biasing the input switchpoint at 1.4 V above GND. However, 5–V CMOS compatibility is maintained as well. Input voltage levels on these pins must be between V_{CC} and GND.

Tx1, Tx2, Tx3
Transmit Data Output (Pins 3, 5, 7)

These are the EIA 232–E transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic 1 at a DI input causes the corresponding Tx output to swing toward V_{SS}. A logic 0 causes the output to swing toward V_{DD} (the output voltages will be slightly less than V_{DD} or V_{SS} depending upon the output load). Output slew rates are limited to a maximum of 30 V per μs. When the MC145406 is off (V_{DD} = V_{SS} = V_{CC} = GND), the minimum output impedance is 300 Ω.

APPLICATIONS INFORMATION

The MC145406 has been designed to meet the electrical specifications of standards EIA 232–E and CCITT V.28. EIA 232–E defines the electrical and physical interface between Data Communication Equipment (DCE) and Data Terminal Equipment (DTE). A DCE is connected to a DTE using a cable that typically carries up to 25 leads. These leads, referred to as interchange circuits, allow the transfer of timing, data, control, and test signals. Electrically this transfer requires level shifting between the TTL/CMOS logic levels of the computer or modem and the high voltage levels of EIA 232–E, which can range from ± 3 to ± 25 V. The MC145406 provides the necessary level shifting as well as meeting other aspects of the EIA 232–E specification.

DRIVERS

As defined by the specification, an EIA 232–E driver presents a voltage of between ± 5 to ± 15 V into a load of between 3 to 7 kΩ. A logic 1 at the driver input results in a voltage of between – 5 to – 15 V. A logic 0 results in a voltage between + 5 to + 15 V. When operating V_{DD} and V_{SS} at ± 7 to ± 12 V, the MC145406 meets this requirement. When operating at ± 5 V, the MC145406 drivers produce less than ± 5 V at the output (when terminated), which does not meet EIA 232–E specification. However, the output voltages when using a ± 5 V power supply are high enough (around ± 4 V) to permit proper reception by an EIA 232–E receiver, and can be used in applications where strict compliance to EIA 232–E is not required.

Another requirement of the MC145406 drivers is that they withstand a short to another driver in the EIA 232–E cable. The worst–case condition that is permitted by EIA 232–E is a ± 15 V source that is current limited to 500 mA. The MC145406 drivers can withstand this condition momentarily. In most short circuit conditions the source driver will have a series 300 Ω output impedance needed to satisfy the EIA 232–E driver requirements. This will reduce the short circuit current to under 40 mA which is an acceptable level for the MC145406 to withstand.

Unlike some other drivers, the MC145406 drivers feature an internally–limited output slew–rate that does not exceed 30 V per μs.

RECEIVERS

The job of an EIA 232–E receiver is to level–shift voltages in the range of – 25 to + 25 V down to TTL/CMOS logic levels (0 to + 5 V). A voltage of between – 3 and – 25 V on Rx1 is defined as a mark and produces a logic 1 at DO1. A voltage between + 3 and + 25 V is a space and produces a logic zero. While receiving these signals, the Rx inputs must present a resistance between 3 and 7 kΩ. Nominally, the input resistance of the Rx1–Rx3 inputs is 5.4 kΩ.

The input threshold of the Rx1–Rx3 inputs is typically biased at 1.8 V above ground (GND) with typically 800 mV of hysteresis included to improve noise immunity. The 1.8 V bias forces the appropriate DO pin to a logic 1 when its Rx input is open or grounded as called for in the EIA 232–E specification. Notice that TTL logic levels can be applied to the Rx inputs in lieu of normal EIA 232–E signal levels. This might be helpful in situations where access to the modem or computer through the EIA 232–E connector is necessary with TTL devices. However, it is important not to connect the EIA 232–E outputs (Tx1–Tx3) to TTL inputs since TTL operates off + 5 V only, and may be damaged by the high output voltage of the MC145406.

The DO outputs are to be connected to a TTL or CMOS input (such as an input to a modem chip). These outputs will swing from V_{CC} to ground, allowing the designer to operate the DO and DI pins from digital power supply. The Tx and Rx sections are independently powered by V_{DD} and V_{SS} so that one may run logic at + 5 V and the EIA 232–E signals at ± 12 V.

POWER SUPPLY CONSIDERATIONS

Figure 4 shows a technique to guard against excessive device current.

The diode D1 prevents excessive current from flowing through an internal diode from the V_{CC} pin to the V_{DD} pin when $V_{DD} < V_{CC}$ by approximately 0.6 V. This high current condition can exist for a short period of time during power up/down. Additionally, if the + 12 V supply is switched off while the + 5 V is on and the off supply is a low impedance to ground, the diode D1 will prevent current flow through the internal diode.

The diode D2 is used as a voltage clamp, to prevent V_{SS} from drifting positive to V_{CC}, in the event that power is removed from V_{SS} (Pin 12). If V_{SS} power is removed, and the impedance from the V_{SS} pin to ground is greater than approximately 3 kΩ, this pin will be pulled to V_{CC} by internal circuitry causing excessive current in the V_{CC} pin.

If by design, neither of the above conditions are allowed to exist, then the diodes D1 and D2 are not required.

ESD PROTECTION

ESD protection on IC devices that have their pins accessible to the outside world is essential. High static voltages applied to the pins when someone touches them either directly or indirectly can cause damage to gate oxides and transistor junctions by coupling a portion of the energy from the I/O pin to the power supply buses of the IC. This coupling will usually occur through the internal ESD protection diodes. The key to protecting the IC is to shunt as much of the energy to ground as possible before it enters the IC. Figure 4 shows a technique which will clamp the ESD voltage at approximately ± 15 V using the MMVZ15VDLT1. Any residual voltage which appears on the supply pins is shunted to ground through the capacitors C1–C3. This scheme has provided protection to the interface part up to ± 10 kV, using the human body model test.

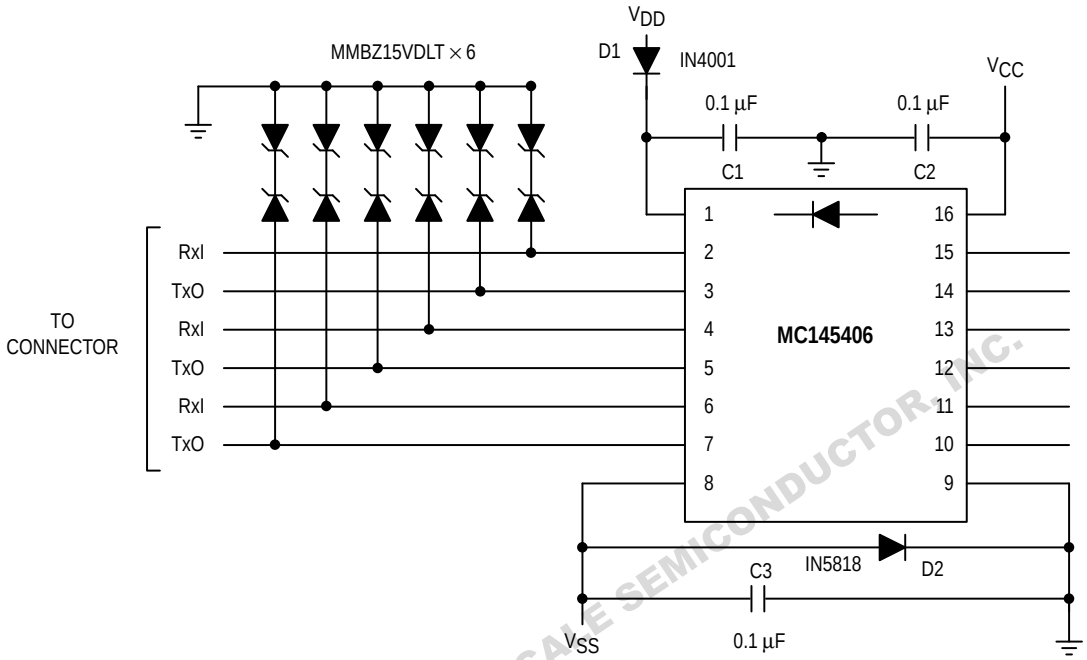
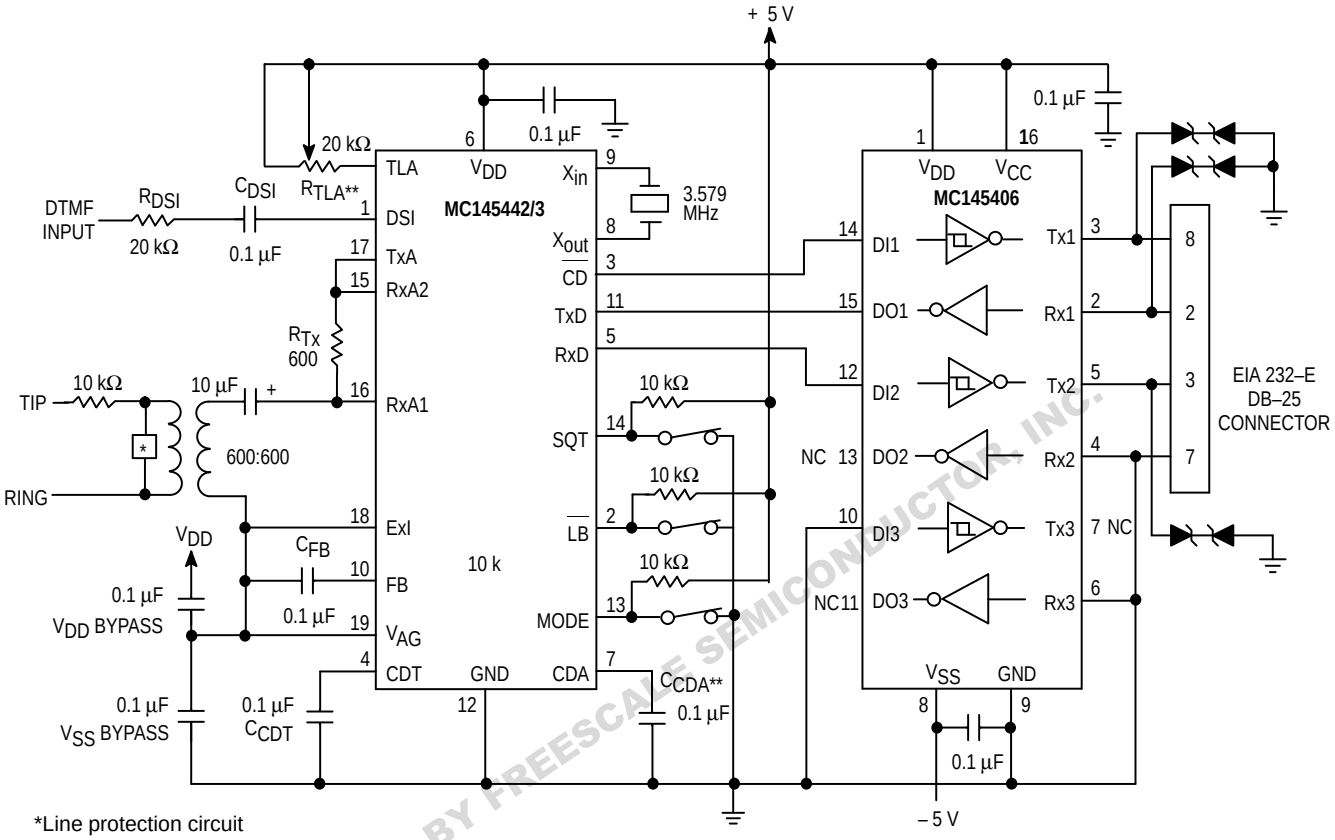


Figure 4. ESD and Power Supply Networks



*Line protection circuit

**Refer to the applications information for values of C_{CDA} and R_{TLA}

Figure 5. 5–V 300–Baud Modem with EIA 232–E Interface

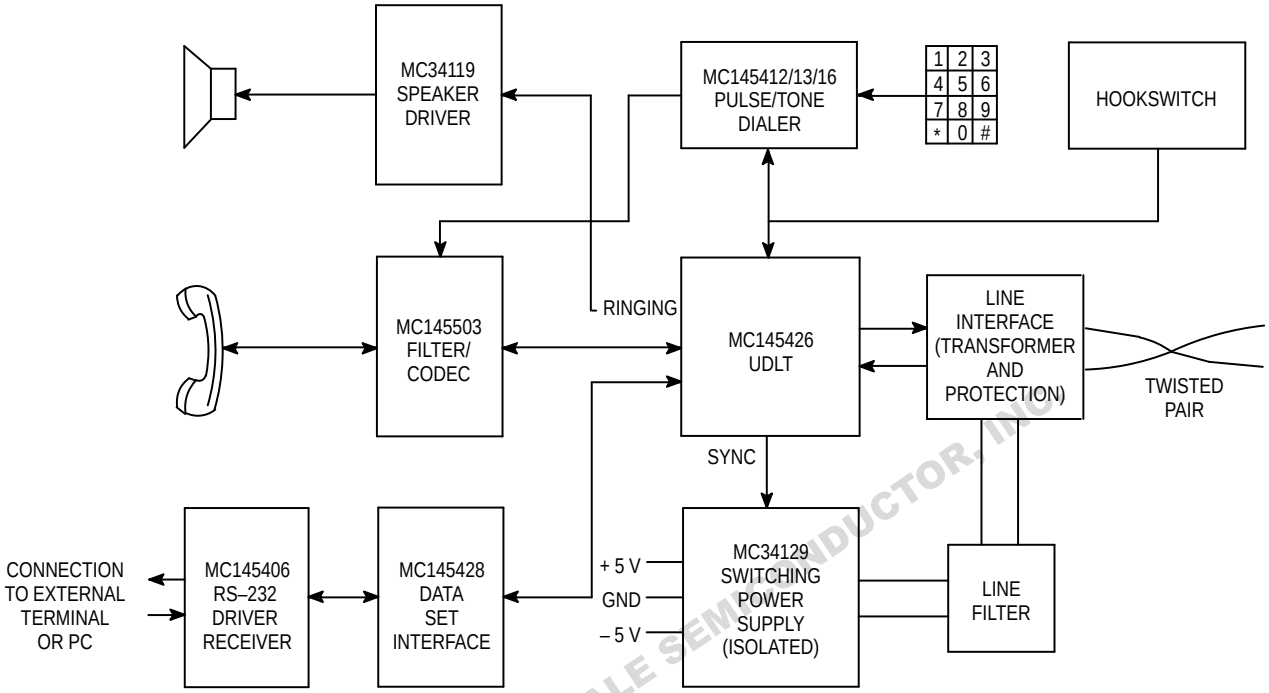


Figure 6. Line–Powered Voice/Data Telephone with Electrically Isolated EIA 232–E Interface

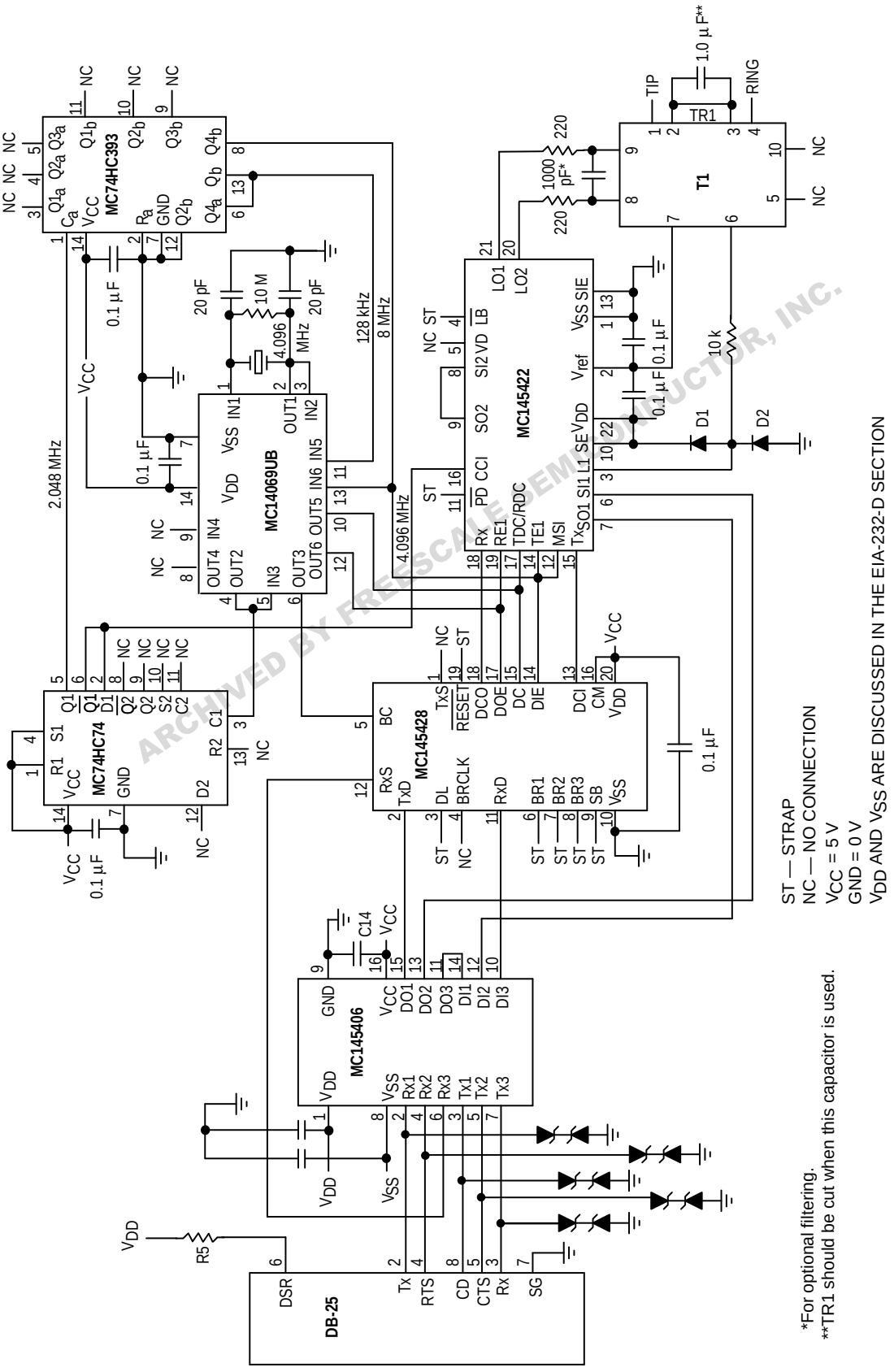
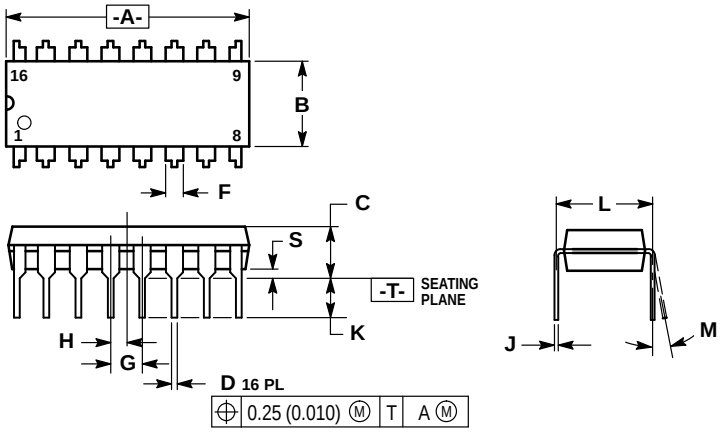


Figure 7. 80–kbps Limited Distance Modem with EIA 232–E Interface (Master)

PACKAGE DIMENSIONS

P SUFFIX
CASE 648–08



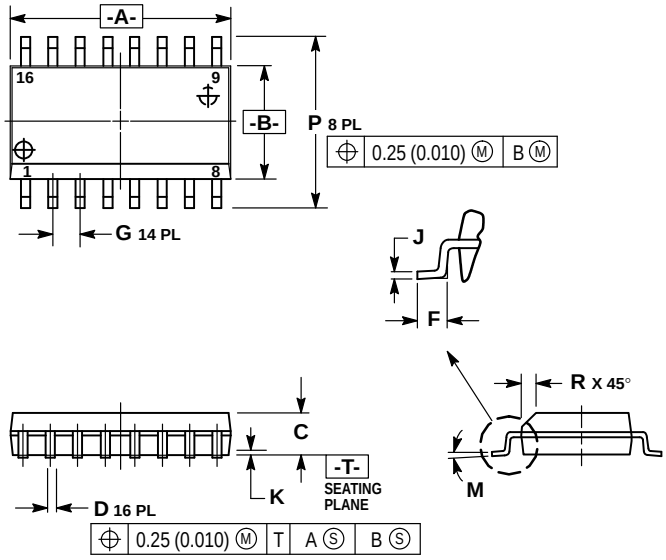
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

STYLE 1:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 2:
PIN 1. COMMON DRAIN
2. COMMON DRAIN
3. COMMON DRAIN
4. COMMON DRAIN
5. COMMON DRAIN
6. COMMON DRAIN
7. COMMON DRAIN
8. COMMON DRAIN
9. GATE
10. SOURCE
11. GATE
12. SOURCE
13. GATE
14. SOURCE
15. GATE
16. SOURCE

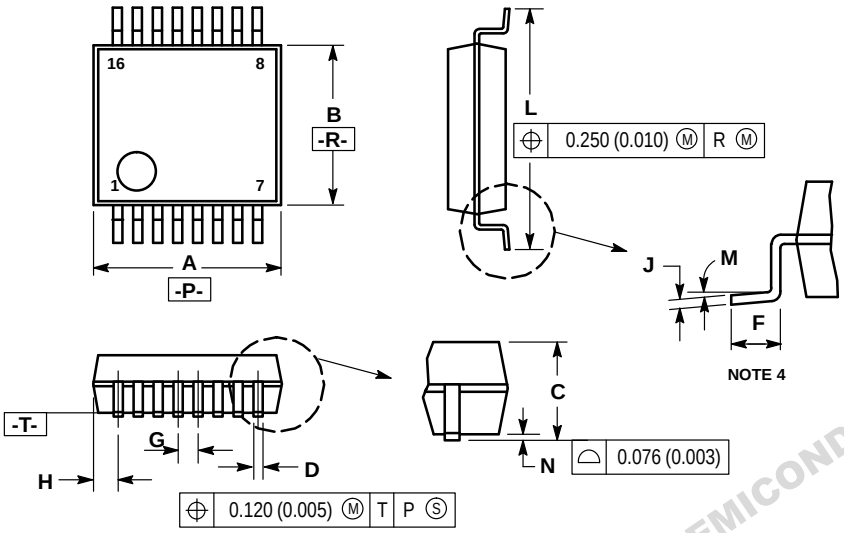
DW SUFFIX
CASE 751G–02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

SD SUFFIX
CASE 940B–02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
5. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
6. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.10	6.30	0.240	0.248
B	5.20	5.38	0.205	0.212
C	1.75	1.99	0.069	0.078
D	0.25	0.38	0.010	0.015
F	0.65	1.00	0.026	0.039
G	0.65 BSC		0.026 BSC	
H	0.73	0.90	0.029	0.035
J	0.10	0.20	0.004	0.008
L	7.65	7.90	0.301	0.311
M	0 °	8 °	0 °	8 °
N	0.05	0.21	0.002	0.008

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