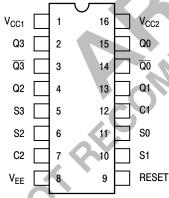
Bi-Quinary Counter

The MC10138 is a four bit counter capable of divide by two, five, or ten functions. It is composed of four set—reset master—slave flip—flops. Clock inputs trigger on the positive going edge of the clock pulse.

Set or reset input override the clock, allowing asynchronous "set" or "clear." Individual set and common reset inputs are provided, as well as complementary outputs for the first and fourth bits.

- $P_D = 370 \text{ mW typ/pkg (No Load)}$
- $f_{tog} = 150 \text{ MHz typ}$
- t_r , $t_f = 2.5$ ns typ (20%–80%)

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



http://onsemi.com

MARKING DIAGRAMS



CDIP-16 L SUFFIX CASE 620





PDIP-16 P SUFFIX CASE 648





PLCC-20 FN SUFFIX CASE 775



A = Assembly Location

WL = Wafer Lot YY = Year WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10138L	CDIP-16	25 Units / Rail
MC10138P	PDIP-16	25 Units / Rail
MC10138FN	PLCC-20	46 Units / Rail

COUNTER TRUTH TABLES

BI-QUINARY

(Clock connected to C2 and $\overline{Q3}$ connected to C1)

BCD	
connecte	•

(Clock connected to C1 and $\overline{Q0}$ connected to C2)

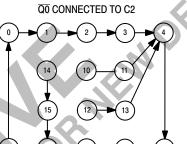
COUNT	Q1	Q2	Q3	Q0			
0	L	L	L	L			
1	Н	L	L	L			
2	L	Н	L	L			
3	Н	Н	L	L			
4	L	L	Н	L			
5	L	L	L	Н			
6	Н	L	L	Н			
7	L	Н	L	Н			
8	Н	Н	L	Н			
9	L	L	Н	Н			

COUNT	Q0	Q1	Q2	Q3
0	L	L	L	L
1	Н	L	L	L
2	L	Н	L	L
3	Н	Н	L	L
4	L	L	Н	L
5	Н	L	Н	L
6	L	Н	Н	L
7	Н	Н	Н	L
8	L	L	L	Н
9	Н	L	L	Н

COUNTER STATE DIAGRAM — POSITIVE LOGIC







ELECTRICAL CHARACTERISTICS

			Test Limits							
		Pin Under	-30)°C		+25°C		+85	5°C	
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit
Power Supply Drain Current	Ι _Ε	8		97		70	88		97	mAdc
Input Current	l _{inH}	12 5,6,10,11 7 9		350 390 460 650			220 245 290 410		220 245 290	μAdc
	I _{inL}	All	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V _{OH}	3,14 (3.) 2,4,13,15 (2.)	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960		-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc
Output Voltage Logic 0	V _{OL}	3,14 (2.) 2,4,13,15 (3.)	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850		-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc
Threshold Voltage Logic 1	V _{OHA}	2,4,13,15 (2.) 3,14 (3.) 13,15 (2.)	-1.080 -1.080 -1.080		-0.980 -0.980 -0.980			-0.910 -0.910 -0.910	S	Vdc
Threshold Voltage Logic 0	V _{OLA}	2,4,13,15 (3.) 3,14 (2.) 13,15 (3.)		-1.655 -1.655 -1.655			-1.630 -1.630 -1.630		-1.595 -1.595 -1.595	Vdc
Switching Times (50 Ω Load)										ns
Propagation Clock Delays Delay	t ₁₂₊₁₅₊ t ₁₂₊₁₄₊ t ₇₊₁₃₊ t ₇₊₄₊ t ₇₊₂₊ t ₇₊₃₊ t ₁₂₊₁₅₋ t ₁₂₊₁₄₋ t ₇₊₁₃₋ t ₇₊₄₋ t ₇₊₂₋	15 14 13 4 2 3 15 14 13 4	1.4 1.4 1.4 1.4 1.4 1.4 1.4 1.4 1.4	5.0 5.0 5.2 5.2 5.2 5.2 5.0 5.0 5.2 5.2 5.2	1.5 1.5 1.5 1.5 1.5 1.5 1.5 1.5 1.5	3.5 3.5 3.5 3.5 3.5 3.5 3.5 3.5 3.5 3.5	4.8 4.8 5.0 5.0 5.0 4.8 4.8 5.0 5.0	1.5 1.5 1.5 1.5 1.5 1.5 1.5 1.5	5.3 5.5 5.5 5.5 5.5 5.3 5.3 5.5 5.5 5.5	
Set Delay	t ₇₊₃₋ t ₁₁₊₁₅₊ t ₁₁₊₁₄₋	3 15 14	1.4 1.4 1.4	5.2 5.2 5.2	1.5 1.5 1.5	3.5	5.0 5.0 5.0	1.5 1.5 1.5	5.5 5.5 5.5	
Reset Delay	t ₉₊₁₄₊ t ₉₊₁₅₋	14 15	1.4 1.4	5.2 5.2	1.5 1.5		5.0 5.0	1.5 1.5	5.5 5.5	
Rise Time (20 to 80%)	t ₁₄₊ t ₁₅₊	14 15	1.1 1.1	4.7 4.7	1.1 1.1	2.5 2.5	4.5 4.5	1.1 1.1	5.0 5.0	
Fall Time (20 to 80%)	t ₁₄₋ t ₁₅₋	14 15	1.1 1.1	4.7 4.7	1.1 1.1	2.5 2.5	4.5 4.5	1.1 1.1	5.0 5.0	
Counting Frequency	f _{count}	2 15	125 125		125 125	150 150		125 125		MHz

Individually test each input; apply V_{ILmin} to pin under test.

Set all four flip–flops by applying pulse
 V_{IHmax} to pins 5, 6, 10, and 11 prior to applying test voltage indicated.
 Reset all four flip–flops by applying pulse
 V_{ILmin} to pin 9 prior to applying test voltage indicated.

ELECTRICAL CHARACTERISTICS (continued)

NOTE: Each MECL 10,000 series circuit has been designed to meet the dc specifications			TEST VOLTAGE VALUES (Volts)					
shown in the test table, after thermal equilibrium has been established. The circuit	@ Test	Temperature	V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}	
is in a test socket or mounted on a printed circuit board and transverse air flow greater		-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	
than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one	+25°C		-0.810	-1.850	-1.105	-1.475	-5.2	
gate. The other gates are tested in the same manner.		+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	
		Pin	TEST V	OLTAGE AP	PLIED TO P	INS LISTED	BELOW	
Characteristic	Symbol	Under Test	V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}	(V _{CC}) Gnd
Power Supply Drain Current	Ι _Ε	8	9				8	1, 16
Input Current	l _{inH}	12 5,6,10,11 7 9	12 5,6,10,11 7 9				8 8 8	1, 16 1, 16 1, 16 1, 16
	I _{inL}	All		Note 1.			8	1, 16
Output Voltage Logic 1	V _{OH}	3,14 (3.) 2,4,13,15 (2.)	9 5,6,10,11				8 8	1, 16 1, 16
Output Voltage Logic 0	V _{OL}	3,14 (2.) 2,4,13,15 (3.)	5,6,10,11 9			la.	8 8	1, 16 1, 16
Threshold Voltage Logic 1	V _{OHA}	2,4,13,15 (2.) 3,14 (3.) 13,15 (2.)			5,6,10,11 9 7,12		8 8 8	1, 16 1, 16 1, 16
Threshold Voltage Logic 0	V _{OLA}	2,4,13,15 (3.) 3,14 (2.) 13,15 (3.)			OP-	5,6,10,11 9 7,12	8 8 8	1, 16 1, 16 1, 16
Switching Times (50Ω Load)				7 4	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay Clock Delays	t ₁₂₊₁₅₊ t ₁₂₊₁₄₊ t ₇₊₁₃₊ t ₇₊₄₊ t ₇₊₂₊ t ₇₊₃₊ t ₁₂₊₁₅₋ t ₁₂₊₁₄₋ t ₇₊₁₃₋ t ₇₊₄₋ t ₇₊₃₋	15 14 13 4 2 3 15 14 13 4 2 3			12 12 7 7 7 7 12 12 12 7 7	15 14 13 4 2 3 15 14 13 4 2 3	8 8 8 8 8 8 8 8	1, 16 1, 16 1, 16 1, 16 1, 16 1, 16 1, 16 1, 16 1, 16 1, 16 1, 16 1, 16 1, 16
Set Delay	t ₁₁₊₁₅₊ t ₁₁₊₁₄₋	15 14			11 11	15 14	8 8	1, 16 1, 16
Reset Delay	t ₉₊₁₄₊ t ₉₊₁₅₋	14 15			9 9	14 15	8 8	1, 16 1, 16
Rise Time (20 to 80%)	t ₁₄₊ t ₁₅₊	14 15			11 11	14 15	8 8	1, 16 1, 16
Fall Time (20 to 80%)	t ₁₄₋ t ₁₅₋	14 15			9 9	14 15	8 8	1, 16 1, 16
Counting Frequency	f _{count}	2 15			7 12	2 15	8 8	1, 16 1, 16

1.	Individually	test each	input ar	nlv V u mir	to pin	under tes	t.

Set all four flip–flops by applying pulse
 V_{IHmax}
 V_{ILmin}
 V_{IHmax}
 V_{ILmin}
 V_{IHmax}

to pins 5, 6, 10, and 11 prior to applying test voltage indicated.

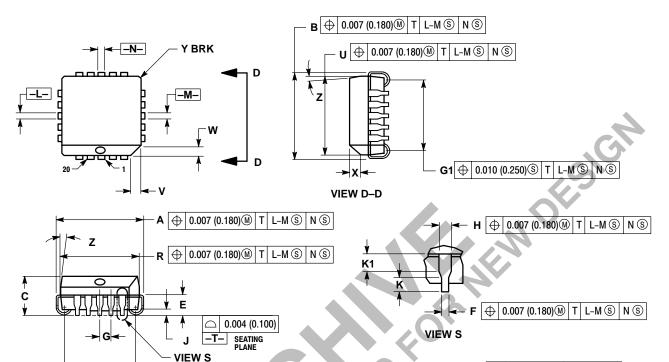
3. Reset all four flip–flops by applying pulse $V_{\rm IHmax}$ $V_{\rm ILmin}$

to pin 9 prior to applying test voltage indicated.

PACKAGE DIMENSIONS

PLCC-20 **FN SUFFIX**

PLASTIC PLCC PACKAGE CASE 775-02 ISSUE C



NOTES:

- OTES:

 1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.

 2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.

 3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.

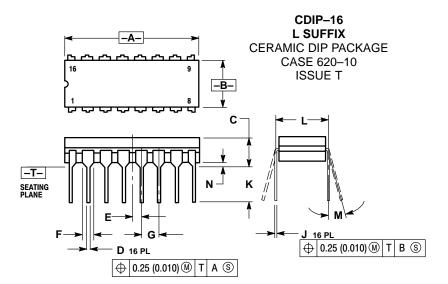
 4. DIMENSIONING AND TOLERANCING PER ANSI V14 5M 1982
- Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INC	HES	MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	0.385	0.395	9.78	10.03
В	0.385	0.395	9.78	10.03
С	0.165	0.180	4.20	4.57
Е	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050	BSC	1.27	BSC
Н	0.026	0.032	0.66	0.81
J	0.020		0.51	
K	0.025		0.64	
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
٧	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
Х	0.042	0.056	1.07	1.42
Υ		0.020		0.50
Z	2°	10°	2°	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040		1.02	

G1 ⊕ 0.010 (0.250)③ T L-M ⑤ N ⑤

OENICE NOT RECO

PACKAGE DIMENSIONS



NOTES:

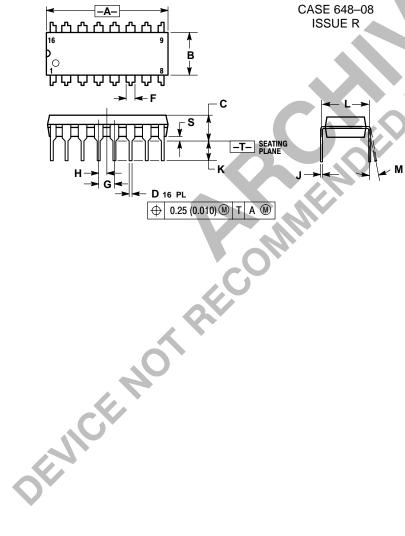
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: INCH.
 DIMENSION LTO CENTER OF LEAD WHEN CONTROLLING DIMENSION LTO CENTER OF LEAD WHEN

- FORMED PARALLEL

 DIMENSION F MAY NARROW TO 0.76 (0.030)
 WHERE THE LEAD ENTERS THE CERAMIC
 BODY.

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.750	0.785	19.05	19.93	
В	0.240	0.295	6.10	7.49	
C		0.200		5.08	
D	0.015	0.020	0.39	0.50	
E	0.050	BSC	1.27 BSC		
F	0.055	0.065	1.40	1.65	
G	0.100	BSC	2.54 BSC		
Н	0.008	0.015	0.21	0.38	
K	0.125	0.170	3.18	4.31	
L	0.300	BSC	7.62	BSC	
M	0 °	15°	0 °	15°	
N	0.020	0.040	0.51	1.01	





- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
С	0.145	0.175	3.69	4.44	
D	0.015	0.021	0.39	0.53	
F	0.040	0.70	1.02	1.77	
G	0.100	BSC	2.54 BSC		
Н	0.050	BSC	1.27	BSC	
J	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
L	0.295	0.305	7.50	7.74	
M	0°	10°	0°	10 °	
S	0.020	0.040	0.51	1.01	

Notes





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