MOTOROLA

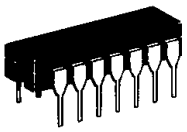
MC4344
MC4044

PHASE-FREQUENCY DETECTOR

The MC4344/4044 consists of two digital phase detectors, a charge pump, and an amplifier. In combination with a voltage controlled multivibrator (such as the MC4324/4024 or MC1648), it is useful in a broad range of phase-locked loop applications. The circuit accepts TTL waveforms at the R and V inputs and generates an error voltage that is proportional to the frequency and/or phase difference of the input signals. Phase detector #1 is intended for use in systems requiring zero frequency and phase difference at lock. Phase detector #2 is used if quadrature lock is desired. Phase detector #2 can also be used to indicate that the main loop, utilizing phase detector #1, is out of lock.

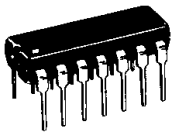
Operating Frequency = 8 MHz typ
Input Loading Factor: R, V = 3
Output Loading Factor (Pin 8) = 10
Total Power Dissipation = 85 mW typ/pkg
Propagation Delay Time = 9.0 ns typ
(thru phase detector)

PHASE-FREQUENCY DETECTOR

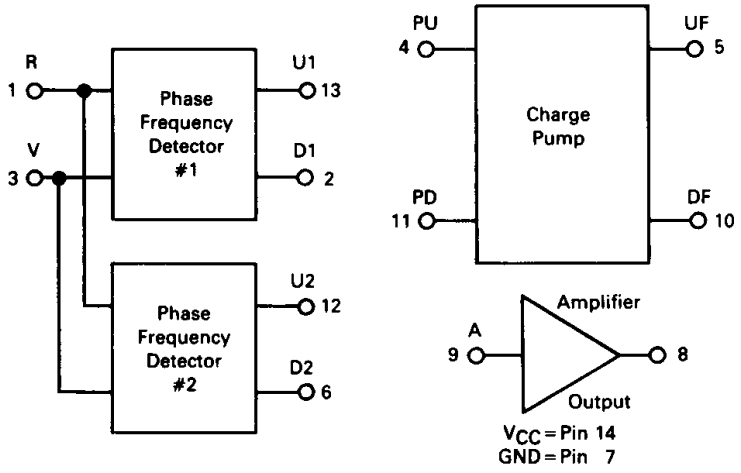


L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)

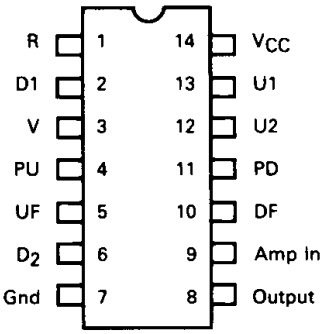
P SUFFIX
PLASTIC PACKAGE
CASE 646
MC4044 only



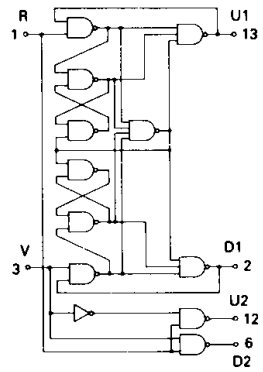
LOGIC DIAGRAM



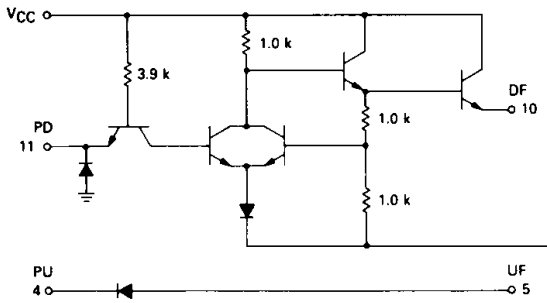
PIN ASSIGNMENT



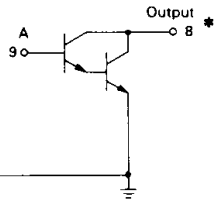
PHASE DETECTOR



CHARGE PUMP



AMPLIFIER



*V_{MAX} not to exceed 8.0 Vdc.

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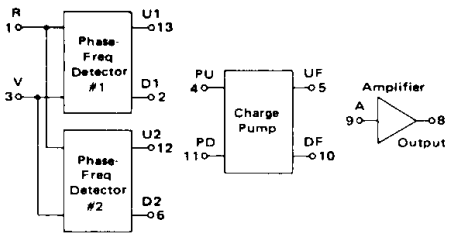
ELECTRICAL CHARACTERISTICS



INPUT STATE	INPUT R	INPUT V	OUTPUT U1	OUTPUT D1	OUTPUT U2	OUTPUT D2
1	0	0	X	X	1	1
2	1	0	X	X	0	1
3	1	1	X	X	1	0
4	1	0	X	X	0	1
5	0	0	X	X	1	1
6	1	0	X	X	0	1
7	0	0	0	1	1	1
8	1	0	0	1	0	1
9	0	0	0	1	1	1
10	0	1	0	1	1	1
11	0	0	1	1	1	1
12	0	1	1	1	1	1
13	0	0	1	0	1	1
14	0	1	1	0	1	1
15	0	0	1	0	1	1
16	1	0	1	0	0	1
17	0	0	1	1	1	1

TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not show all possible modes of operation. It is useful for dc testing.

1. X indicates output state unknown.
2. U1 and D1 outputs are sequential; i.e., they must be sequenced in order shown.
3. U2 and D2 outputs are combinational; i.e., they need only inputs shown to obtain outputs.

	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL}	I_{OH1}	I_{OH2}	I_{in}	I_{IC}	I_A	Volts V_{IL}	V_{IH}	V_{IHH}	V_{ILT}	V_{IHT}	V_{out}	V_{CC}	V_{CCL}	V_{CCH}
MC4344	-55°C	20	-1.6	-1.0	–	–	0.002	0.4	2.4	–	1.1	2.0	1.5	5.0	4.5	5.5
MC4344	+25°C	20	-1.6	-1.0	1.0	-10	0.002	0.4	2.4	5.5	1.1	1.8	1.5	5.0	4.5	5.5
MC4344	+125°C	20	-1.6	-1.0	–	–	0.002	0.4	2.4	–	0.9	1.8	1.5	5.0	4.5	5.5
MC4044	0°C	20	-1.6	-1.0	–	–	0.002	0.4	2.5	–	1.1	2.0	1.5	5.0	4.75	5.25
MC4044	+25°C	20	-1.6	-1.0	1.0	-10	0.002	0.4	2.5	5.5	1.1	1.8	1.5	5.0	4.75	5.25
MC4044	+75°C	20	-1.6	-1.0	–	–	0.002	0.4	2.5	–	0.9	1.8	1.5	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC4344 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4044 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW I_{OL}	I_{OH1}	I_{OH2}	I_{in}	I_{IC}	I_A	V_{IL}	V_{IH}	V_{IHH}	V_{ILT}	V_{IHT}	V_{out}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																														
Forward Current	I_{IL}	1	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	mAdc	–	–	–	–	–	–	1	–	–	–				14	7
		3		-4.8		-4.8		-4.8		-4.8		-4.8		-4.8								3								
		11		-1.6		-1.6		-1.6		-1.6		-1.6		-1.6	↓							11							↓	↓
Leakage Current	I_{IH}	1		120	–	120	–	120	–	120	–	120	–	120	μAdc	–	–	–	–	–	–	–	1	–	–	–				14	7
		3		120	–	120	–	120	–	120	–	120	–	120		–	–	–	–	1	–		3	–	–	–				14	7
		4		5.0		5.0		5.0		5.0		5.0		5.0		–	–							–						4	5,7
		11		40	–	40		40		40		40		40	↓	–	–						11	–						14	7
	I_{IHH}	1				1.0						1.0			mAdc	–								1						14	7
		3				↓						↓												3							7
		11			–										↓									11						↓	↓
Clamp Voltage	V_{IC}	1	–	–	–	-1.5	–	–				-1.5			Vdc	–				1				–					14		7
		3				-1.5						-1.5			Vdc	–				3				–					14		7
Output (Note 1)																														
Output Voltage	V_{OH}	6	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		6								1.3				14		7
		12	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		12								1.3				14		7
		..																							3	1			14		7
	V_{OL}	6		0.4		0.4		0.4		0.4		0.4		0.4	Vdc	6										1.3			14		7
	V_{OH}	12	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		12									1.3			14		7
		..													Vdc										3	1			14		7
		..													Vdc										1.3				14		7
	V_{OH}	6	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		6								3	1			14		7
	V_{OL}	12		0.4		0.4		0.4		0.4		0.4		0.4	Vdc	12									3	1			14		7
		..																							1.3				14		7
		..																							3	1			14		7
	V_{OH}	2	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		2								1.3				13		7
	V_{OL}	13		0.4		0.4		0.4		0.4		0.4		0.4	Vdc	13									1.3				14		7
	V_{OH}	2	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		2								1	3			14		7
	V_{OL}	13		0.4		0.4		0.4		0.4		0.4		0.4	Vdc	13									1	3			14		7
	V_{OH}	2	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		2								1.3				14		7
		13	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		13								1.3				14		7
	V_{OH}	2	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		2								1	3			14		7
		13	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		13								1	3			14		7
	V_{OL}	2		0.4		0.4		0.4		0.4		0.4		0.4	Vdc	2									1.3				14		7
	V_{OH}	13	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		13								1.3				14		7
	V_{OL}	2		0.4		0.4		0.4		0.4		0.4		0.4	Vdc	2									1	3			14		7
	V_{OH}	13	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		13								1	3			14		7
	V_{OL}	2		0.4		0.4		0.4		0.4		0.4		0.4	Vdc	2									1.3				14		7
	V_{OH}	13	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		13								1.3				14		7
	V_{OL}	2		0.4		0.4		0.4		0.4		0.4		0.4	Vdc	2									3	1			14		7
	V_{OH}	13	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		13								3	1			14		7
	V_{OH}	2	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		2								1.3				14		7
		13	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		13								1.3				14		7
Short Circuit Current (Note 1)	I_{OS}	*2	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc															2,3,7,1
		6																												1,3,6,7
		12																												1,3,7,12
		*13																												1,3,7,13
Leakage Current (Note 1)	I_{OLK}	*2		250		250		250		250		250		250	μAdc																1,3,7
		6																									2,14			1,3,7
		12																									6,14			1,3,7
		*13																									12,14			1,3,7
																											13,14			
Diode Voltage	V_F	5			0.5						0.5				Vdc				5											4,7
Output Voltage	V_{EH}	10	1.5		1.5		1.5		1.5		1.5		1.5		Vdc			10						–	11				14		7
Output Current	I_O	8	0.2		0.8		1.0		0.5	–	0.8		1.0		mAdc	–				9										8	7
Leakage Current	I_{OLK}	8		120		120		120		120		120		120	μAdc									–						8	7,9
		10		5.0		5.0		5.0		5.0		5.0		5.0	μAdc	–						11		–			10			14	7
Power Requirements (Total Device) Power Supply Drain	I_{CC}	14	–	40		40		40	–	40		40		40	mAdc	–								–				14			7

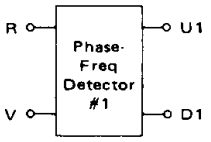
Note 1. The output state of Pin 2 or Pin 13 depends upon the sequence that has been applied to the R and V inputs as shown in the Truth Table. In testing output voltage, the outputs of the device are tested by sequencing through the indicated input states according to the Truth Table. Procedures identified by a double asterisk (**) are necessary to change the state of the sequential logic. When testing I_{OS} and I_{OLK} on Pins 2 or 13, a single asterisk (*) indicates that the R and V inputs are sequenced per the Truth Table to input state 11 where the tests are performed. All input, power supply, and ground voltages must be maintained while sequencing and testing unless otherwise noted.

APPLICATION

Operation of the MC4344/4044 is best explained by initially considering each section separately. If phase detector #1 is used, loop lockup occurs when both outputs U1 and D1 remain high. This occurs only when all the negative transitions on R, the reference input, and V, the variable or feedback input, coincide. The circuit responds only to transitions, hence phase error is independent of input waveform duty cycle or amplitude variation. Phase detector #1 consists of sequential logic circuitry, therefore operation prior to lockup is determined by initial conditions.

When operation is initiated, by either applying power to the circuit or active input signals to R and V, the circuitry can be in one of several states. Given any particular starting conditions, the flow table of Figure 1 can be used to determine subsequent operation. The flow table indicates the status of U1 and D1 as the R and V inputs are varied. The numbers in the table which are in parentheses are arbitrarily assigned labels that correspond to stable states that can result for each input combination. The numbers without parentheses refer to unstable conditions. Input changes are traced by horizontal movement in the table; after each input change, circuit operation will settle in the numbered state indicated by moving horizontally to the appropriate R-V column. If the number at that location is not in parentheses, move vertically to the number of the same value that is in parentheses. For a given input pair, any one of three stable states can exist. As an example, if R = 1 and V = 0, the circuit will be in one of the stable states (4), (8), or (12).

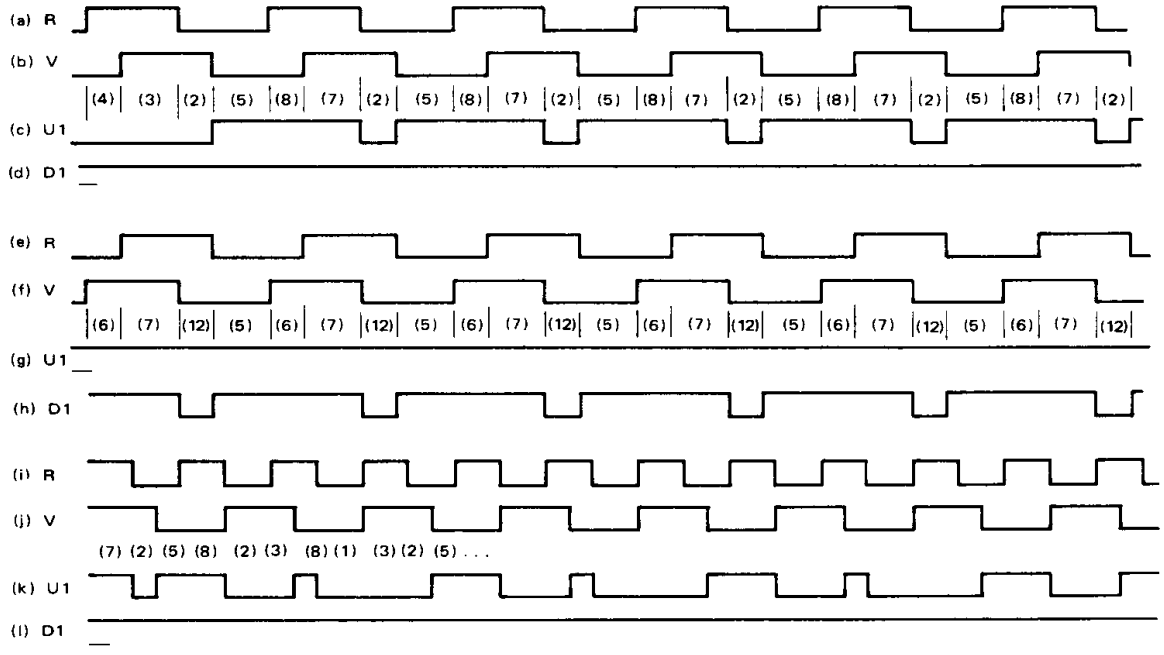
FIGURE 1 — PHASE DETECTOR #1 FLOW TABLE



R-V 0-0	R-V 0-1	R-V 1-1	R-V 1-0	U1	D1
(1)	2	3	(4)	0	1
5	(2)	(3)	8	0	1
(5)	6	7	8	1	1
9	(6)	7	12	1	1
5	2	(7)	12	1	1
5	2	7	(8)	1	1
(9)	(10)	11	12	1	0
5	6	(11)	(12)	1	0

Use of the table in determining circuit operation is illustrated in Figure 2. In the timing diagram, the input to R is the reference frequency; the input to V is the same frequency but lags in phase. Stable state (4) is arbitrarily assumed as the initial condition. From the timing diagram and flow table, when the circuit is in stable state (4), outputs U1 and D1 are "0" an "1" respectively. The next input state is R-V = 1-1; moving horizontally from stable state (4) under R-V = 1-0 to the R-V = 1-1 column, state 3 is indicated. However, this is an unstable condition and the circuit will assume the state indicated by moving vertically in the R-V = 1-1 column to stable state (3). In this

FIGURE 2 — PHASE DETECTOR #1 TIMING DIAGRAM



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instance, outputs U1 and D1 remain unchanged. The input states next become R-V = 0-1; moving horizontally to the R-V = 0-1 column, stable state (2) is indicated. At this point there is still no change in U1 or D1. The next input change shifts operation to the R-V = 0-0 column where unstable state 5 is indicated. Moving vertically to stable state (5), the outputs now change state to U1-D1 = 1-1. The next input change, R-V = 1-0, drives the circuitry to stable state (8), with no change in U1 or D1. The next input, R-V = 1-1, leads to stable state (7) with no change in the outputs. The next two input state changes cause U1 to go low between the negative transitions of R and V. As the inputs continue to change, the circuitry moves repeatedly through stable states (2), (5), (8), (7), (2), etc., as shown, and a periodic waveform is obtained on the U1 terminal while D1 remains high.

A similar result is obtained if V is leading with respect to R, except that the periodic waveform now appears on D1 as shown in rows e–h of the timing diagram of Figure 2. In each case, the average value of the resulting waveform is proportional to the phase difference between the two inputs. In a closed loop application, the error signal for controlling the VCO is derived by translating and filtering these waveforms.

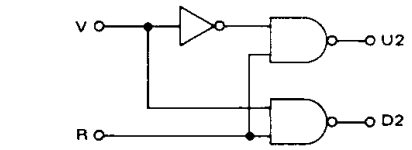
The results obtained when R and V are separated by a fixed frequency difference are indicated in rows i–l of the timing system. For this case, the U1 output goes low when R goes low and stays in that state until a negative transition on V occurs. The resulting waveform is similar to the fixed phase difference case, but now the duty cycle of the U1 waveform varies at a rate proportional to the difference frequency of the two inputs, R and V. It is this characteristic that permits the MC4344/4044 to be used as a frequency discriminator; if the signal on R has been frequency modulated and if the loop bandwidth is selected to pass the deviation frequency but reject R and V, the resulting error voltage applied to the VCO will be the recovered modulation signal.

Phase detector #2 consists only of combinatorial logic, therefore its characteristics can be determined from the simple truth table of Figure 3. Since circuit operation requires that both inputs to the charge pump either be high or have the same duty cycle when lock occurs, using this phase detector leads to a quadrature relationship between R and V. This is illustrated in rows a–d of the timing diagram of Figure 3. Note that any deviation from a fifty percent duty cycle on the inputs would appear as phase error.

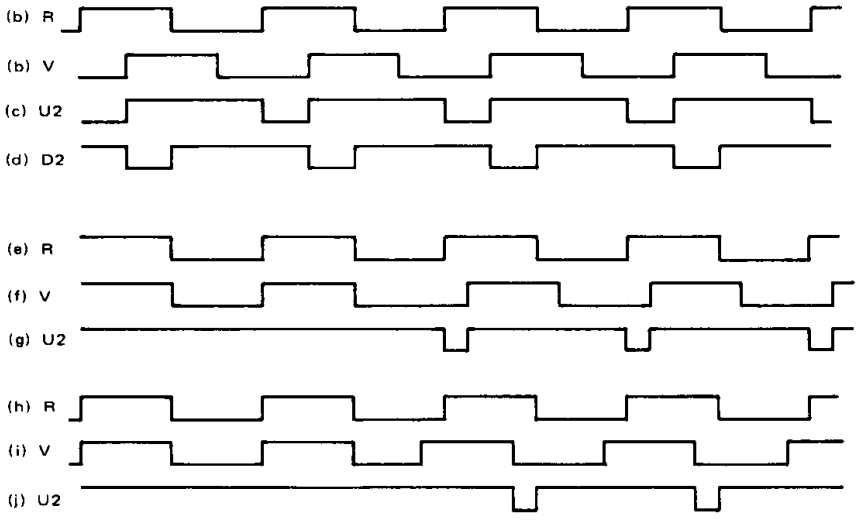
Waveforms showing the operation of phase detector #2 when phase detector #1 is being used in a closed loop are indicated in rows e–j. When the main loop is locked, U2 remains high. If the loop drifts out of lock in either direction a negative pulse whose width is proportional to the amount of drift appears on U2. This can be used to generate a simple loss-of-lock indicator.

Operation of the charge pump is best explained by considering it in conjunction with the Darlington amplifier included in the package (see Figure 4). There will be

FIGURE 3 — PHASE DETECTOR #2 OPERATION



R	V	U2	D2
0	0	1	1
0	1	1	1
1	0	0	1
1	1	1	0



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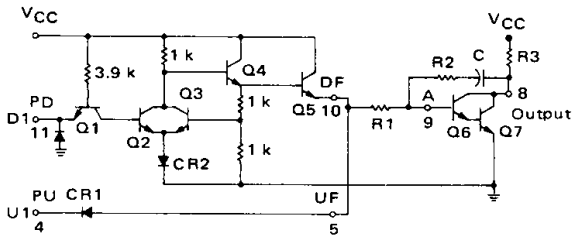
a pulsed waveform on either PD or PU, depending on the phase-frequency relationship of R and V. The charge pump serves to invert one of the input waveforms (D1) and translates the voltage levels before they are applied to the loop filter. When PD is low and PU is high, Q1 will be conducting in the normal direction and Q2 will be off. Current will be flowing through Q3 and CR2; the base of Q3 will be two V_{BE} drops above ground or approximately 1.5 volts. Since both of the resistors connected to the base of Q3 are equal, the emitter of Q4 (base of Q5) will be approximately 3.0 volts. For this condition, the emitter of Q5 (DF) will be on V_{BE} below this voltage, or about 2.25 volts. The PU input to the charge pump is high (> 2.4 volts) and CR1 will be reverse biased. Therefore Q5 will be supplying current to Q6. This will tend to lower the voltage at the collector of Q7, resulting in an error signal that lowers the VCO frequency as required by a "pump down" signal.

FIGURE 4 — CHARGE PUMP OPERATION

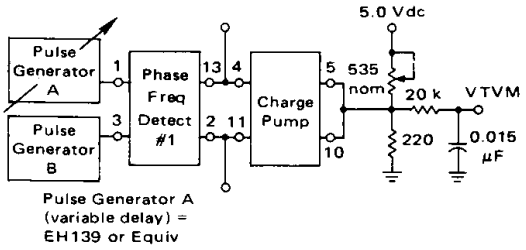


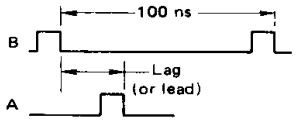
When PU is low and PD is high, CR1 is forward biased and UF will be approximately one V_{BE} above ground (neglecting the $V_{CE(sat)}$ of the driving gate). With PD high, Q1 conducts in the reverse direction, supplying base current for Q2. While Q2 is conducting, Q4 is prevented from supplying base drive to Q5; with Q5 cut off and UF low there is no base current for Q6 and the voltage at the collector of Q7 moves up, resulting in an increase in the VCO operating frequency as required by a "pump up" signal.

If both inputs to the charge pump are high (zero phase difference), both CR1 and the base-emitter junction of Q5 are reverse biased and there is no tendency for the error voltage to change. The output of the charge pump varies between one V_{BE} and three V_{BE} as the phase difference of R and V varies from minus 2π to plus 2π. If this signal is filtered to remove the high-frequency components, the phase detector transfer function, K_ϕ, of approximately 0.12 volt/radian is obtained (see Figure 5).

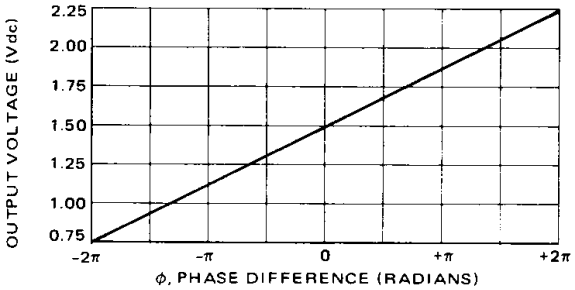
The specified gain constant of 0.12 volt/radian may not be obtained if the amplifier/filter combination is improperly designed. As indicated previously, the charge pump delivers pump commands of about 2.25 volts on the positive swings and 0.75 volt on the negative swings for a mean no-pump value of 1.5 volts. If the filter amplifier is biased to threshold "on" at 1.5 volts, then the pump up and down voltages have equal effects. The pump signals are established by V_{BE}s of transistors with milliamperes of current flowing. On the other hand, the transistors included for use as a filter amplifier will have very small currents flowing and will have correspondingly lower V_{BE}s — on the order of 0.6 volt each for a threshold of 1.2 volts. Any displacement of the threshold from 1.5 volts causes an increase in gain in one direction and a reduction in the other. The transistor configuration provided is hence not optimum but does allow for the use of an additional transistor to improve filter response. This addition also results in a non-symmetrical response since the threshold is now approximately 1.8 volts. The effective positive swing is limited to 0.45 volt while the negative swing below threshold can be greater than 1.0 volt. This means that the loop gain when changing from a high frequency to a lower frequency is less than when changing in the opposite direction. For type two loops this tends to increase overshoot when going from low to high and increases damping in the other direction. These problems and the selection of external filter components are intimately related to system requirements and are discussed in detail in the filter design section.

FIGURE 5 — PHASE DETECTOR TEST





Shown for positive phase angle. Reverse A and B for negative phase angle.



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PHASE-LOCKED LOOP COMPONENTS

General

A basic phase-locked loop, when operating properly, will acquire ("lock on") an input signal, track it in frequency, and exhibit a fixed phase relationship relative to the input. In this basic loop, the output frequency will be identical to the input frequency (Figure 6). A fundamental loop consists of a phase detector, amplifier/filter, and voltage-controlled oscillator (Figure 7). It appears and acts like a unity gain feedback loop. The controlled variable is phase; any error between f_{in} and f_{out} is amplified and applied to the VCO in a corrective direction.

FIGURE 6 — BASIC PHASE-LOCKED LOOP FREQUENCY RELATIONSHIP

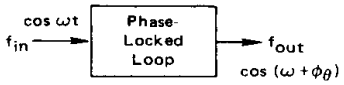
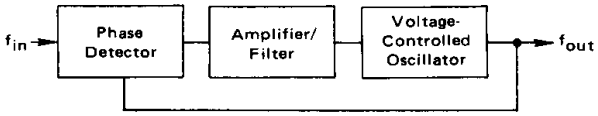


FIGURE 7 — FUNDAMENTAL PHASE-LOCKED LOOP



Simple phase detectors in digital phase-locked loops usually put out a series of pulses. The average value of these pulses is the "gain constant," K_ϕ, of the phase detector — the volts out for a given phase difference, expressed as volts/radian.

The VCO is designed so that its output frequency range is equal to or greater than the required output frequency range of the system. The ratio of change in output frequency to input control voltage is called "gain constant," K_O. If the slope of f_{out} to V_{in} is not linear (i.e., changes greater than 25%) over the expected frequency range, the curve should be piece-wise approximated and the appropriate constant applied for "best" and "worst" case analysis of loop performance.

System dynamics when in lock are determined by the amplifier/filter block. Its gain determines how much phase error exists between f_{in} and f_{out}, and filter characteristics shape the capture range and transient performance. This will be discussed in detail later.

Loop Filter

Fundamental loop characteristics such as capture range, loop bandwidth, capture time, and transient response are controlled primarily by the loop filter. The loop behavior is described by gains in each component block of Figure 8. The output to input ratio reflects a second order low pass filter in frequency response with a static gain of N:

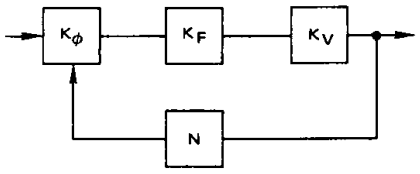
$$\frac{\theta_O(s)}{\theta_i(s)} = \frac{K_\phi K_F K_V}{s + \frac{K_\phi K_F K_V}{N}} \quad (1)$$

where: $K_F = \frac{1 + T_1 s}{T_2 s}$ (2)

$T_1 = R_2C$ and $T_2 = R_1C$ of Figure 4. Therefore,

$$\frac{\theta_O(s)}{\theta_i(s)} = \frac{N(1 + T_1 s)}{\frac{s^2 N T_2}{K_\phi K_V} + T_1 s + 1} \quad (3)$$

FIGURE 8 — GAIN CONSTANTS



K_ϕ = Phase Detector Gain (volts/radian)
K_F = Amplifier/Filter Gain
K_V = VCO Gain (radians/second/volt)
N = Integer Divisor

Both ω_n (loop bandwidth or natural frequency) and ζ (damping factor) are particularly important in the transient response to a step input of phase or frequency (Figure 9), and are defined as:

$$\omega_n = \sqrt{\frac{K_\phi K_V}{N T_2}} \quad (4)$$

$$\zeta = \sqrt{\frac{K_\phi K_V}{N T_2}}\left(\frac{T_1}{2}\right) \quad (5)$$

Using these terms in Equation 3,

$$\frac{\theta_O(s)}{\theta_i(s)} = \frac{N(1 + T_1 s)}{\frac{s^2}{\omega_n^2} + \frac{2\zeta s}{\omega_n} + 1} \quad (6)$$

In a well defined system controlling factors such as ω_n and ζ may be chosen either from a transient basis (time domain response) or steady state frequency plot (roll-off point and peaking versus frequency). Once these two design goals are defined, synthesis of the filter is relatively straight-forward.

Constants K_ϕ, K_V, and N are usually fixed due to other design constraints, leaving T_1 and T_2 as variables to set ω_n and ζ. Since only T_2 appears in Equation 4, it is the easiest to solve for initially.

$$T_2 = \frac{K_\phi K_V}{N \omega_n^2} \quad (7)$$

From Equation 5, we find

$$T_1 = \frac{2\zeta}{\omega_n} \quad (8)$$

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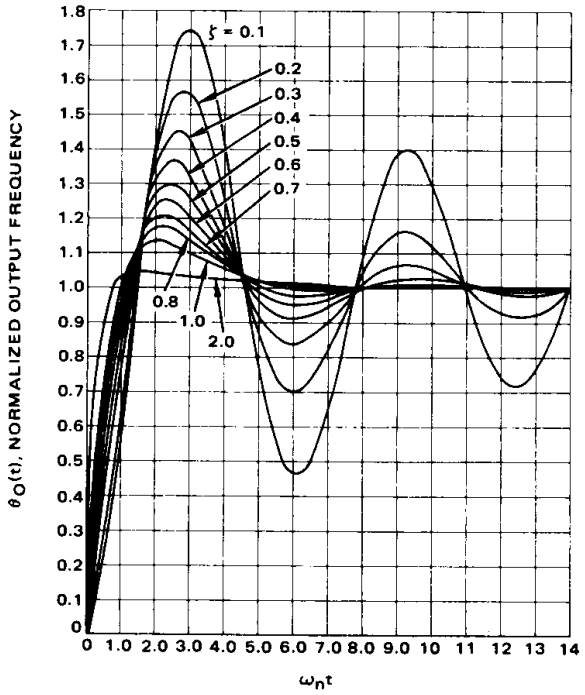
FIGURE 9 — TYPE 2 SECOND ORDER STEP RESPONSE



Using relationships 7 and 8, actual resistor values may be computed:

$$R_1 = \frac{K\phi K_V}{N\omega_n^2 C} \quad (9)$$

$$R_2 = \frac{2\zeta}{\omega_n C} \quad (10)$$

Although fundamentally the range of R_1 and R_2 may be from several hundred to several thousand ohms, sideband considerations usually force the value of R_1 to be set first, and then R_2 and C computed.

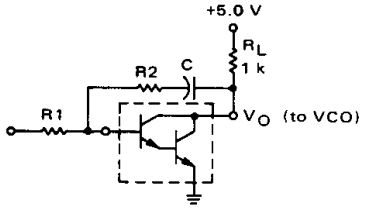
$$C = \frac{K\phi K_V}{N\omega_n^2 R_1} \quad (11)$$

Calculation of passive components R_2 and C (in synthesizers) is complicated by incomplete information on N, which is variable, and the limits of ω_n and ζ during that variance. Equally important are changes in K_V over the output frequency range. Minimum and maximum values of ω_n and ζ can be computed from Equations 4 and 5 when the appropriate worst case numbers are known for all the factors.

Amplifier/filter gain usually determines how much phase error exists between f_{in} and f_{out}, and the filter characteristic shapes capture range and transient performance. A relatively simple, low gain amplifier may usually be used in the loop since many designs are not constrained so much by phase error as by the need to make f_{in} equal f_{out}. Unnecessarily high gains can cause problems in linear loops when the system is out of lock if the amplifier output swing is not adequately restricted since integrating operational amplifier circuits will latch up in time and effectively open the loop.

The internal amplifier included in the MC4344/4044 may be used effectively if its limits are observed. The circuit configuration shown in Figure 10 illustrates the placement of R_1, R_2, C, and load resistor R_L (1 kΩ). Due to the non-infinite gain of this stage ($A_V \approx 30$) and other non-ideal characteristics, some restraint must be placed on passive component selection. Foremost is a lower limit on the value of R_2 and an upper limit on R_1. Placed in order of priority, the recommendations are as follows: (a) R2 > 50 Ω, (b) R1/R2 ≤ 10, (c) 1 kΩ < R1 < 5 kΩ.

FIGURE 10 — USING MC4344/4044 LOOP AMPLIFIER



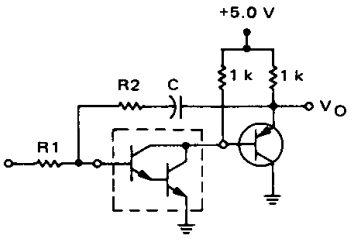
Limit (c) is the most flexible and may be violated with either higher sidebands and phase error (R_1 > 5 kΩ) or lower phase detector gain (R_1 < 1 kΩ). If limit (b) is exceeded, loop bandwidth will be less than computed and may not have any similarity to the prediction. For an accurate reproduction of calculated loop characteristics one should go to an operational amplifier which has sufficient gain to make limit (b) readily satisfied. Limit (a) is very important because T_1 in Equation 5 is in reality composed of three elements:

$$T_1 = C\left(R_2 - \frac{1}{g_m}\right) \quad (12)$$

where g_m = transconductance of the common emitter amplifier.

Normally g_m is large and T_1 nearly equals R_2C, but resistance values below 50 Ω can force the phase-compensating "zero" to infinity or worse (into the right half plane) and give an unstable system. The problem can be circumvented to a large degree by buffering the feedback with an emitter follower (Figure 11). Inequality (a) may then be reduced by at least an order of magnitude (R_2 > 5 Ω) keeping in mind that electrolytic capacitors used

FIGURE 11 — AMPLIFIER CAPABLE OF HANDLING LOWER R2



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as C may approach this value by themselves at the frequency of interest (ω_n).

Larger values of R_1 may be accommodated by either using an operational amplifier with a low bias current ($I_b < 1.0\ \mu A$) as shown in Figure 12 or by buffering the internal Darlington pair with an FET (Figure 13). It is vitally important, however, that the added device be operated at zero V_{GS}. Source resistor R_4 should be adjusted for this condition (which amounts to I_{DSS} current for the FET). This insures that the overall amplifier input threshold remains at the proper potential of approximately two base-emitter drops. Use of an additional emitter follower instead of the FET and R_4 (Figure 14) gives a threshold near the upper limit of the phase detector charge pump, resulting in an extremely unsymmetrical phase detector gain in the pump up versus pump down mode. It is not unusual to note a 5:1 difference in K_ϕ for circuits having the bipolar buffer stage. If the initial design can withstand this variation in loop gain and remain stable, the approach should be considered since there are no critical adjustments as in the FET circuit.

FIGURE 12 — USING AN OPERATIONAL AMPLIFIER TO EXTEND THE VALUE OF R1

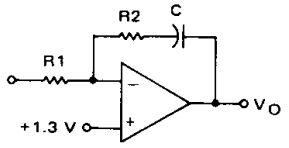


FIGURE 13 — FET BUFFERING TO RAISE AMPLIFIER INPUT IMPEDANCE

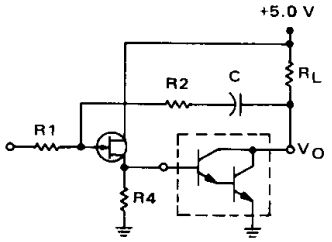
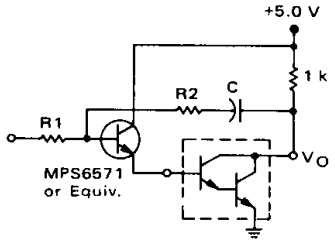


FIGURE 14 — EMITTER FOLLOWER BUFFERING OF AMPLIFIER INPUT



DESIGN PROBLEMS AND THEIR SOLUTIONS

Dynamic Range

A source of trouble for all phase-locked loops, as well as most electronics is simply overload or lack of sufficient dynamic range. One limit is the amplifier output drive to the VCO. Not only must a designer note the outside limits of the dc control voltage necessary to give the output frequency range, he must also account for the worst case of overshoot expected for the system. Relatively large damping factors ($\zeta = 0.5$) can contribute significant amounts of overshoot (30%). To be prepared for the worst case output swing the amplifier should have as much margin to positive and negative limits as the expected swing itself. That is, if a two-volt swing is sufficient to give the desired output frequency excursion, there should be at least a two-volt cushion above and below maximum expected steady-state values on the control line.

This increase in range, in order to be effective, must of course by followed by an equivalent range in the VCO or there is little to be gained. Any loss in loop gain will in general cause a decrease in ζ and a consequent increase in overshoot and ringing. If the loss in gain is caused by saturation or near saturation conditions, the problem tends to accelerate towards a situation where the system settles in not only a slow but oscillator manner as well.

Loss of amplifier gain may not be due entirely to normal system damping considerations. In loops employing digital phase detectors, an additional problem is likely to appear. This is due to amplifier saturation during a step input when there is a maximum phase detector output simultaneous with a large transient overshoot. The phase detector square wave rides on top of the normal transient and may even exceed the amplifier output limits imposed above. Since the input frequency will exceed the R_2C time constant, gain K_F for these annoying pulses will be R_2/R_1. Ordinarily this ratio will be less than 1, but some circumstances dictate a low loop gain commensurate with a fairly high ω_n. For these cases, R_2/R_1 may be higher than 10 and cause pulse-wise saturation of the amplifier. Since the dc control voltage is an average of phase detector pulses, clipping can be translated into a reduction in gain with all the "benefits" already outlined, i.e., poor settling time. An easy remedy to apply in many cases is a simple RC low pass section preceding or together with the integrator-lag section. To make transient suppression independent of amplifier response, the network may be imbedded within the input resistor R_1 (Figure 15) or be implemented by placing a feedback capacitor across R_2 (Figure 16). Besides rounding off and inhibiting pulses, these networks add an additional pole to the loop and may cause further overshoot if the cutoff frequency (ω_c) is too close to ω_n. If at all possible the cutoff point should be five to ten times ω_n. How far ω_c can be placed from ω_n depends on the input frequency relationship to ω_n since f_{in} is, after all, what is being filtered. A side benefit of this simple RC pulse "flattener" is a reduction in f_{in} sidebands around f_{out} for synthe-

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sizers with N > 1. However, a series of RC filters is not recommended for either extended pulse suppression or sideband improvement as excess phase will begin to build up at the loop crossover ($\approx \omega_n$) and tend to cause instability. This will be discussed in more detail later.

FIGURE 15 — IMPROVED TRANSIENT SUPPRESSION WITH R1 — C_c

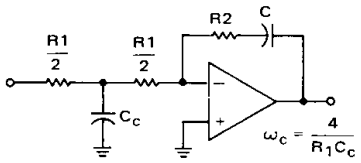
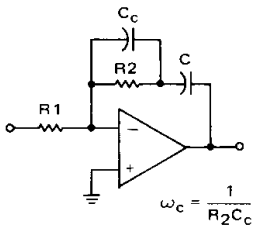


FIGURE 16 — IMPROVED TRANSIENT SUPPRESSION WITH R2 — C_c



Spurious Outputs

Although the major problem in phase-locked loop design is defining loop gain and phase margin under dynamic operating conditions, high-quality synthesizer designs also require special consideration to minimize spurious spectral components — the worst of which is reference-frequency sidebands. Requirements for good sideband suppression often conflict with other performance goals — loop dynamic behavior, suppression of VCO noise, or suppression of other in-loop noise. As a result, most synthesizer designs require compromised specifications. For a given set of components and loop dynamic conditions, reference sidebands should be predicted and checked against design specifications before any hardware is built.

Any steady-state signal on the VCO control will produce sidebands in accordance with normal FM theory. For small spurious deviations on the VCO, relative sideband-to-carrier levels can be predicted by:

$$\frac{\text{sidebands}}{\text{carrier}} \cong \frac{V_{ref} K_V}{2\omega_{ref}} \qquad (13)$$

where V_{ref} = peak voltage value of spurious frequency at the VCO input.

Unwanted control line modulation can come from a variety of sources, but the most likely cause is phase detector pulse components feeding through the loop filter. Although the filter does establish loop dynamic conditions, it leaves something to be desired as a low pass section for reference frequency components.

For the usual case where ω_{ref} is higher than $1/T_2$, the K_F function amounts to a simple resistor ratio:

$$K_F(j\omega)\Big|_{\omega = \omega_{ref}} \cong -\frac{R_2}{R_1} \qquad (14)$$

By substitution of Equations 9 and 10, this signal transfer can be related to loop parameters.

$$K_F(j\omega)\Big|_{\omega = \omega_{ref}} \cong \frac{2\zeta N\omega_n}{K_\phi K_V} = \frac{V_{ref}}{V_\phi} \qquad (15)$$

where V_{ref} = peak value of reference voltage at the VCO input, and

V_ϕ = peak value of reference frequency voltage at the phase detector output.

Sideband levels relative to reference voltage at the phase detector output can be computed by combining Equations 13 and 15:

$$\frac{\text{sideband level}}{f_{out}\ \text{level}} = V_\phi \left(\frac{\zeta N\omega_n}{\omega_{ref} K_\phi}\right) \qquad (16)$$

From Equation 16 we find that for a given phase detector, a given value of R_1 (which determines V_ϕ), and given basic system constraints (N, f_{ref}), only ζ and ω_n remain as variables to diminish the sidebands. If there are few limits on ω_n, it may be lowered indefinitely until the desired degree of suppression is obtained. If ω_n is not arbitrary and the sidebands are still objectionable, additional filtering is indicated.

One item worthy of note is the absence of K_V in Equation 16. From Equation 15 it might be concluded that decreasing K_V would be another means for reducing spurious sidebands, but for constant values of ζ and ω_n this is not a free variable. In a given loop, varying K_V will certainly affect sideband voltage, but will also vary ζ and ω_n.

On the other hand, the choice of ω_n may well affect spectral purity near the carrier, although reference sideband levels may be quite acceptable.

In computing sideband levels, the value of V_ϕ must be determined in relation to other loop components. Residual reference frequency components at the phase detector output are related to the dc error voltage necessary to supply charge pump leakage current and amplifier bias current. From these average voltage figures, spectral components of the reference frequency and its harmonics can be computed using an approximation that the phase detector output consists of square waves τ seconds

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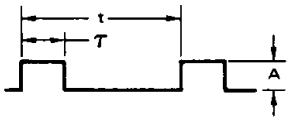
wide repeated at t second intervals (Figure 17). A Fourier analysis can be summarized for small ratios of τ/t by:

(1) the average voltage (V_{avg}) is $A(\tau/t)$
(2) the peak reference voltage value (V_ϕ) is twice V_{avg}, and
(3) the second harmonic ($2f_{ref}$) is roughly equal in amplitude to the fundamental.

By knowing the requirements for (1) due to amplifier bias and leakage currents, values for (2) and (3) are uniquely determined.

FIGURE 17 — PHASE DETECTOR OUTPUT



An example of this sideband approximation technique can be illustrated using the parameters specified for the synthesizer design included in the applications information section.

$N_{max} = 30$ $\quad \omega_n = 4500$ rad/s
$K_V = 11.2 \times 10^6$ rad/s/V $\quad R_1 = 2$ kΩ
$K_\phi = 0.12$ V/rad $\quad f_{ref} = 100$ kHz
$\zeta = 0.8$

Substituting these numbers into Equation 16:

$$\frac{\text{sideband}}{f_{out}} = V_\phi \frac{(0.8)(30)(4500)}{2\pi(10^5)(0.111)} \quad (17)$$

$$= V_\phi (1.55) \quad (18)$$

The result illustrates how much reference feedthrough will affect sideband levels. If 1.0 mV peak of reference appears at the output of the phase detector, the nearest sideband will be down 56.2 dB.

If the amplifier section included in the MC4344/4044 is used, with $R_L = 1$ kΩ, some approximations of the value of V_ϕ can be made based on the input bias current and the value of R_1. The phase detector must provide sufficient average voltage to supply the amplifier bias current, I_b, through R_1; when the bias current is about 5.0 μA and R_1 is 2 kΩ, V_{avg} must be 10 mV. From the assumptions earlier concerning the Fourier transform, and with the help of Figure 18, we can see that the phase detector duty cycle will be about 1.7% (A = 0.6 V), giving a fundamental (reference) of 20 mV peak. If this value for V_ϕ is substituted into Equation 18, the resulting sideband ratio represents 30 dB suppression due to this component alone.

In addition to the amplifier bias current, another factor to consider is transistor Q5 reverse leakage current I_L flowing into pin 10 of the MC4344/4044 charge pump. I_L is generally less than 1.0 μA and is no more than 5.0 μA over the temperature range. A typical design value for 25°C is 0.1 μA. Both I_L and amplifier bias current I_B are in a direction to deplenish the charge on filter capacitor C. A second charge pump leakage, I_L', attributed by diode CR1 flows out of pin 5. This current, however, is in a direction to help supply I_B and I_L and thus tends to minimize the discharge of C. Typically I_L' is much less than I_L and, since it is also in a direction to minimize discharge of the filter capacitor, it will be ignored in the following discussion. The total charge removed from C must be replaced by current supplied by the charge pump during the next up-date opportunity. This current flows through R1. To minimize the effects of I_B and I_L a relative small value of R1 should be chosen. A minimum value of 1 kΩ is a good choice.

FIGURE 18 — OUTPUT ERROR CHARACTERISTICS

DUTY CYCLE (%)	PHASE ERROR (Deg)	V_{avg} (mV)	$V_{\phi(peak)}$ (mV)
0.1	0.36	0.6	1.2
0.2	0.72	1.2	2.4
0.3	1.08	1.8	3.6
0.4	1.44	2.4	4.8
0.5	1.80	3.0	6.0
0.6	2.16	3.6	7.2
0.7	2.52	4.2	8.4
0.8	2.88	4.8	9.6
0.9	3.24	5.4	10.8
1.0	3.60	6.0	12.0
2.0	7.2	12.0	24.0
3.0	10.8	18.0	35.9
4.0	14.4	24.0	47.9
5.0	18.0	30.0	59.8
6.0	21.6	36.0	71.6
7.0	25.2	42.0	83.3
8.0	28.8	48.0	95.0
9.0	32.4	54.0	106.6
10.0	36.0	60.0	118.0

After values for C and R_2 have been computed on the basis of loop dynamic properties, the overall sideband to f_{out} ratio computation can be simplified.

Since

$$V_\phi = 2V_{avg}$$
$$V_{avg} = (I_b + I_L)R_1 \quad = 2R_1(I_b + I_L)\left(\frac{R_2}{R_1}\right)$$
$$V_\phi = 2(I_b + I_L)R_1$$

$$V_{ref} = V_\phi \left(\frac{R_2}{R_1}\right) \quad = 2R_2(I_b + I_L)$$

we find that

$$\frac{\text{sideband}}{f_{out}} = \frac{V_{ref}K_V}{2\omega_{ref}} \quad (19)$$

$$\frac{\text{sideband}}{f_{out}} = \frac{2R_2(I_b + I_L)K_V}{2\omega_{ref}} \quad (20)$$

Equation 20 indicates that excellent suppression could be achieved if the bias and leakage terms were nulled by current summing at the amplifier input (Figure 19). This has indeed proved to be the case. Experimental results indicate that greater than 60 dB rejection can routinely

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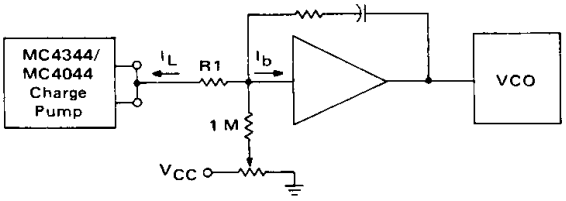
be achieved at a constant temperature. However when nulling fairly large values (> 100 nA), the rejection becomes quite sensitive since leakages are inherently a function of temperature. This technique has proved useful in achieving improved system performance when used in conjunction with good circuit practice and reference filtering.

FIGURE 19 — COMPENSATING FOR BIAS AND LEAKAGE CURRENT



Additional Loop Filtering

So far, only the effects of fundamental loop dynamics on resultant sidebands have been considered. If further sideband suppression is required, additional loop filtering is indicated. However, care must be taken in placement of any low pass rolloff with regard to the loop natural frequency (ω_n). On one hand, the "corner" should be well below (lower than) ω_{ref} and yet far removed (above) from ω_n. Although no easy method for placing the roll-off point exists, a rule of thumb that usually works is:

$$\omega_c = 5\omega_n \qquad (21)$$

Reference frequency suppression per pole is the ratio of ω_c to ω_{ref}.

$$SB_{dB} \cong n\ 20 \log_{10} \left(\frac{\omega_c}{\omega_{ref}}\right) \qquad (22)$$

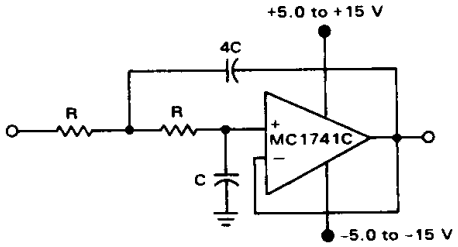
where n is the number of poles in the filter.

Equation 22 gives the additional loop suppression to ω_{ref}; this number should be added to whatever suppression already exists.

For non-critical applications, simple RC networks may suffice, but if more than one section is required, loop dynamics undergo undesirable changes. Loop damping factor decreases, resulting in a high percentage of overshoot and increased ringing since passive RC sections tend to accumulate phase shift more rapidly than signal suppression and part of this excess phase subtracts from the loop phase margin. Less phase margin translates into a lower damping factor and can, in the limit, cause outright oscillation.

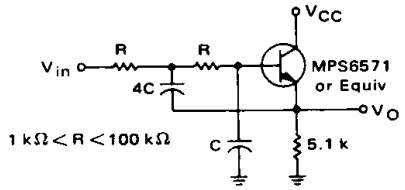
A suitable alternative is an active RC section, Figure 20, compatible with the existing levels and voltages. An active two pole filter (second order section) can realize a more gradual phase shift at frequencies less than the cutoff point and still get nearly equal suppression at frequencies above the cutoff point. Sections designed with a slight amount of peaking ($\zeta \cong 0.5$) show a good compromise between excess phase below cutoff (ω_c), without peaking enough to cause any danger of raising the loop gain for frequencies above ω_n. A fairly non-critical section may simply use an emitter follower as the active device with two resistors and capacitors completing the circuit (Figure 21). This provides a −12 dB/octave (−40 dB/decade) rolloff characteristic above ω_n, though the attenuation may be more accurately determined by Equation 22. If the sideband problem persists, an additional section may be added in series with the first. No more than two sections are recommended since at that time either (1) the constraint between ω_n and ω_{ref} is too close, or (2) reference voltage is modulating the VCO from a source other than the phase detector through the loop amplifier.

FIGURE 20 — OPERATIONAL AMPLIFIER LOW PASS FILTER



1. Choose R
   $1\ k\Omega < R < 1\ M\Omega$
2. $C = \frac{0.5}{\omega_c R}$

FIGURE 21 — EMITTER FOLLOWER LOW PASS FILTER

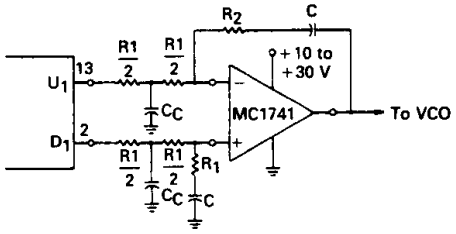


NOTE: If $V_O \geq V_{CC} - 1.0$ V, this stage is susceptible to power supply noise.

Operation without charge pump phase detector #1 of the MC4344/4044 can be implemented quite successfully in many applications without using the charge pump and internal darlington amplifier approach. An operational amplifier filter can be used to process the error information appearing at U1 and D1 (pins 13 and 2) directly (Figure 22).This phase detector/filter approach offers a potentially superior performing system because:

a. Charge pump delay time is eliminated.
b. Charge pump input signed threshold level need not be overcome before error information is obtained. This can result in a substantial improvement in the

FIGURE 22—TYPICAL FILTER AND SUMMING NETWORK



4044's transfer function linearity in the vicinity of zero phase error between the R and V inputs.

c. The filter amplifier ground location can be separated from the phase detector ground.

d. An "optimum" filter amplifier input threshold of approximately two diode drops need not be established.

The filter discussions and relationships developed for integrator-log filter sections can be applied to the system of Figure 22 and the previously derived equations can be used to determine values for R1, R2 and C.

It may be desirable to split each of the R1 resistors and incorporate a capacitor to ground in a manner similar to that shown in Figure 15. This should improve transient suppression and provide integration of the U1 and D1 signals to better enable the operational amplifier to develop corrective error information from very narrow U1 and D1 pulse widths.

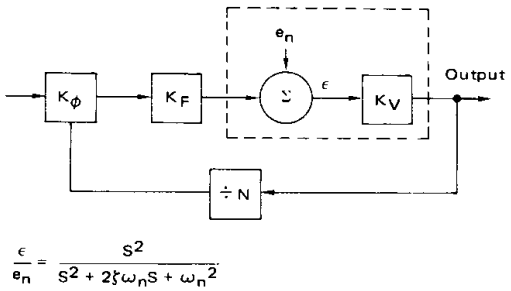
Phase error for the circuit in Figure 22 will result from input offset voltage in the operational amplifier, resistor mismatch and mismatch between the phase detector output states appearing at U1 and D1. Phase error can be trimmed to zero initially by adjusting either the amplifier input offset or one of the R1 resistors.

VCO Noise

Effects of noise within the VCO itself can be evaluated by considering a closed loop situation with an external noise source, e_n, introduced at the VCO (Figure 23). Resultant modulation of the VCO by error voltage, ε, is a second order high pass function:

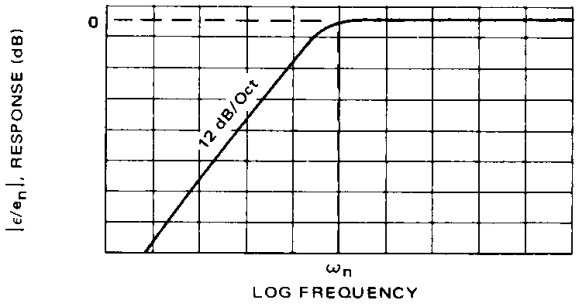
$$\frac{\varepsilon}{e_n} = \frac{S^2}{S^2 + \frac{ST_1K\phi K_V}{T_2N} + \frac{K\phi K_V}{T_2N}} = \frac{S_2}{S^2 + 2\zeta\omega_n S + \omega_n{}^2} \quad (23)$$

FIGURE 23 — EFFECTS OF VCO NOISE



This function has a slope of 12 dB/octave at frequencies less than ω_n (loop natural frequency), as shown in Figure 24. This means that noise components in the VCO above ω_n will pass unattenuated and those below will have some degree of suppression. Therefore choice of loop natural frequency may well rest on VCO noise quality.

FIGURE 24 — LOOP RESPONSE TO VCO NOISE

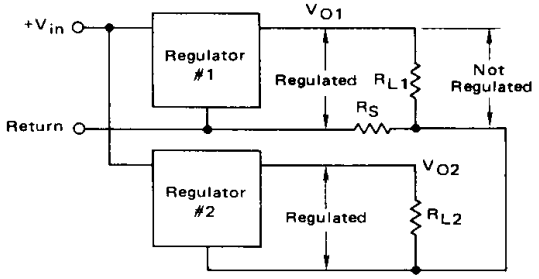


Other Spurious Responses

Spurious components appearing in the output spectrum are seldom due to reference frequency feedthrough alone. Modulation of any kind appearing on the VCO control line will cause spurious sidebands and can come in through the loop amplifier supply, bias circuitry in the control path, a translator, or even the VCO supply itself. Some VCOs have a relatively high sensitivity to power supply variation. This should be investigated and its effects considered. Problems of this nature can be minimized by operating all devices except the phase detector, charge pump, and VCO from a separate and well isolated supply. A common method uses a master supply of about 10 or 12 volts and two regulators to produce voltages for the PLL — one for all the logic (including the phase detector) and the other for all circuitry associated with the VCO control line.

Sideband and noise performance is also a function of good power supply and regulator layout. As mentioned earlier, extreme care should be exercised in isolating the control line voltage to the VCO from influences other than the phase detector. This not only means good voltage regulation but ac bypassing and adherence to good grounding techniques as well. Figure 25 shows two separate regulators and their respective loads. Resistor R_S is a small stray resistance due to a common thin ground return for both R_{L1} and R_{L2}. Any noise in R_{L2} is now reproduced (in a suppressed form) across R_{L1}. Load current from R_{L1} does not affect the voltage across R_{L2}. Even though the regulators may be quite good, they can hold V_O constant only across their outputs, not necessarily across the load (unless remote sensing is used).

FIGURE 25 — LOOP VOLTAGE REGULATION



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One solution to the ground-coupled noise problem is to lay out the return path with the most sensitive regulated circuit at the farthest point from power supply entry as shown in Figure 26.

Even for regulated subcircuits, accumulated noise on the ground bus can pose major problems since although the cross currents do not produce a differential load voltage directly, they do produce essentially common mode noise on the regulators. Output differential load noise then is a function of the input regulation specification. By far the best way to sidestep the problem is to connect each subcircuit ground to the power supply entry return line as shown in Figure 27.

FIGURE 26 — REGULATOR LAYOUT

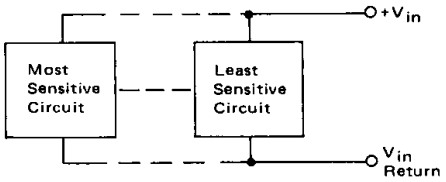
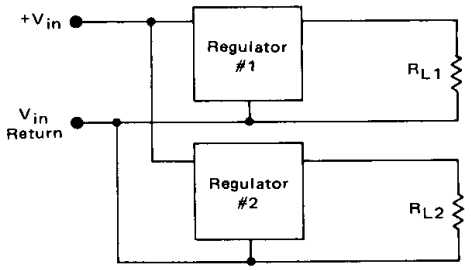


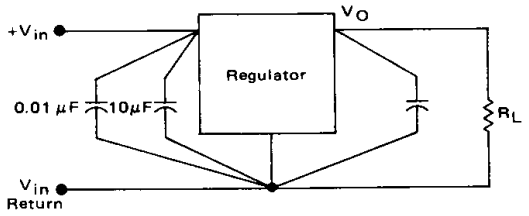
FIGURE 27 — REGULATOR GROUND CONNECTION



In Figures 25 and 27, R_{L1} and R_{L2} represent component groups in the system. The designer must insure that all ground return leads in a specific component group are returned to the common ground. Probably the most overlooked components are bypass capacitors. To minimize sidebands, extreme caution must be taken in the area immediately following the phase detector and through the VCO. A partial schematic of a typical loop amplifier and filter is shown in Figure 28 to illustrate the common grounding technique.

Bypassing in a phase-locked loop must be effective at both high frequencies and low frequencies. One capacitor in the 1.0-to-10 μF range and another between 0.01 and 0.001 μF are usually adequate. These can be effectively utilized both at the immediate circuitry (between supply and common ground) and the regulator if it is some distance away. When used at the regulator, a single electrolytic capacitor on the output and a capacitor pair at the input is most effective (Figure 29). It is important, again, to note that these bypasses go from the input/output pins to as near the regulator ground pin as possible.

FIGURE 29 — SUGGESTED BYPASSING PROCEDURE



APPLICATIONS INFORMATION

Frequency Synthesizers

The basic PLL discussed earlier is actually a special case of frequency synthesis. In that instance, $f_{out} = f_{in}$, although normally a programmable counter in the feedback loop insures the general rule that $f_{out} = Nf_{in}$ (Figure 30). In the synthesizer f_{in} is usually constant (crystal controlled) and f_{out} is changed by varying the programmable divider (÷ N). By stepping N in integer increments, the output frequency is changed by f_{in} per increment. In com-

FIGURE 30 — PHASE-LOCKED LOOP WITH PROGRAMMABLE COUNTER

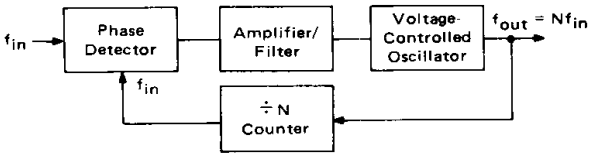
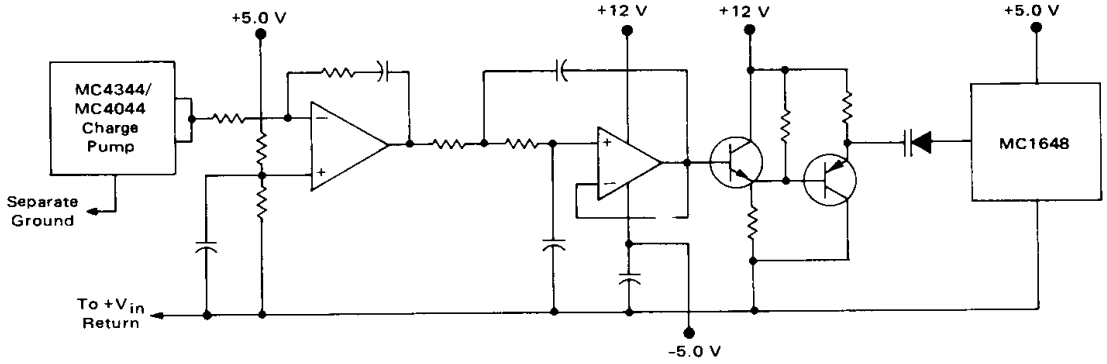


FIGURE 28 — PARTIAL SCHEMATIC OF LOOP AMPLIFIER AND FILTER



munication use, this input frequency is called the "channel spacing" or, in general, it is the reference frequency.

There is essentially no difference in loop dynamic problems between the basic PLL and synthesizers except that synthesizer designers must contend with problems peculiar to loops where N is variable and greater than 1. Also, sidebands or spectral purity usually require special attention. These and other aspects are discussed in greater detail in AN-535. The steps for a suitable synthesis procedure may be summarized as follows:

Synthesis Procedure

1. Choose input frequency. (f_{ref} = channel spacing)
2. Compute the range of digital division:

$$N_{max} = \frac{f_{max}}{f_{ref}}$$

$$N_{min} = \frac{f_{min}}{f_{ref}}$$

3. Compute needed VCO range:

$$(2f_{max} - f_{min}) < f_{VCO} < (2f_{min} - f_{max})$$

4. Choose minimum ζ from transient response plot, Figure 9. A good starting point is $\zeta = 0.5$.
5. Choose ω_n from needed response time (Figure 9):

$$\omega_n = \frac{\omega_n t}{t}$$

6. Compute C:

$$C = \frac{K_\phi K_V}{N_{max}\omega_n^2 R_1}$$

7. Compute R_2:

$$R_2 = \frac{2\zeta_{min}}{\omega_n C}$$

8. Compute ζ_{max}:

$$\zeta_{max} = \zeta_{min}\sqrt{\frac{N_{max}}{N_{min}}}$$

9. Check transient response of ζ_{max} for compatibility with transient specification.
10. Compute expected sidebands:

$$\frac{\text{sideband}}{f_{out}} \cong \frac{(I_b + I_L)R_2 K_V}{\omega_{ref}} \qquad \text{(A)}$$

(I_L is about 100 nA at $T_J = 25°C$.)

11. If step 10 yields larger sidebands than are acceptable, add a single pole at the loop amplifier by splitting R_1 and adding C_c as shown in Figure 15:

$$C_c \cong \frac{0.8}{R_1\omega_n}$$

Added sideband suppression (dB) is:

$$dB \cong 20\log_{10}\frac{1}{\sqrt{1 + \frac{\omega_{ref}^2}{25(\omega_n)^2}}} \qquad \text{(B)}$$

12. If step 11 still does not give the desired results, add a second order section at $\omega_c = 5\,\omega_n$ using either the configuration of Figure 20 or 21. The expected improvement is twice that of the single pole in step 11.

$$dB \cong 40\log_{10}\frac{1}{\sqrt{1 + \frac{\omega_{ref}^2}{25(\omega_n)^2}}} \qquad \text{(C)}$$

Total sideband rejection is then the total of $20\log_{10}$(A) + (B) + (C).

Design Example (Figure 31)

Assume the following requirements:
Output frequency, f_{out} = 2.0 MHz to 3.0 MHz
Frequency steps, f_{in} = 100 kHz
Lockup time between channels (to 5%) = 1.0 ms
Overshoot < 20%.
Minimum sideband suppression = −30 dB

From the steps of the synthesis procedure:

1. $f_{ref} = f_{in} = 100$ kHz
2. $N_{max} = \frac{f_{max}}{f_{ref}} = \frac{3.0\text{ MHz}}{0.1\text{ MHz}} = 30$

   $N_{min} = \frac{f_{min}}{f_{ref}} = \frac{2.0\text{ MHz}}{0.1\text{ MHz}} = 20$
3. VCO range:
   The VCO output frequency range should extend beyond the specified minimum-maximum limits to accommodate the overshoot specification. In this instance f_{out} should be able to cover an additional 20% on either end. End limits on the VCO are:

   $f_{out}max \geq 3.0 + 0.2(1.0) = 3.2$ MHz
   $f_{out}min \leq 2.0 - 0.2(1.0) = 1.8$ MHz

   This VCO range (≈ 1.8:1) is realizable with the MC4324/4024 voltage controlled multivibrator. From Figure 5 of the MC4324/4024 data sheet we find the required tuning capacitor value to be 120 pF and the VCO gain, K_V, typically 11 x 10^6 rad/s/v.
4. From the step response curve of Figure 9, $\zeta = 0.8$ will produce a peak overshoot less than 20%.
5. Referring to Figure 9, overshoot with $\zeta = 0.8$ will settle to within 5% at $\omega_n t = 4.5$. Since the required lock-up time is 1.0 ms,

$$\omega_n = \frac{\omega_n t}{t} = \frac{4.5}{t} = \frac{4.5}{0.001} = (4.5)(10^3)\text{rad/s}$$

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6. In order to compute C, phase detector gain and R1 must be selected. Phase detector gain, K_ϕ, for the MC4344/4044 is approximately 0.1 volt/radian with $R_1 = 1\ k\Omega$. Therefore,

$$C = \frac{(0.1)(11 \times 10^6)}{(30)(4.5 \times 10^3)^2(10^3)} = 1.8\ \mu F$$

7. At this point, R_2 can be computed:

$$R_2 = \frac{2\zeta_{min}}{\omega_n C} = \frac{1.6}{(4.5 \times 10^3)(1.8 \times 10^{-6})} = 200\ \Omega$$

8. $$\zeta_{max} = \zeta_{min}\sqrt{\frac{N_{max}}{N_{min}}} = 0.98$$

9. Figure 9 shows that $\zeta = 0.98$ will meet the settling time requirement.
10. Sidebands may be computed for two cases: (1) with I_L (charge pump leakage current) nominal (100 nA), and (2) with I_L maximum (5.0 μA). A value of 5 μA will also be assumed for the amplifier bias current, i_b.

$$\left.\frac{\text{sideband}}{f_{out}}\right|_{max} = \frac{(10 \times 10^{-6})(200)(11 \times 10^6)}{6.28 \times 10^5} \cong 35 \times 10^{-3}$$

The sideband-to-center frequency ratio nominally will be:

$$\left.\frac{\text{sideband}}{f_{out}}\right|_{nom} = \frac{5.1}{10} \times 35 \times 10^{-3}$$

$$= 20 \log_{10}(17.85 \times 10^{-3}) \cong -35\ dB$$

If desired additional sideband filtering can be obtained as noted in steps 11 and 12.

11. By splitting R_1 and C_C, further attenuation can be gained. The magnitude of C_C is approximately:

$$C_C = \frac{0.8}{R_1\omega_n} = \frac{0.8}{(10^3)(4.5)(10^3)} \cong 0.18\ \mu F$$

Improvement in sidebands will be:

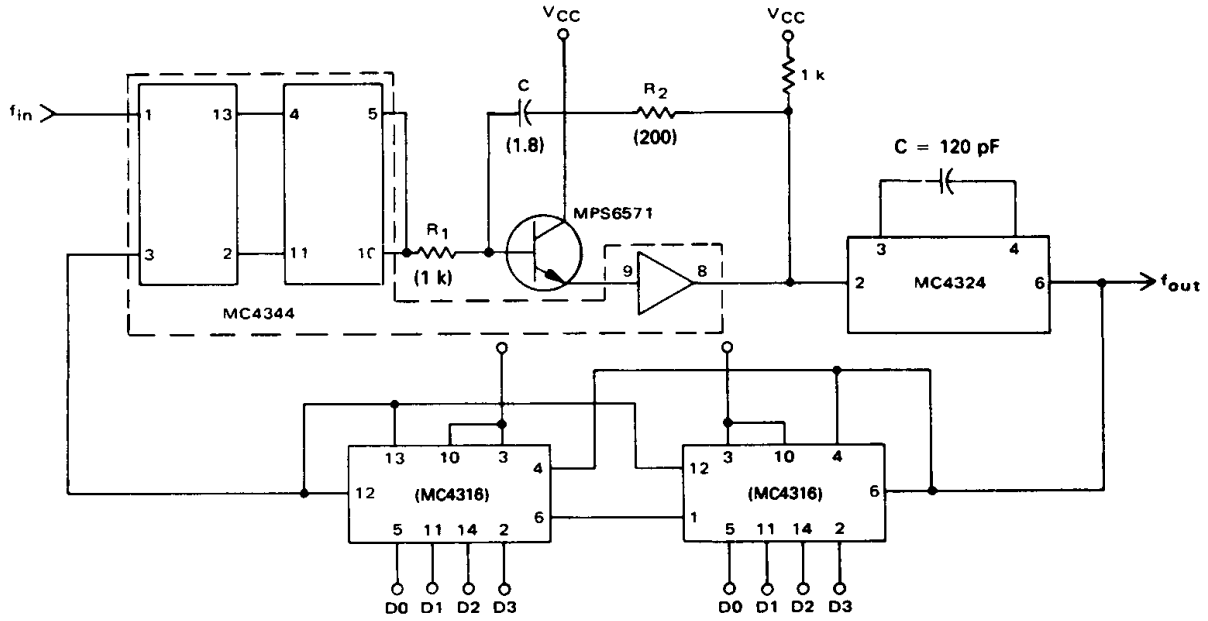
$$20 \log_{10} \frac{1}{\sqrt{1 + \frac{(2\pi \times 10^5)^2}{25(4.5 \times 10^3)^2}}} = -28\ dB$$

Nominal suppression is now −63 dB. Worst-case is 6 dB higher than nominal suppression of −57 dB. This is well within the −30 dB design requirement, step 12 is included for completeness only.

12. Attenuation of a second order filter is double that of the single order filter section described in step11. The calculations for a second order filter indicate an additional −56 dB of sideband rejection. Figures 20 and 21 show two second order filter configurations. If R is assigned a value of 10 kΩ then C may be calculated.

$$C = \frac{0.1}{\omega_n R} = \frac{0.1}{(4.5 \times 10^3)(10^4)} = 0.0022\ \mu F$$

FIGURE 31 — CIRCUIT DIAGRAM OF TYPE 2 PHASE-LOCKED LOOP



Clock Recovery from Phase-Encoded Data

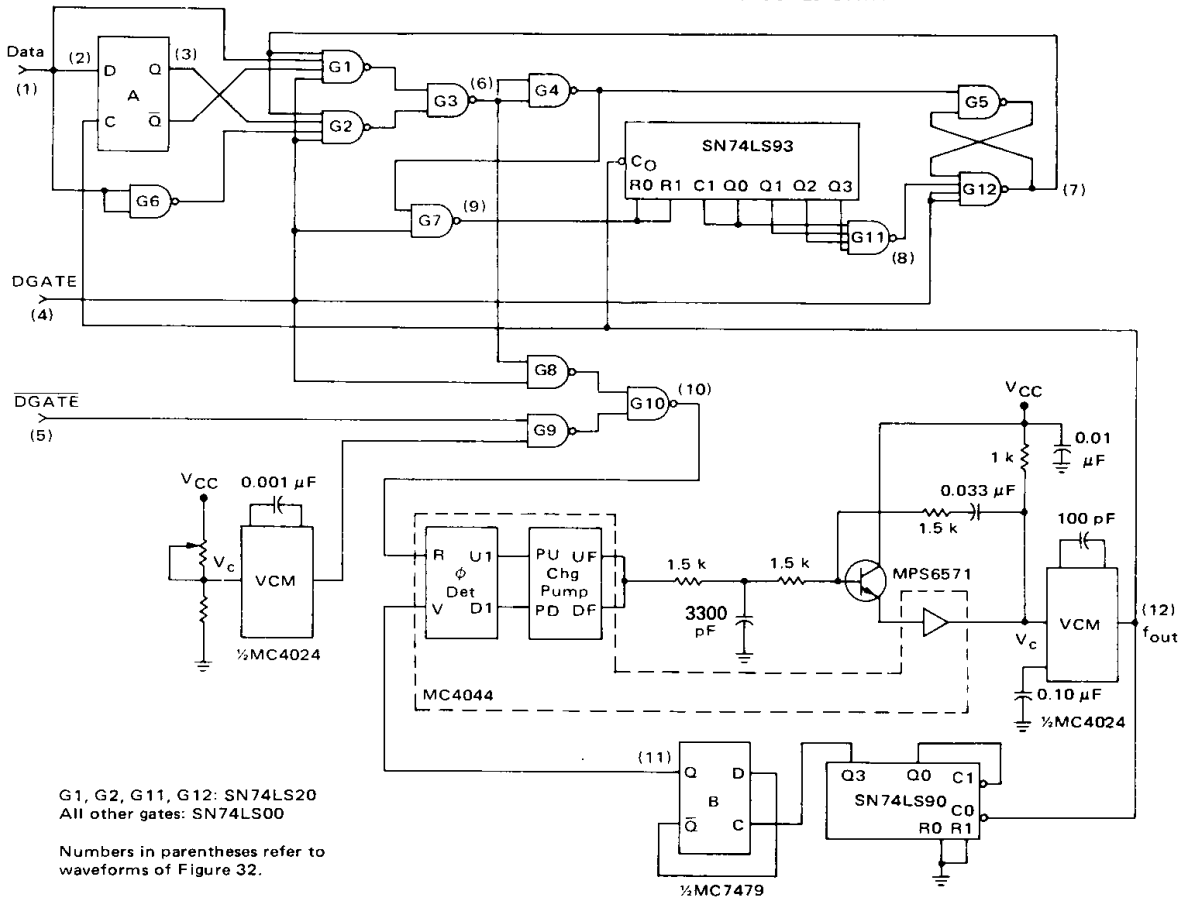
The electro-mechanical system used for recording digital data on magnetic tape often introduces random variations in tape speed and data spacing. Because of this and the encoding technique used, it is usually necessary to regenerate a synchronized clock from the data during this read cycle. One method for doing this is to phase-lock a voltage controlled multivibrator to the data as it is read (Figure 32).

A typical data block using the phase encoded format is shown in row 1 of Figure 33. The standard format calls for recording a preamble of forty "0"s followed by a single "1"; this is followed by from 18 to 2048 characters of data and a postamble consisting of a "1" followed by forty "0"s. The encoding format records a "0" as a transition from low to high in the middle of a data cell. A "1" is indicated by a transition from high to low at the data cell midpoint. When required, phase transitions occur at the end of data cells. If a string of either consecutive "0"s or consecutive "1"s is recorded, the format duplicates the original clock; the clock is easily recovered by straight forward synchronization with a phase-locked loop. In the general case, where the data may appear in any order, the phase-encoded data must be processed to obtain a single pulse during each data cell before it is applied to the phase detector. For example, if the data consisted only of alternating "1"s and "0"s, the phase-encoded format would result in a waveform equal to one-half the original clock frequency. If this were applied directly to the loop, the VCM would of course move down to that frequency. The encoding format insures that there will be a transition in the middle of each data time. If only these transitions are sensed they can be used to regenerate the clock. The schematic diagram of Figure 32 indicates one method of accomplishing this.

The logic circuitry generates a pulse at the midpoint of each data cell which is then applied to the reference input of the phase detector. The loop VCM is designed to operate at some multiple of the basic clock rate. The VCM frequency selected depends on the decoding resolution desired and other system timing requirements. In this example, the VCM operates at twenty-four times the clock rate (Figure 33, Row 12).

Referring to Figure 32 and the timing diagram of Figure 33, the phase-encoded data (Figure 33, Row 1) is combined with a delayed version of itself (output of flip-flop A row 3) to provide a positive pulse out of G3 for every transition of the input signal. Portions of the data block are shown expanded in row 2 of Figure 33. Flip-flop A delays the incoming data of one-half of a VCM clock period. Gates G1, G2 and G3 implement the logic Exclusive OR of waveforms 1 and 3 except when inhibited by DGATE (row 4) or the output of G12 (row 7). DGATE and

FIGURE 32 — CLOCK RECOVERY FROM PHASE-ENCODED DATA



its complement, $\overline{DGATE}$, serve to initialize the circuitry and insure that the first transition of the data block (a phase transition) is ignored. The MC7493 binary counter and the G5-G12 latch generate a suitable signal for gating out G3 pulses caused by phase transitions at the end of a data cell, such as the one shown dashed in row 6.

The initial data pulse from G3 sets G12 low and is combined with DGATE in G7 to reset the counter to its zero state. Subsequent VCM clock pulses now cycle the counter and approximately one-third of the way through the next data cell the counter's full state is decoded by G11, generating a negative transition. This causes G12 to go high, removing the inhibit signal until it is again reset by the next data transition. This pulse also resets the counter, continuing the cycle and generating a positive pulse at the midpoint of each data cell as required.

Acquisition time is reduced if the loop is locked to a frequency approximately the same as the expected data rate during inter-block gaps. In Figure 32, this is achieved by operating the remaining half of the dual VCM at slightly less than the data rate and applying it to the reference input of the phase detector via the G8-G9-G10 data selector. When data appears, DGATE and $\overline{DGATE}$ cause the output of G3 to be selected as the reference input to the loop.

The loop parameters are selected as a compromise between fast acquisition and jitter-free tracking once synchronization is achieved. The resulting filter component values indicated in Figure 32 are suitable for recovering the clock from data recorded at a 120 kHz rate, such as would result in a tape system operating at 75 i.p.s. with a recording density of 1600 b.p.i. Synchronization is achieved by approximately the twenty-fourth bit time of the preamble. The relationship between system requirements and the design procedure is illustrated by the following sample calculation:

Assume a −3.0 dB loop bandwidth much less than the input data rate (≈ 120 kHz), say 10 kHz. Further, assume a damping factor of $\zeta = 0.707$. From the expression for loop bandwidth as a function of damping factor and undamped natural frequency, ω_n, calculate ω_n as:

$$\omega_{-3\ dB} = \omega_n \left(1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}\right)^{1/2} \quad (24)$$

or for $\omega_{-3\ dB} = (2\pi)10^4$ rad/s and $\zeta = 0.707$:

$$\omega_n = \frac{(2\pi)10^4}{2.06} = (3.05)10^4 \text{ rad/s}$$

As a rough check on acquisition time, assume that lockup should occur not later than half-way through a 40-bit preample, or for twenty 8.34 μs data periods.

$$\omega_n t = (3.05)10^4(20)(8.34)10^{-6} = 5.1 \quad (26)$$

From Figure 9, the output will be within 2 to 3% of its final value for $\omega_n t \approx 5$ and $\zeta = 0.707$. The filter components are calculated by:

$$\frac{K_\phi K_V}{R_1 CN} = \omega_n^2 \quad (27)$$

and

$$\frac{K_\phi K_V R_2}{R_1 N} = 2\zeta\omega_n \quad (28)$$

where $K_\phi = 0.115$ v/rad
$K_V = (18.2)\ 10^6$ rad/s/volt
$N = 24$ = Feedback divider ratio
$\omega_n = (3.05)\ 10^4$ rad/s
$\zeta = 0.707$

$$\frac{K_\phi K_V}{N} = \frac{(0.115)(18.2)10^6}{24} = (8.72)10^4$$

From Equation 27:

$$R_1 C = \frac{K_\phi K_V}{N\omega_n^2} = \frac{(8.72)10^4}{(3.05)^2 10^8} = (9.34)10^{-5}$$

From Equation 28:

$$\frac{R_2}{R_1} = \frac{2\zeta\omega_n N}{K_\phi K_V} = \frac{2(0.707)(3.05)10^4}{(8.72)10^4} = 0.494 \approx \tfrac{1}{2}$$

Let $R_1 = 3.0$ kΩ; then $R_2 = 1.5$ kΩ and

$$C = \frac{(9.34)10^{-5}}{(3.0)10^3} = (3.1)10^{-8}$$

or using a close standard value, use C = 0.033 μF. Now add the additional prefiltering by splitting R_1 and selecting a time constant for the additional section so that it is large with respect to R_2C_2.

$$10(\tfrac{1}{2}R_1)C_C = R_2 C$$

or

$$C_C = \frac{2R_2C}{10R_1} = \frac{2(1.5)10^3(3.3)10^{-8}}{10(3.0)10^3} = 3300 \text{ pF}$$

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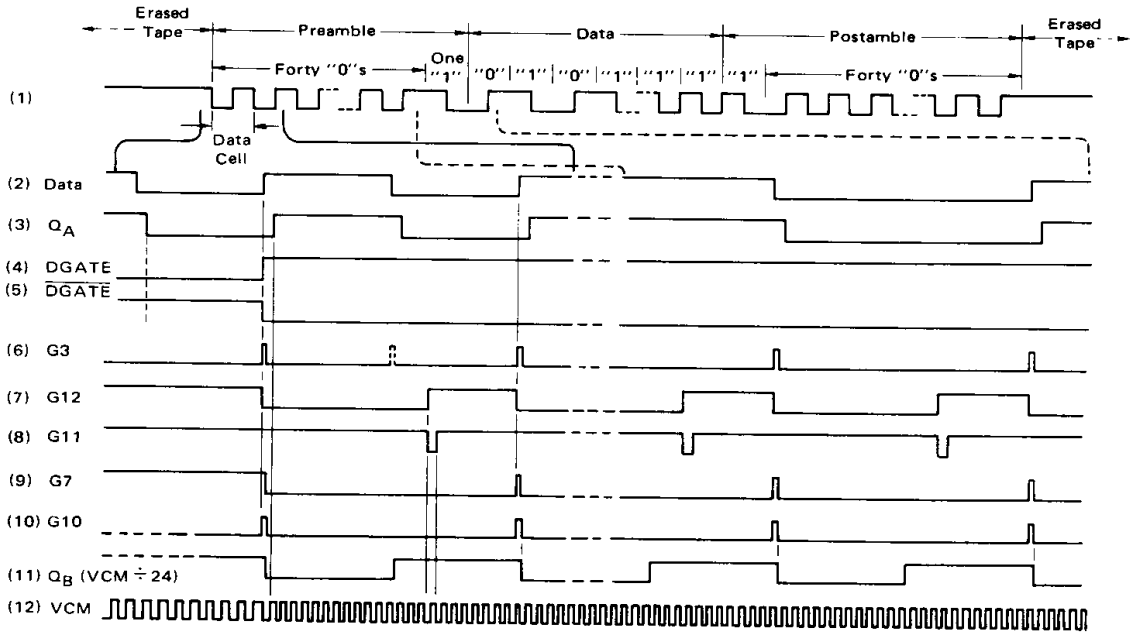
FIGURE 33 — TIMING DIAGRAM — CLOCK RECOVERY FROM PHASE-ENCODED DATA



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