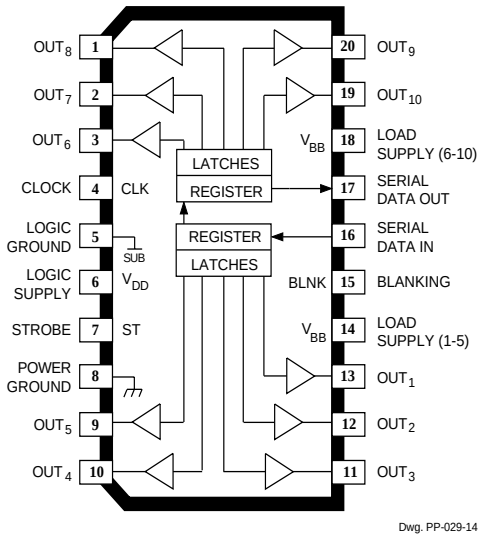
5910

Data Sheet
26182.2A

HIGH-VOLTAGE BiMOS III 10-BIT SERIAL-INPUT, LATCHED DRIVERS



Note that the dual in-line package (designator 'A') and small-outline IC package (designator 'LW') are electrically identical and share a common terminal number assignment.

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Logic Supply Voltage, V_{DD} ..... **15 V**
Driver Supply Voltage, V_{BB}
UCN5910A/LW ..... **150 V**
Suffix "-2" ..... **140 V**
Continuous Output Current Range,
I_{OUT} ..... **-30 mA to +40 mA**
Input Voltage Range,
V_{IN} ..... **-0.3 V to V_{DD} + 0.3 V**
Package Power Dissipation, P_D. **See Graph**
Operating Temperature Range,
T_A ..... **-20°C to +85°C**
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

The UCN5910x combines a 10-bit CMOS shift register and accompanying data latches, control circuitry, high-voltage bipolar sourcing outputs with DMOS active pull-downs. Designed primarily to drive ink-jet and piezoelectric printers, large flat-panel vacuum-fluorescent or ac plasma displays, the 140 V or 150 V and ±50 mA output ratings also allow these devices to be used in many other peripheral power driver applications. The lower-cost (suffix "-2") devices are identical to the basic devices except for output voltage rating.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. With a 5 V logic supply, serial-data input rates are typically over 5 MHz, with significantly higher speeds obtainable at 12 V. Use with TTL may require appropriate pull-up resistors to ensure an input logic high.

A CMOS serial data output enables cascade connections in applications requiring additional drive lines. Similar devices for up to 60-volt operation are available in 10, 12, 20, and 32-bit configurations.

The UCN5910A/LW output source drivers are npn Darlingtons capable of sourcing at least 40 mA. The DMOS active pull-downs are capable of sinking at least 30 mA. For inter-digit blanking, all of the output drivers can be disabled and the DMOS sink drivers turned ON by the BLANKING input high.

The UCN5910A and UCN5910A-2 are furnished in a 20-pin dual in-line plastic package. The surface-mount UCN5910LW and UCN5910LW-2 are furnished in a wide-body, small-outline plastic package (SOIC) with gull-wing leads. Copper lead frames, reduced supply current requirements, and lower output saturation voltages allow all devices to be operated at ±20 mA from all outputs (50% duty cycle), at ambient temperatures up to +30°C, or at ±15 mA to +55°C.

FEATURES

- High-Speed Source Drivers
- 140 V (suffix "-2") or 150 V Minimum Output Breakdown
- Improved Replacements for TL4810B
- Low Output Saturation Voltages
- Low-Power CMOS Logic and Latches
- To 3.3 MHz Data Input Rate
- Active DMOS Pull-Downs

PRELIMINARY INFORMATION
(Subject to change without notice)
January 18, 2000

Always order by complete part number, e.g., **UCN5910A-2** .

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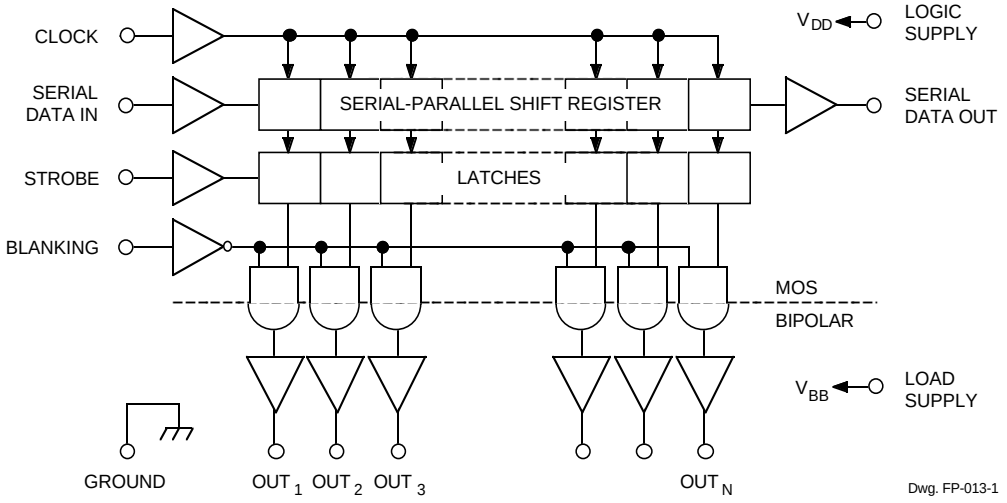
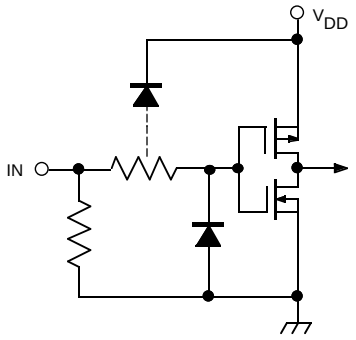
FUNCTIONAL BLOCK DIAGRAM

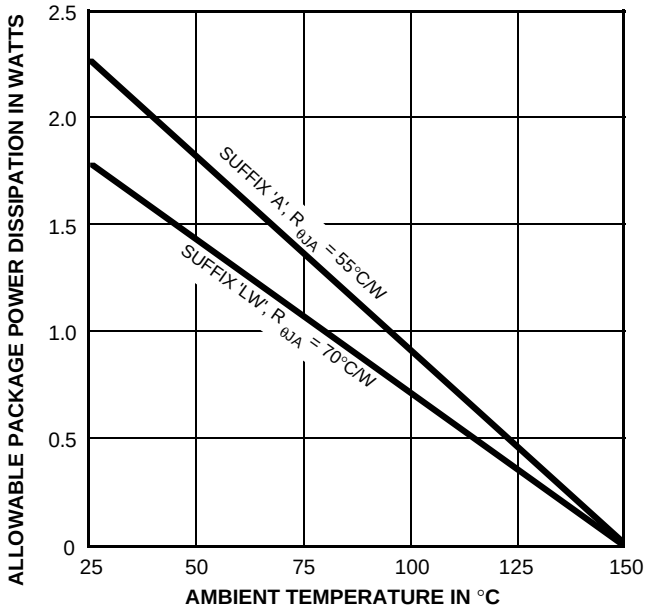


Dwg. FP-013-1

TYPICAL INPUT CIRCUIT

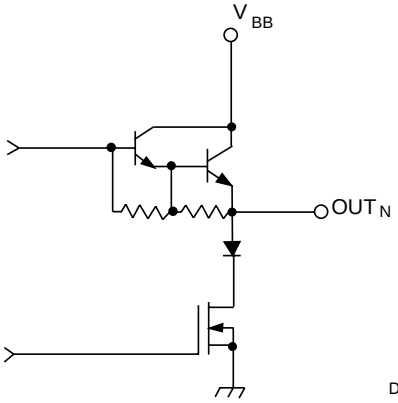


Dwg. EP-010-4A



Dwg. GS-004A

TYPICAL OUTPUT DRIVER



Dwg. No. A-14,219

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ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 150 V (basic devices) or 140 V (suffix "-2") unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 5 V			Limits @ V_{DD} = 12 V			Units
			Mln.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, T_A = +70°C	–	-5.0	-15	–	-5.0	-15	µA
Output Voltage	$V_{OUT(1)}$	Basic, I_{OUT} = -40 mA	145	148	–	145	148	–	V
		Suffix "-2", I_{OUT} = -40 mA	135	–	–	135	–	–	V
	$V_{OUT(0)}$	I_{OUT} = 5 mA	–	2.5	3.2	–	2.0	3.2	V
		I_{OUT} = 10 mA	–	5.0	–	–	–	–	V
		I_{OUT} = 30 mA	–	–	–	–	12	25	V
Output Pull-Down Current	$I_{OUT(0)}$	V_{OUT} = 5 V to V_{BB}	10	14	–	–	–	–	mA
		V_{OUT} = 20 V to V_{BB}	–	–	–	25	40	–	mA
Input Voltage	$V_{IN(1)}$		3.5	–	5.3	10.5	–	12.3	V
	$V_{IN(0)}$		-0.3	–	+0.8	-0.3	–	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	–	0.05	0.5	–	0.05	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	-0.3	–	-0.8	-0.3	–	-0.8	µA
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 µA	4.5	5.0	–	11.7	12	–	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	–	200	250	–	200	250	mV
Maximum Clock Frequency	f_{clk}		3.3	5.0	–	5.0	–	–	MHz
Supply Current	$I_{DD(1)}$	All Outputs High	–	320	450	–	650	800	µA
	$I_{DD(0)}$	All Outputs Low	–	320	450	–	650	800	µA
	$I_{BB(1)}$	Outputs High, No Load	–	0.6	1.75	–	0.9	1.75	mA
	$I_{BB(0)}$	Outputs Low	–	10	100	–	10	100	µA
Blanking to Output Delay	t_{PHL}	C_L = 30 pF, 50% to 50%	–	0.7	0.9	–	0.35	0.6	µs
	t_{PLH}	C_L = 30 pF, 50% to 50%	–	0.9	1.3	–	0.35	0.6	µs
Output Fall Time	t_f	C_L = 30 pF, 90% to 10%	–	1.3	1.5	–	0.6	0.7	µs
Output Rise Time	t_r	C_L = 30 pF, 10% to 90%	–	1.2	1.5	–	1.0	1.2	µs

Negative current is defined as coming out of (sourcing) the specified device terminal.

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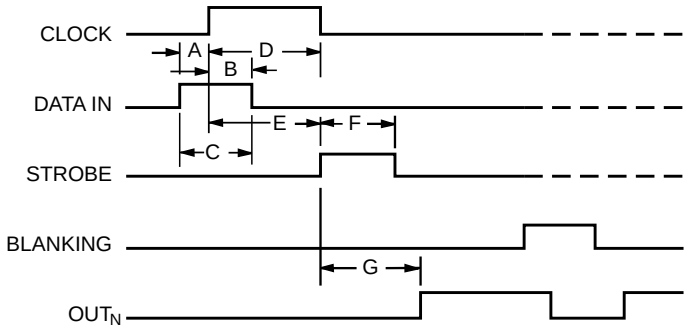
HIGH-VOLTAGE BiMOS III 10-BIT SERIAL-INPUT, LATCHED DRIVERS



Dwg. No. A-12,649A

TIMING CONDITIONS

(T_A = +25°C, V_{DD} = 12 V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) ..... **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) ..... **75 ns**
C. Minimum Data Pulse Width ..... **150 ns**
D. Minimum Clock Pulse Width ..... **100 ns**
E. Minimum Time Between Clock Activation and Strobe ..... **300 ns**
F. Minimum Strobe Pulse Width ..... **100 ns**
G. Typical Time Between Strobe Activation and Output Transition ..... **750 ns**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Blanking	Output Contents
		I_1 I_2 I_3 ... I_{N-1} I_N			I_1 I_2 I_3 ... I_{N-1} I_N		I_1 I_2 I_3 ... I_{N-1} I_N
H	⎍	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	⎍	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	⎎	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

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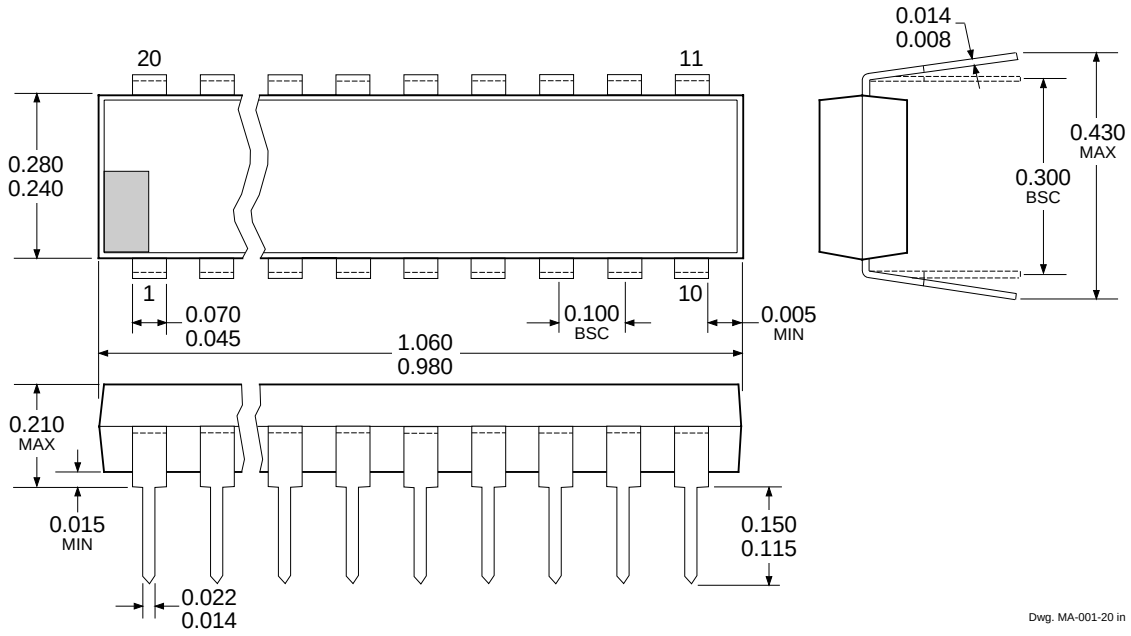
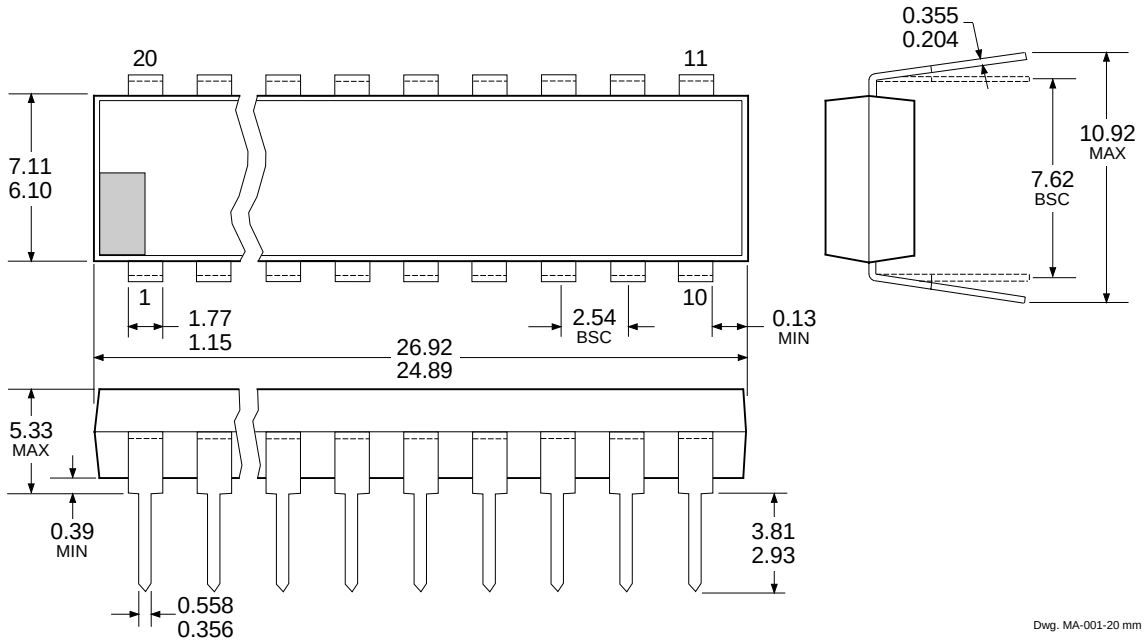
UCN5910A & UCN5910A-2

Dimensions in Inches
(controlling dimensions)



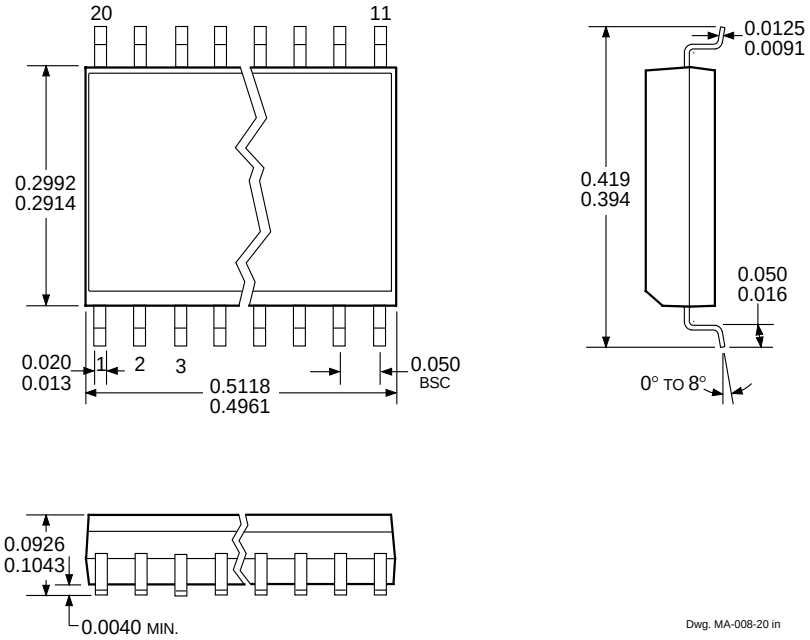
Dimensions in Millimeters
(for reference only)



NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Lead thickness is measured at seating plane or below.

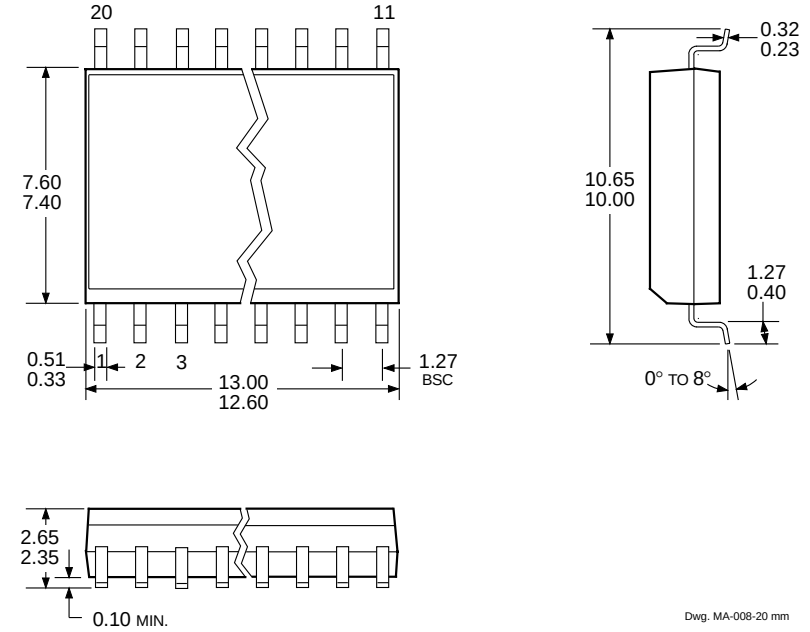
UCN5910LW & UCN5910LW-2

Dimensions in Inches
(for reference only)



Dwg. MA-008-20 in

Dimensions in Millimeters
(controlling dimensions)



Dwg. MA-008-20 mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.

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HIGH-VOLTAGE BiMOS III 10-BIT SERIAL-INPUT, LATCHED DRIVERS

BiMOS II (Series 5800), BiMOS III (Series 5900), & DABiC IV (Series 6800) INTELLIGENT POWER INTERFACE DRIVERS

Function	Output Ratings*		Part Number†
SERIAL-INPUT LATCHED DRIVERS			
8-Bit (saturated drivers)	-120 mA	50 V‡	5895
8-Bit	350 mA	50 V	5821
8-Bit	350 mA	80 V	5822
8-Bit	350 mA	50 V‡	5841
8-Bit	350 mA	80 V‡	5842
8-Bit (constant-current LED driver)	75 mA	17 V	6275
9-Bit	1.6 A	50 V	5829
10-Bit (active pull-downs)	-25 mA	60 V	5810-F and 6809/10
10-Bit (active pull-downs)	-40 mA	140 V	5910-2
10-Bit (active pull-downs)	-40 mA	150 V	5910
12-Bit (active pull-downs)	-25 mA	60 V	5811 and 6811
16-Bit (constant-current LED driver)	75 mA	17 V	6276
20-Bit (active pull-downs)	-25 mA	60 V	5812-F and 6812
32-Bit (active pull-downs)	-25 mA	60 V	5818-F and 6818
32-Bit	100 mA	30 V	5833
32-Bit (saturated drivers)	100 mA	40 V	5832
PARALLEL-INPUT LATCHED DRIVERS			
4-Bit	350 mA	50 V‡	5800
8-Bit	-25 mA	60 V	5815
8-Bit	350 mA	50 V‡	5801
SPECIAL-PURPOSE DEVICES			
Unipolar Stepper Motor Translator/Driver	1.25 A	50 V‡	5804
Addressable 28-Line Decoder/Driver	450 mA	30 V	6817

* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits. Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Internal transient-suppression diodes included for inductive-load protection.

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