3.3V LOW SKEW CMOS PLL CLOCK DRIVER WITH INTEGRATED LOOP FILTER

QS5LV919

FEATURES:

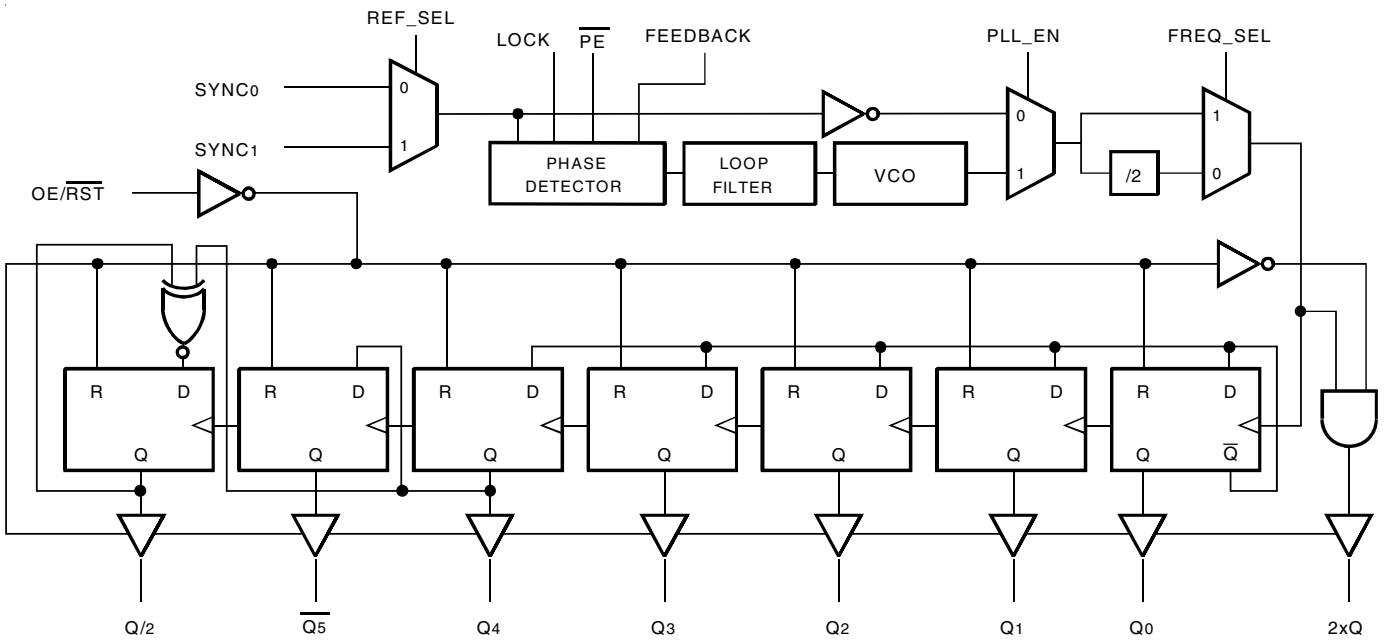
- **3.3V operation**
- **JEDEC compatible LVTTL level outputs**
- **Clock inputs are 5V tolerant**
- **< 300ps output skew, Q_0–Q_4**
- **2xQ output, Q outputs, $\overline{Q}$ output, Q/2 output**
- **Outputs 3-state and reset while OE/$\overline{RST}$ low**
- **PLL disable feature for low frequency testing**
- **Internal loop filter RC network**
- **Functional equivalent to MC88LV915, IDT74FCT388915**
- **Positive or negative edge synchronization ($\overline{PE}$)**
- **Balanced drive outputs ±24mA**
- **160MHz maximum frequency (2xQ output)**
- **Available in QSOP and PLCC packages**

DESCRIPTION:

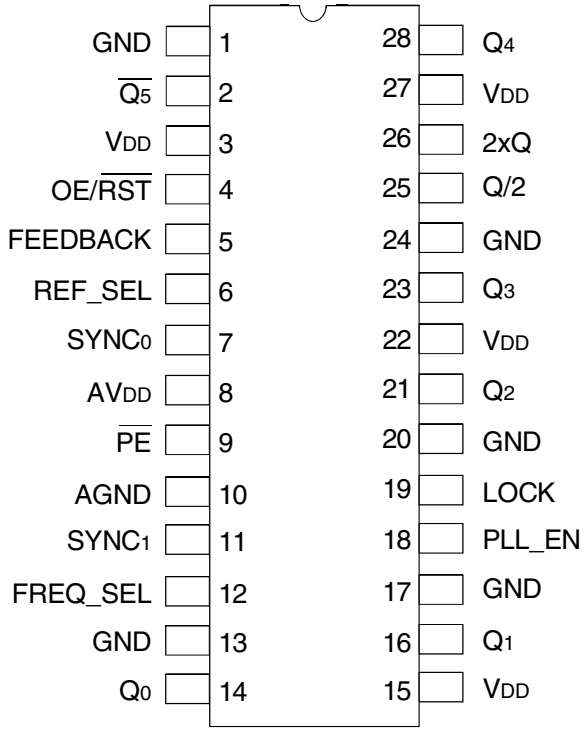
The QS5LV919 Clock Driver uses an internal phase locked loop (PLL) to lock low skew outputs to one of two reference clock inputs. Eight outputs are available: 2xQ, Q_0-Q_4, $\overline{Q_5}$, Q/2. Careful layout and design ensure < 300 ps skew between the Q_0-Q_4, and Q/2 outputs. The QS5LV919 includes an internal RC filter which provides excellent jitter characteristics and eliminates the need for external components. Various combinations of feedback and a divide-by-2 in the VCO path allow applications to be customized for linear VCO operation over a wide range of input SYNC frequencies. The PLL can also be disabled by the PLL_EN signal to allow low frequency or DC testing. The LOCK output asserts to indicate when phase lock has been achieved. The QS5LV919 is designed for use in high-performance workstations, multi-board computers, networking hardware, and mainframe systems. Several can be used in parallel or scattered throughout a system for guaranteed low skew, system-wide clock distribution networks.

For more information on PLL clock driver products, see Application Note AN-227.

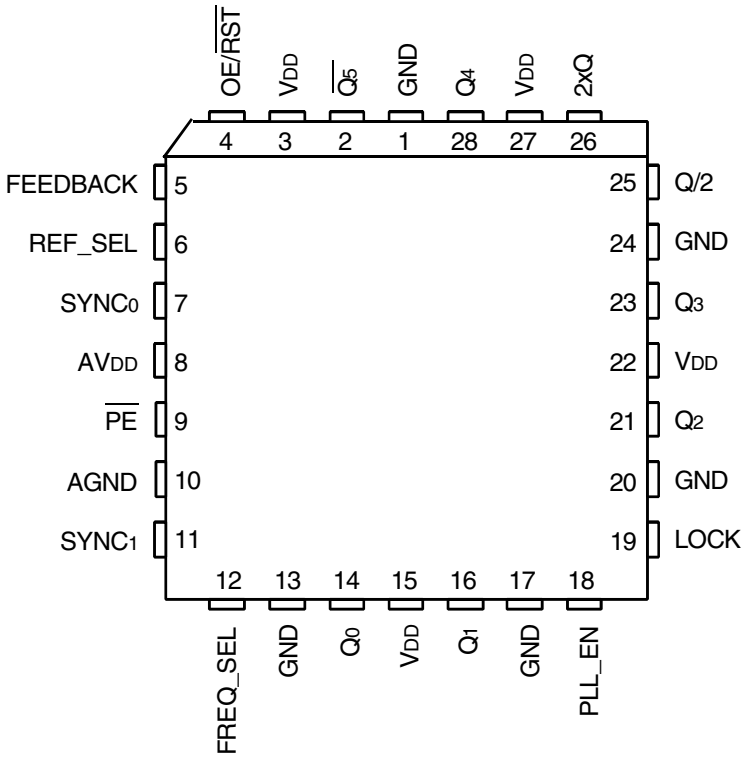
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QSOP
TOP VIEW



PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating		Max.	Unit
V_{DD}, AV_{DD}	Supply Voltage to Ground		–0.5 to +7	V
	DC Input Voltage V_{IN}		–0.5 to +5.5	V
	Maximum Power	QSOP	655	mW
	Dissipation (T_A = 85°C)	PLCC	770	mW
T_{STG}	Storage Temperature Range		–65 to +150	°C

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = 25°C, f = 1MHz, V_{IN} = 0V)

	QSOP		PLCC		
Parameter	Typ.	Max.	Typ.	Max.	Unit
C_{IN}	3	4	4	6	pF

PIN DESCRIPTION

Pin Name	I/O	Description
$SYNC_0$	I	Reference clock input
$SYNC_1$	I	Reference clock input
REF_SEL	I	Reference clock select. When 1, selects $SYNC_1$. When 0, selects $SYNC_0$.
FREQ_SEL	I	VCO frequency select. For choosing optimal VCO operating frequency depending on input frequency.
FEEDBACK	I	PLL feedback input which is connected to a user selected output pin. External feedback provides flexibility for different output frequency relationships. See the Frequency Selection Table for more information.
Q_0 -Q_4	O	Clock outputs
Q_5	O	Clock output. Matched in frequency, but inverted with respect to Q.
2xQ	O	Clock output. Matched in phase, but frequency is double the Q frequency.
Q/2	O	Clock output. Matched in phase, but frequency is half the Q frequency.
LOCK	O	PLL lock indication signal. 1 indicates positive lock. 0 indicates that the PLL is not locked and outputs may not be synchronized to the inputs.
OE/$\overline{RST}$	I	Output enable/asynchronous reset. Resets all output registers. When 0, all outputs are held in a tri-stated condition. When 1, outputs are enabled.
PLL_EN	I	PLL enable. Enables and disables the PLL. Useful for testing purposes.
$\overline{PE}$	I	When $\overline{PE}$ is LOW, outputs are synchronized with the positive edge of SYNC. When HIGH, outputs are synchronized with the negative edge of SYNC.
V_{DD}	—	Power supply for output buffers.
AV_{DD}	—	Power supply for phase lock loop and other internal circuitries.
GND	—	Ground supply for output buffers.
AGND	—	Ground supply for phase lock loop and other internal circuitries.

OUTPUT FREQUENCY SPECIFICATIONS

Industrial: T_A = –40°C to +85°C, AV_{DD} / V_{DD} = 3.3V ± 0.3V

Symbol	Description	–55	–70	–100	–133	–160	Units
F_{MAX_2XQ}	Max Frequency, 2xQ	55	70	100	133	160	MHz
F_{MAX_Q}	Max Frequency, Q_0 - Q_4, Q_5	27.5	35	50	66.5	80	MHz
$F_{MAX\_Q/2}$	Max Frequency, Q/2	13.75	17.5	25	33.25	40	MHz
F_{MIN_2XQ}	Min Frequency, 2xQ	20	20	20	20	20	MHz
F_{MIN_Q}	Min Frequency, Q_0 - Q_4, Q_5	10	10	10	10	10	MHz
$F_{MIN\_Q/2}$	Min Frequency, Q/2	5	5	5	5	5	MHz

FREQUENCY SELECTION TABLE

FREQ_SEL	Output Used for Feedback	SYNC (MHz) (allowable range)(1)		Output Frequency Relationships(2)			
		Min.	Max	Q/2	Q5	Q0 - Q4	2XQ
HIGH	Q/2	$F_{MIN\_Q/2}$	$F_{MAX\_Q/2}$	SYNC	– SYNC X 2	SYNC X 2	SYNC X 4
HIGH	Q0 -Q4	F_{MIN_Q}	F_{MAX_Q}	SYNC / 2	– SYNC	SYNC	SYNC X 2
HIGH	Q5	F_{MIN_Q}	F_{MAX_Q}	– SYNC / 2	SYNC	– SYNC	– SYNC X 2
HIGH	2xQ(3)	F_{MIN_2XQ}	100	SYNC / 4	– SYNC / 2	SYNC / 2	SYNC
LOW	Q/2	$F_{MIN\_Q/2}$/2	$F_{MAX\_Q/2}$/2	SYNC	– SYNC X 2	SYNC X 2	SYNC X 4
LOW	Q0 -Q4	F_{MIN_Q} /2	F_{MAX_Q} /2	SYNC / 2	– SYNC	SYNC	SYNC X 2
LOW	Q5	F_{MIN_Q} /2	F_{MAX_Q} /2	– SYNC / 2	SYNC	– SYNC	– SYNC X 2
LOW	2xQ	F_{MIN_2XQ} /2	F_{MAX_2XQ} /2	SYNC / 4	– SYNC / 2	SYNC / 2	SYNC

NOTES:

1. Operation in the specified SYNC frequency range guarantees that the VCO will operate in its optimal range of 20MHz to F_{MAX_2xQ}. Operation with Sync inputs outside specified frequency ranges may result in out-of-lock outputs. FREQ_SEL only affects VCO frequency and does not affect output frequencies.
2. The lock output pin (LOCK) may not indicate reliably for VCO frequencies below 30MHz.
3. The 2xQ is limited to a maximum frequency (F_{MAX_2XQ}) of 100MHz only when used as a feedback.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified
Industrial: T_A = -40°C to +85°C, AV_{DD}/V_{DD} = 3.3V ± 0.3V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	—	—	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = –24mA	V_{DD} – 0.6	—	—	V
		I_{OH} = –100µA	V_{DD} – 0.2	—	—	
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 24mA	—	—	0.45	V
		V_{DD} = Min., I_{OL} = 100µA	—	—	0.2	
V_H	Input Hysteresis	—	—	100	—	mV
I_{OZ}	Output Leakage Current	V_{OUT} = V_{DD} or GND, V_{DD} = Max.	—	—	± 5	µA
I_{IN}	Input Leakage Current	AV_{DD} = Max., V_{IN} = AV_{DD} or GND	—	—	± 5	µA
I_{PD}	Input Pull-Down Current ($\overline{PE}$)	AV_{DD} = Max., V_{IN} = AV_{DD}	—	—	± 100	µA

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions	Typ.	Max.	Unit
I_{DDQ}	Quiescent Power Supply Current	V_{DD} = Max., OE/$\overline{RST}$ = LOW, SYNC = LOW, All outputs unloaded		1	mA
ΔI_{DD}	Power Supply Current per Input HIGH	V_{DD} = Max., V_{IN} = 3V	1	30	µA
I_{DDD}	Dynamic Power Supply Current (1)	V_{DD} = Max., C_L = 0pF	0.2	0.4	mA/MHz

NOTE:

1. Relative to the frequency of Q outputs.

INPUT TIMING REQUIREMENTS

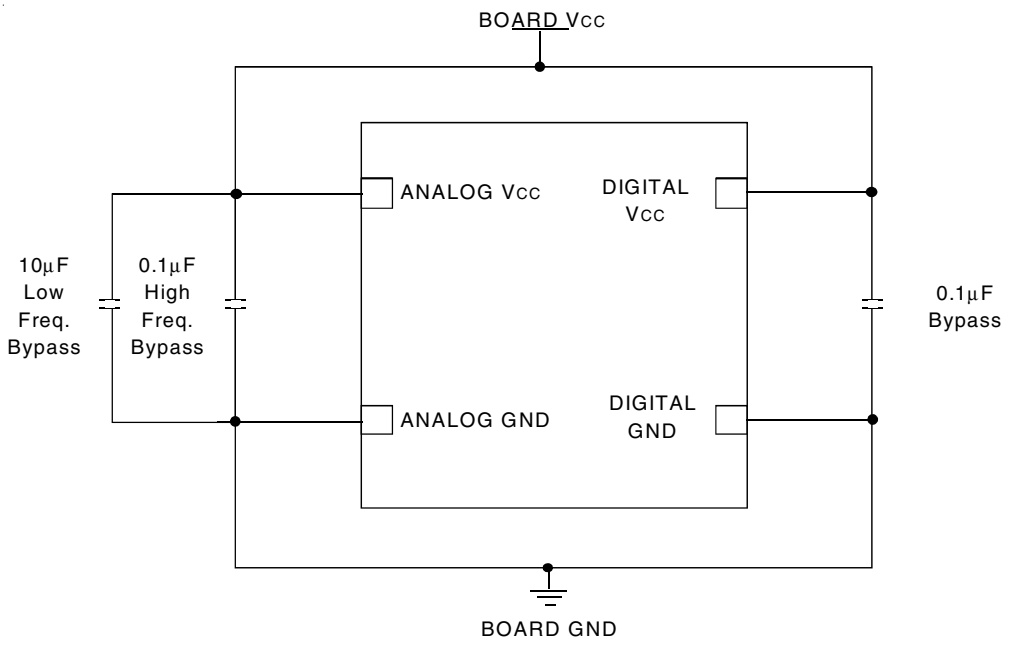
Symbol	Description[1]	Min.	Max.	Unit
t_R, t_F	Maximum input rise and fall times, 0.8V to 2V	—	3	ns
F_I	Input Clock Frequency, $SYNC_0$, $SYNC_1$[1]	2.5	100	MHz
t_{PWC}	Input clock pulse, HIGH or LOW[2]	2	—	ns
D_H	Input duty cycle, $SYNC_0$, $SYNC_1$[2]	25	75	%

NOTES:
1. See Output Frequency and Frequency Selection tables for more detail on allowable SYNC input frequencies for different speed grades with different FEEDBACK and FREQ_SEL combinations.
2. Where pulse witdh implied by D_H is less than t_{WPC} limit, t_{WPC} limit applies

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter[1]	Min.	Max.	Unit
t_{SKR}	Output Skew Between Rising Edges, Q_0-Q_4 (and $Q/2$ if $\overline{PE}$ = LOW)[2]	—	300	ps
t_{SKF}	Output Skew Between Falling Edges, Q_0-Q_4 (and $Q/2$ if $\overline{PE}$ = HIGH)[2]	—	300	ps
t_{SKALL}	Output Skew, All Outputs[2,5]	—	500	ps
t_{PW}	Pulse Width, 2xQ output, >40MHz	$T_{CY}/2 - 0.4$	$T_{CY}/2 + 0.4$	ns
t_{PW}	Pulse Width, Q_0-Q_4, Q_5, Q/2 outputs, 80MHz	$T_{CY}/2 - 0.4$	$T_{CY}/2 + 0.4$	ns
t_J	Cycle-to-Cycle Jitter[4]	−0.15	0.15	ns
t_{PD}	SYNC Input to Feedback Delay[6]	−500	0	ps
t_{LOCK}	SYNC to Phase Lock	—	10	ms
t_{PZH} t_{PZL}	Output Enable Time, OE/$\overline{RST}$ LOW to HIGH[3]	0	14	ns
t_{PHZ} t_{PLZ}	Output Disable Time, OE/$\overline{RST}$ HIGH to LOW[3]	0	14	ns
t_R, t_F	Output Rise/Fall Times, 0.8V ~ 2V	0.3	2	ns

NOTES:
1. See Test Loads and Waveforms for test load and termination.
2. Skew specifications apply under identical environments (loading, temperature, V_{DD}, device speed grade).
3. Measured in open loop mode PLL_EN = 0.
4. Jitter is characterized with Q output at 20MHz. See Frequency Selection Table for information on proper FREQ_SEL level for specified input frequencies.
5. Skew measured at selected synchronization edge.
6. t_{PD} measured at device inputs at $0.5V_{DD}$, Q output at 80MHz.



A separate Analog power supply is not necessary and should not be used. Following these prescribed guidelines is all that is necessary to use the QS5LV919 in a normal digital environment.

Figure 1. Recommended Analog Isolation Scheme for the QS5LV919

NOTES:

1. Figure 1 shows an analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter-free operation:

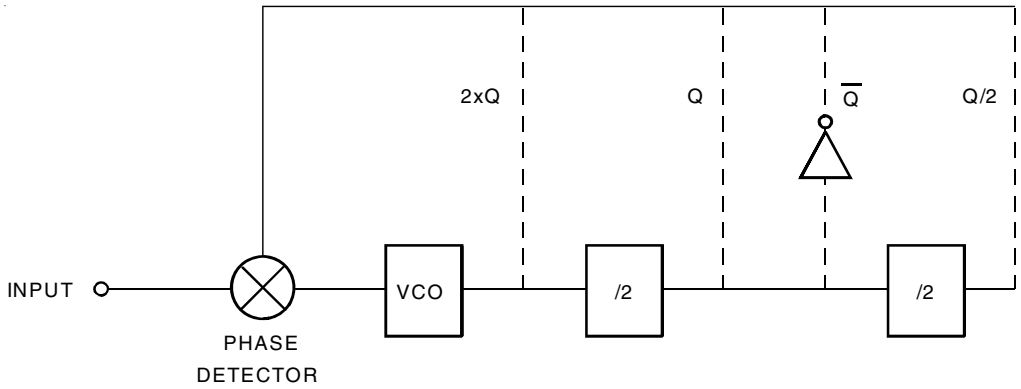
   a. All analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients.
   b. The 10µF low frequency bypass capacitor and the 0.1µF high frequency bypass capacitor form a wide bandwidth filter that will minimize the QS5LV919's sensitivity to voltage transients from the system digital Vcc supply and ground planes.
   If good bypass techniques are used on a board design near components which may cause digital Vcc and ground noise, Vcc step deviations should not occur at the QS5LV919's digital Vcc supply. The purpose of the bypass filtering scheme shown in figure 1 is to give the QS5LV919 additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

2. The bypass capacitors can be ceramic chip capacitors. There should be a 0.1µF bypass capacitor between each of the other (digital) four Vcc pins and the board ground plane. This will reduce output switching noise caused by the QS5LV919 outputs, in addition to reducing potential for noise in the "analog" section of the chip. These bypass capacitors should also be tied as close to the QS5LV919 package as possible.

PLL OPERATION

The Phase Locked Loop (PLL) circuit included in the QS5LV919 provides for replication of incoming SYNC clock signals. Any manipulation of that signal, such as frequency multiplying or inversion is performed by digital logic following the PLL (see the block diagram). The key advantage of the PLL circuit is to provide an effective zero propagation delay between the output and input signals. In fact, adding delay circuits in the feedback path, 'propagation delay' can even be negative! A simplified schematic of the QS5LV919 PLL circuit is shown below.

SIMPLIFIED DIAGRAM OF QS5LV919 FEEDBACK



The phase difference between the output and the input frequencies feeds the VCO which drives the outputs. Whichever output is fed back, it will stabilize at the same frequency as the input. Hence, this is a true negative feedback closed loop system. In most applications, the output will optimally have zero phase shift with respect to the input. In fact, the internal loop filter on the QS5LV919 typically provides within 150ps of phase shift between input and output.

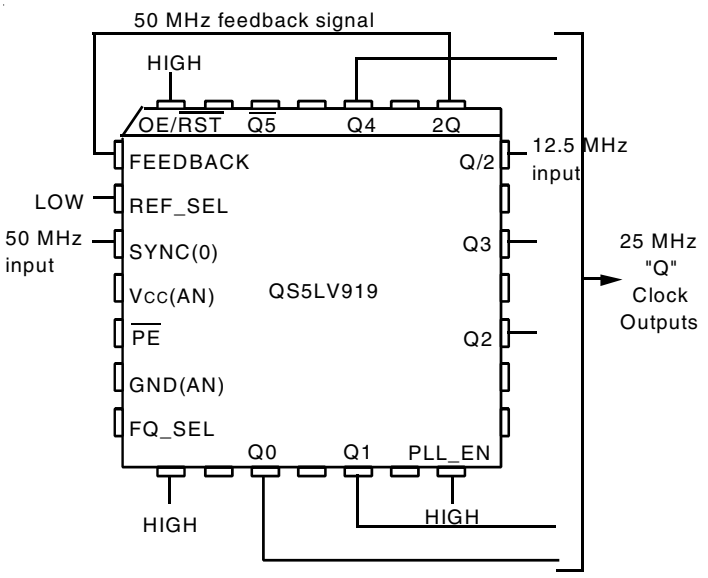
If the user wishes to vary the phase difference (typically to compensate for backplane delays), this is most easily accomplished by adding delay circuits to the feedback path. The respective output used for feedback will be advanced by the amount of delay in the feedback path. All other outputs will retain their proper relationships to that output.

The frequency relationship shown here is applicable to all Q outputs (Q0, Q1, Q2, Q3 and Q4).

2:1 INPUT TO "Q" OUTPUT FREQUENCY RELATIONSHIP

In this application, the 2Q output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of 2Q and SYNC, thus the 2Q frequency will equal the SYNC frequency. The Q/2 output will always run at 1/4 the 2Q frequency, and the Q output will run at 1/2 the 2Q frequency.

Note that with 2Q as feedback, the maximum input frequency is 100MHz for FS = HIGH

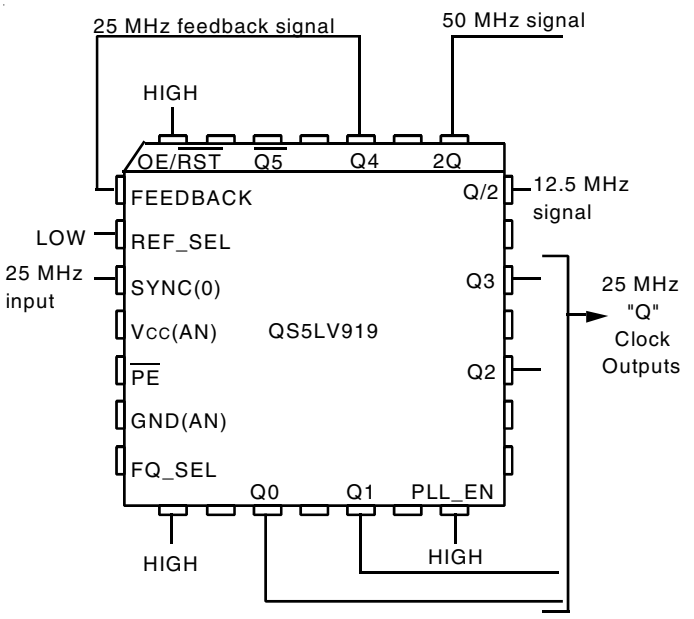


Allowable Input Frequency Range:
40MHz to (f2Q MAX Spec) (for FREQ_SEL HIGH)
20MHz to (f2Q MAX Spec)/2 (for FREQ_SEL LOW)

Figure 2a. Wiring Diagram and Frequency Relationships with 2Q Output Feedback

1:1 INPUT TO "Q" OUTPUT FREQUENCY RELATIONSHIP

In this application, the Q4 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q4 and SYNC, thus the Q4 frequency (and the rest of the "Q" outputs) will equal the SYNC frequency. The Q/2 output will always run at 1/2 the Q frequency, and the 2Q output will run at 2X the Q frequency.

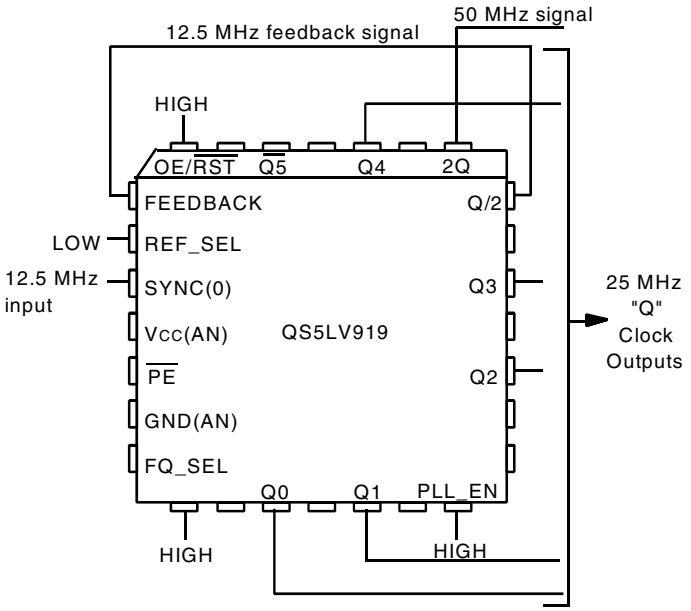


Allowable Input Frequency Range:
20MHz to (f2Q MAX Spec)/2 (for FREQ_SEL HIGH)
10MHz to (f2Q MAX Spec)/4 (for FREQ_SEL LOW)

Figure 2b. Wiring Diagram and Frequency Relationships with Q4 Output Feedback

1:2 INPUT TO "Q" OUTPUT FREQUENCY RELATIONSHIP

In this application, the Q/2 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q/2 and SYNC, thus the Q/2 frequency will equal the SYNC frequency. The Q outputs (Q0-Q4, $\overline{Q5}$) will always run at 2X the Q/2 frequency, and the 2Q output will run at 4X the Q/2 frequency.



Allowable Input Frequency Range:
10MHz to (f2Q MAX Spec)/4 (for FREQ_SEL HIGH)
5MHz to (f2Q MAX Spec)/8 (for FREQ_SEL LOW)

Figure 2c. Wiring Diagram and Frequency Relationships with Q2 Output Feedback

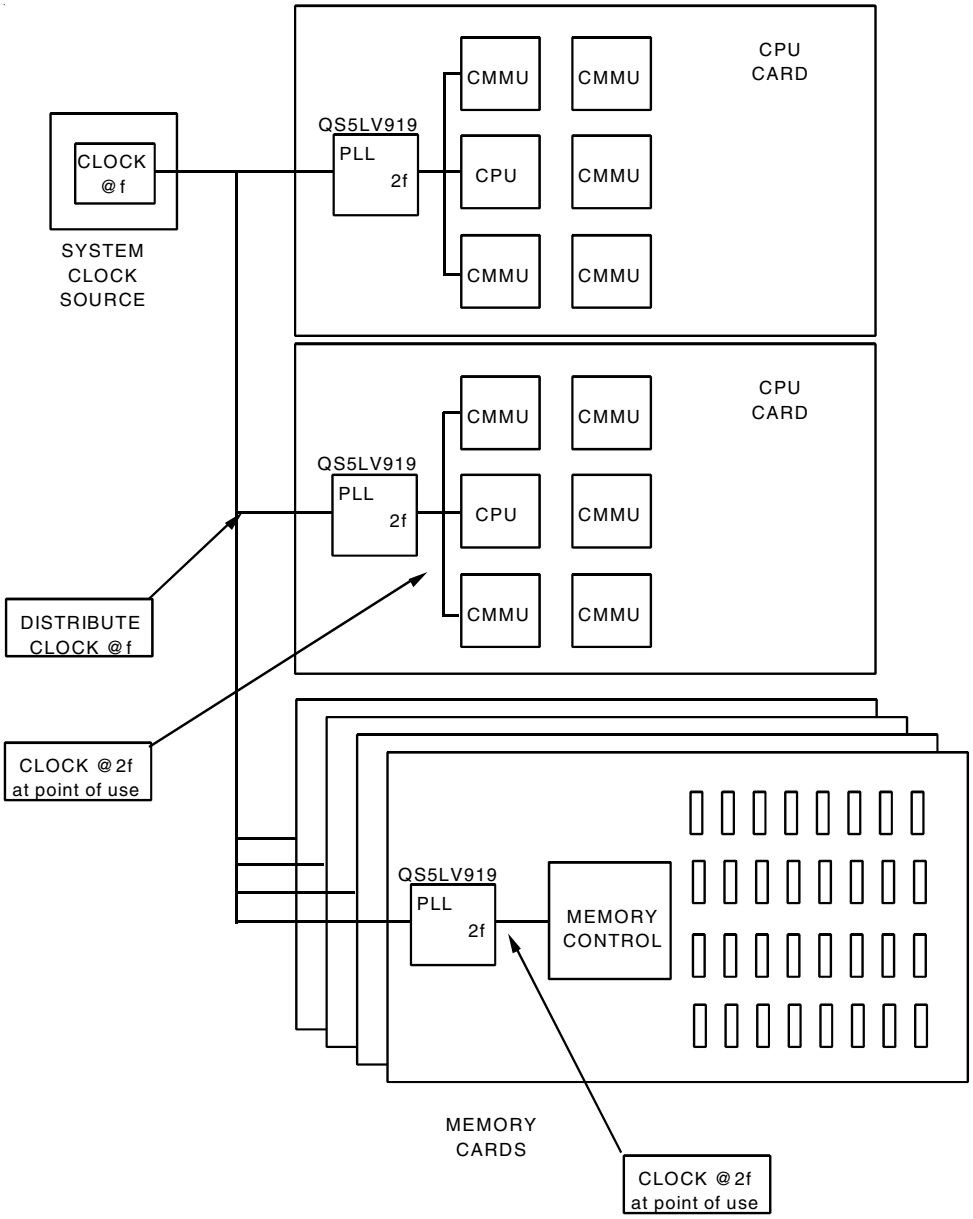


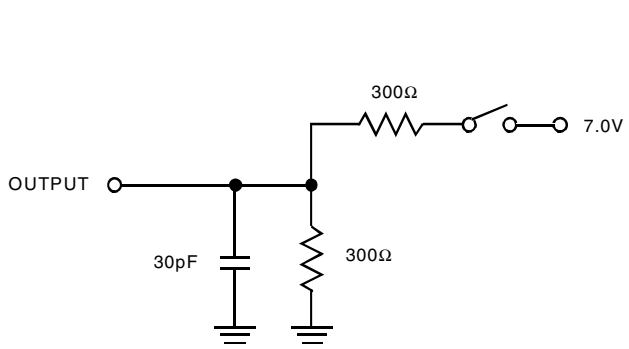
Figure 3. Multiprocessing Application Using the QS5LV919 for Frequency Multiplication and Low Board-to-Board skew

QS5LV919 System Level Testing Functionality

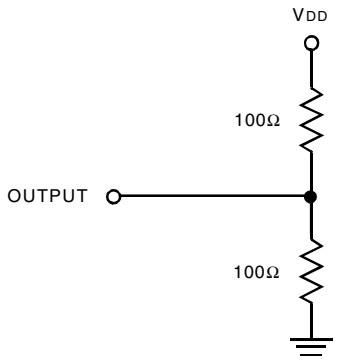
When the PLL_EN pin is LOW, the PLL is bypassed and the QS5LV919 is in low frequency "test mode". In test mode (with FREQ_SEL HIGH), the 2Q output is inverted from the selected SYNC input, and the Q outputs are divide-by-2 (negative edge triggered) of the SYNC input, and the Q/2 output is divide-by-4 (negative edge triggered). With FREQ_SEL LOW the 2Q output is divide-by-2 of the SYNC, the Q outputs divide-by-4, and the Q/2 output divide-by-8. These relationships can be seen in the block diagram. A recommended test configuration would be to use SYNC0 or SYNC1 as the test clock input, and tie PLL_EN and REF_SEL together and connect them to the test select logic.

This functionality is needed since most board-level testers run at 1 MHz or below, and the QS5LV919 cannot lock onto that low of an input frequency. In the test mode described above, any test frequency test can be used.

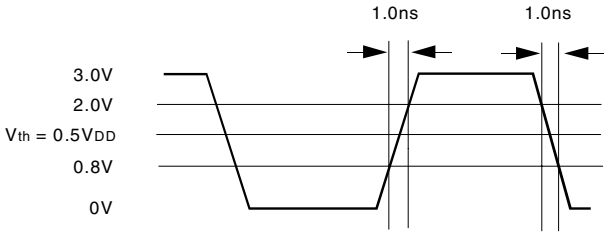
AC TEST LOADS AND WAVEFORMS



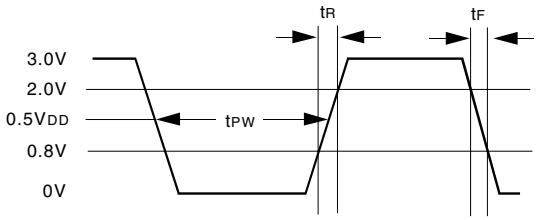
TEST CIRCUIT 1



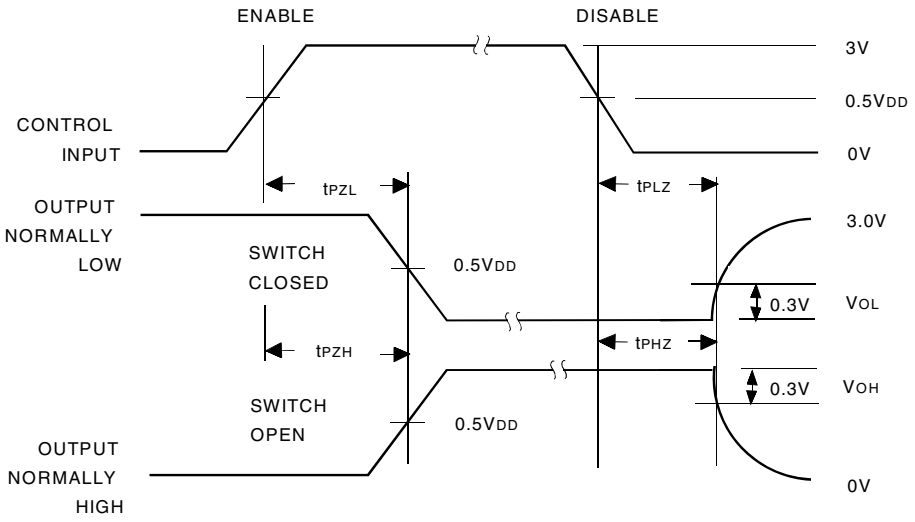
TEST CIRCUIT 2



LVTTL INPUT TEST WAVEFORM



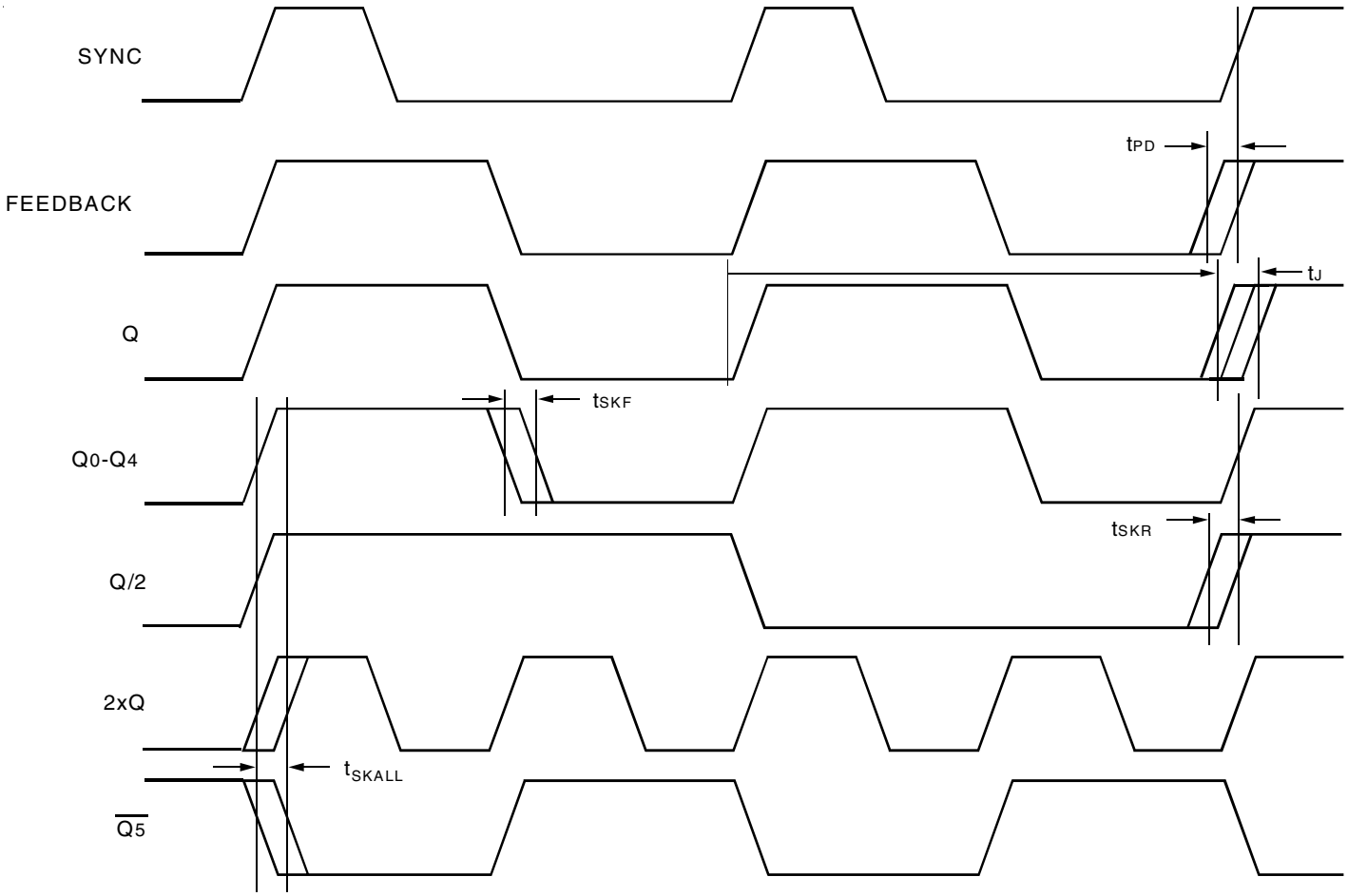
LVTTL OUTPUT WAVEFORM



ENABLE AND DISABLE TIMES

TEST CIRCUIT 1 is used for output enable/disable parameters.
TEST CIRCUIT 2 is used for all other timing parameters.

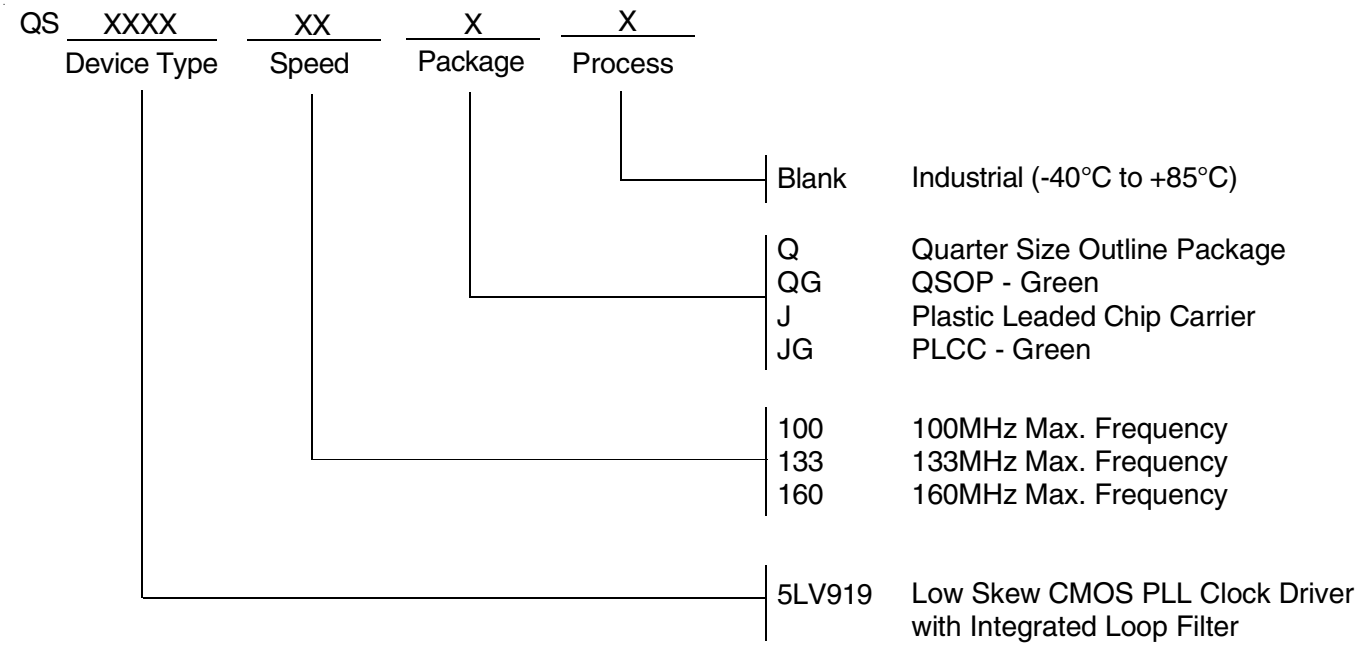
AC TIMING DIAGRAM



NOTES:

1. AC Timing Diagram applies to Q output connected to FEEDBACK and PE = GND. For PE = V_{DD}, the negative edge of FEEDBACK aligns with the negative edge of SYNC input, and the negative edges of the multiplied and divided outputs align with the negative edge of SYNC.
2. All parameters are measured at $0.5V_{DD}$.

ORDERING INFORMATION



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