FAST CMOS OCTAL REGISTERED TRANSCEIVER

IDT29FCT52AT/CT

FEATURES:

- A and C grades
- Low input and output leakage ≤1µA (max.)
- CMOS power levels
- True TTL input and output compatibility:
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High Drive outputs (-15mA I_{OH}, 64mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Power off disable outputs permit "live insertion"
- Available in SOIC and QSOP packages

DESCRIPTION:

The IDT29FCT52T is an 8-bit registered transceiver built using an advanced dual metal CMOS technology. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-state output enable signals are provided for each register. Both A outputs and B outputs are guaranteed to sink 64mA.
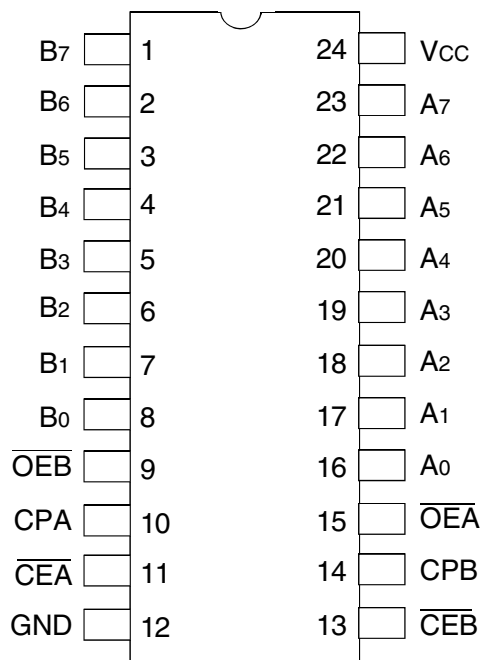
FUNCTIONAL BLOCK DIAGRAM
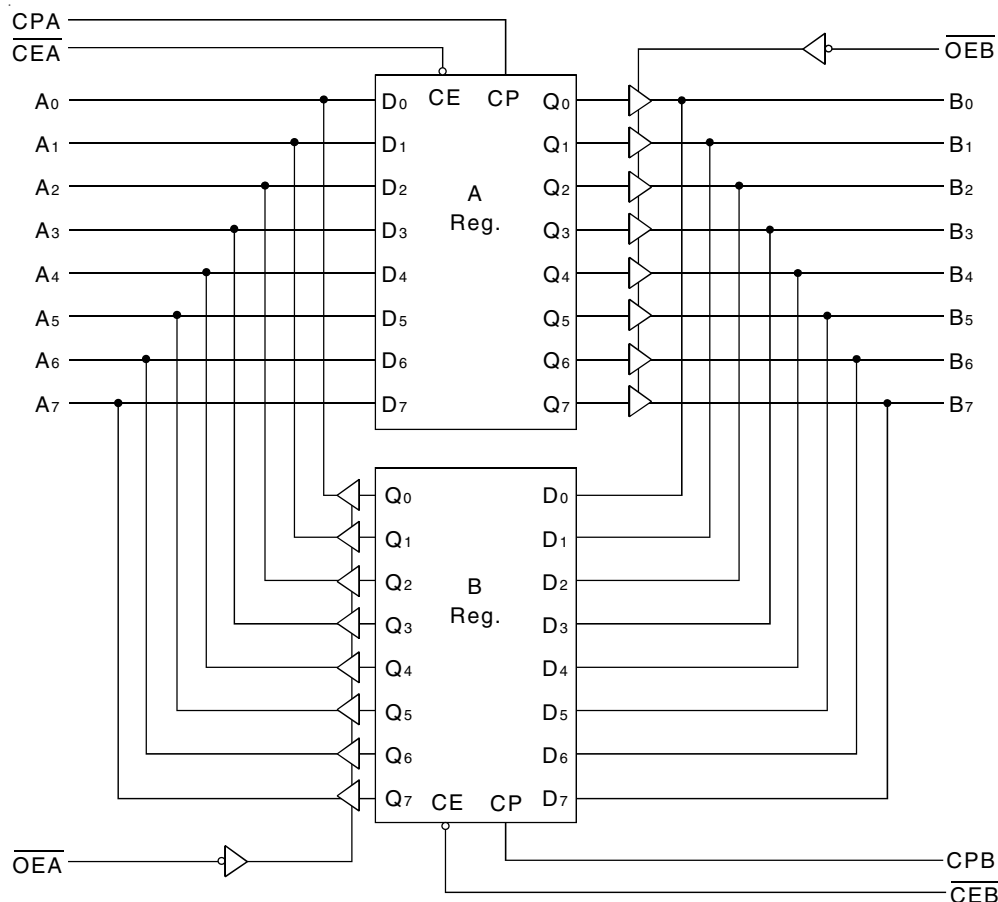
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INDUSTRIAL TEMPERATURE RANGE

FEBRUARY 2006

DSC-5483/3

PIN CONFIGURATION

B7	1	24	VCC
B6	2	23	A7
B5	3	22	A6
B4	4	21	A5
B3	5	20	A4
B2	6	19	A3
B1	7	18	A2
B0	8	17	A1
$\overline{OEB}$	9	16	A0
CPA	10	15	$\overline{OEA}$
$\overline{CEA}$	11	14	CPB
GND	12	13	$\overline{CEB}$

SOIC/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Description	Max	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by =0.5V unless otherwise noted.
2. All device terminals.

CAPACITANCE $(T_A = +25°C, F = 1.0MHz)$

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

REGISTER FUNCTION TABLE [1]

(Applies to A or B Register)

Inputs			Internal	
D	CP	$\overline{CE}$	Q	Function
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   NC = No Change
   ↑ = LOW-to-HIGH Transition

OUTPUT CONTROL [1]

	Internal		
$\overline{OE}$	Q	Y-Outputs	Function
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance

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PIN DESCRIPTION

Name	I/O	Description
A0-7	I/O	Eight bidirectional lines carrying the A Register inputs or B Register outputs.
B0-7	I/O	Eight bidirectional lines carrying the B Register inputs or A Register outputs.
CPA	I	Clock for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal.
$\overline{CEA}$	I	Clock Enable for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal. When $\overline{CEA}$ is HIGH, the A Register holds its contents, regardless of CPA signal transitions.
$\overline{OEB}$	I	Output Enable for the A Register. When $\overline{OEB}$ is LOW, the A Register outputs are enabled onto the B0-7 lines. When $\overline{OEB}$ is HIGH, the B0-7 outputs are in the high-impedance state.
CPB	I	Clock for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal.
$\overline{CEB}$	I	Clock Enable for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal. When $\overline{CEB}$ is HIGH, the B Register holds its contents, regardless of CPB signal transitions.
$\overline{OEA}$	I	Output Enable for the B Register. When $\overline{OEA}$ is LOW, the B Register outputs are enabled onto the A0-7 lines. When $\overline{OEA}$ is HIGH, the A0-7 outputs are in the high-impedance state.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5.0V \pm 5\%$

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	μA
I_{IL}	Input LOW Current[4]	V_{CC} = Max.	V_I = 0.5V	—	—	±1	μA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_I = 2.7V	—	—	±1	μA
I_{OZL}	(3-State Output pins)[4]		V_I = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	μA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = −18mA		—	−0.7	−1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	μA

OUTPUT DRIVE CHARACTERISTICS

V_{OH}	Output HIGH Voltage	V_{CC} = Min	I_{OH} = −8mA	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15mA	2	3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min	I_{OL} = 64mA	—	0.3	0.55	V
		V_{IN} = V_{IH} or V_{IL}					
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		−60	−120	−225	mA
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = Max., V_{IN} or $V_O \leq 4.5V$		—	—	±1	μA

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. The test limit for this parameter is ±5μA at T_A = −55°C.
5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ or $\overline{OE}_B$ = GND One Input Togging 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	—	1.5	3.5	mA
		$\overline{OE}_A$ or $\overline{OE}_B$ = GND One Bit Togging at fi = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	2	5.5	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	—	3.8	7.3[5]	
		$\overline{OE}_A$ or $\overline{OE}_B$ = GND Eight Bits Toggling at fi = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	6	16.3[5]	

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
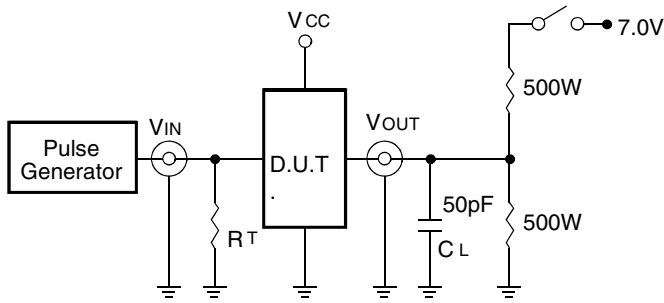All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

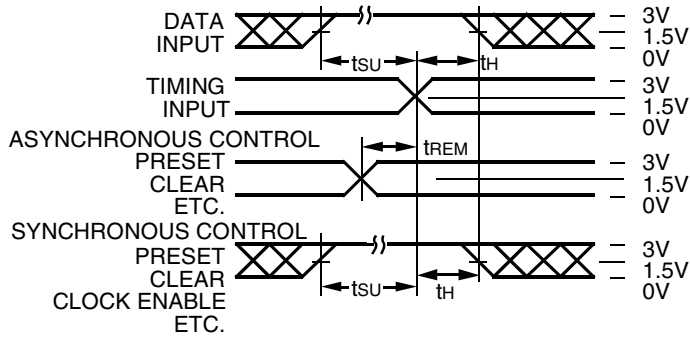| Symbol	Parameter	Condition[1]	29FCT52AT		29FCT52CT		Unit
			Min.[2]	Max.	Min.[2]	Max.	
t_{PLH}	Propagation Delay	$C_L = 50pF$	2	10	2	6.3	ns
t_{PHL}	CPA, CPB to Ax, Bx	$R_L = 500\Omega$					
t_{PZH}	Output Enable Time		1.5	10.5	1.5	7	ns
t_{PZL}	$\overline{OEA}$ or $\overline{OEB}$ to Ax, Bx						
t_{PHZ}	Output Disable Time		1.5	10	1.5	6.5	ns
t_{PLZ}	$\overline{OEA}$ or $\overline{OEB}$ to Ax, Bx						
t_{SU}	Set-up Time, HIGH or LOW		2.5	—	2.5	—	ns
	Ax, Bx to CPA, CPB						
t_H	Hold Time, HIGH or LOW		2	—	1.5	—	ns
	Ax, Bx to CPA, CPB						
t_{SU}	Set-up Time, HIGH or LOW		3	—	3	—	ns
	$\overline{CEA}$, $\overline{CEB}$ to CPA, CPB						
t_H	Hold Time, HIGH or LOW		2	—	2	—	ns
	$\overline{CEA}$, $\overline{CEB}$ to CPA, CPB						
t_W	Clock Pulse Width HIGH or LOW[3]		3	—	3	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This limit is guaranteed but not tested.
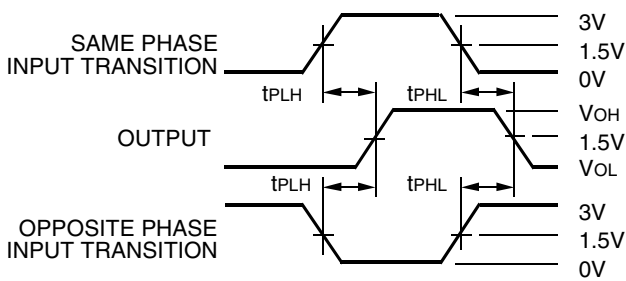
TEST CIRCUITS AND WAVEFORMS

VCC

VIN

Pulse Generator

D.U.T.

RT

VOUT

7.0V

500W

50pF

CL

500W

Octal Link

Test Circuits for All Outputs

DATA INPUT — 3V / 1.5V / 0V

t_{SU} t_H

TIMING INPUT — 3V / 1.5V / 0V

ASYNCHRONOUS CONTROL
PRESET
CLEAR
ETC. — 3V / 1.5V / 0V

t_{REM}

SYNCHRONOUS CONTROL
PRESET
CLEAR
CLOCK ENABLE
ETC. — 3V / 1.5V / 0V

t_{SU} t_H

Octal Link

Set-Up, Hold, and Release Times

SAME PHASE INPUT TRANSITION — 3V / 1.5V / 0V

t_{PLH} t_{PHL}

OUTPUT — VOH / 1.5V / VOL

t_{PLH} t_{PHL}

OPPOSITE PHASE INPUT TRANSITION — 3V / 1.5V / 0V

Octal Link

Propagation Delay

SWITCH POSITION

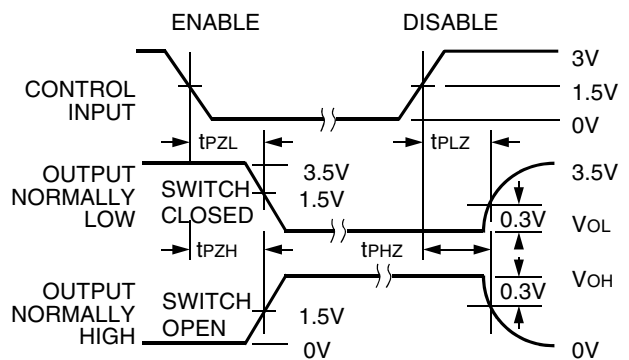| Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

LOW-HIGH-LOW PULSE — 1.5V

t_w

HIGH-LOW-HIGH PULSE — 1.5V

Pulse Width

Octal Link

ENABLE   DISABLE

CONTROL INPUT — 3V / 1.5V / 0V

t_{PZL} t_{PLZ}

OUTPUT NORMALLY LOW
SWITCH CLOSED — 3.5V / 1.5V

t_{PZH} t_{PHZ}

0.3V / VOL

OUTPUT NORMALLY HIGH
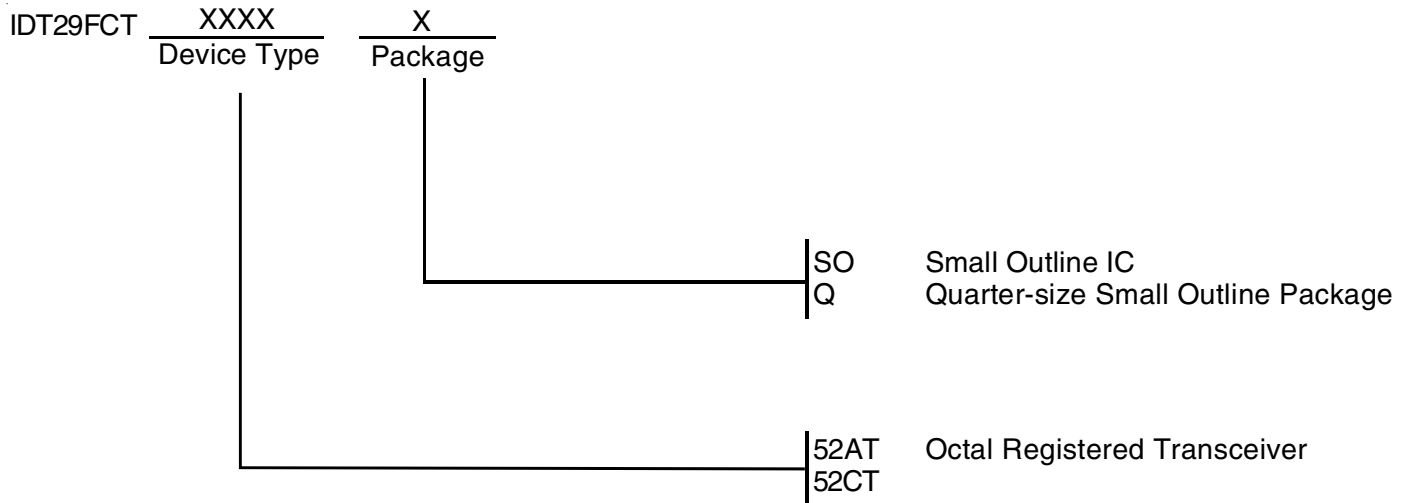SWITCH OPEN — 1.5V / 0V

3.5V / VOH / 0.3V / 0V
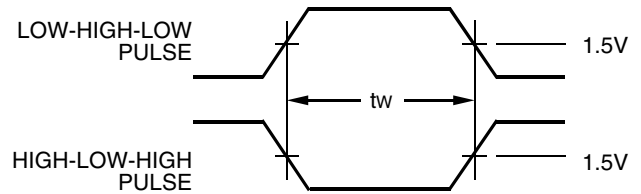
Octal Link

Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

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ORDERING INFORMATION

IDT29FCT <u>XXXX</u>   <u>X</u>
        Device Type   Package

SO   Small Outline IC
Q   Quarter-size Small Outline Package

52AT   Octal Registered Transceiver
52CT