Agilent Technologies
Innovating the HP Way

DC – 2.5 GHz 3 V, High Isolation Silicon RFIC Amplifier

Technical Data

INA-31063

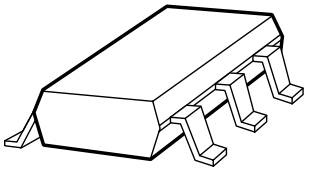
Features

- **High Reverse Isolation -40 dB at 1.9 GHz**
- **Single +3V Supply**
- **15 dB $|S_{21}|^2$ at 1.9 GHz**
- **200 Ω Output Impedance**
- **Ultra-Miniature Package**
- **Unconditionally Stable**

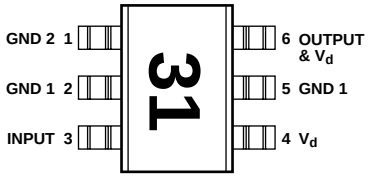
Applications

- **LO Buffer and Amplifier for Cellular, Cordless, Special Mobile Radio, PCS, ISM, Wireless LAN, DBS, TVRO, and TV Tuner**

Surface Mount SOT-363 (SC-70) Package

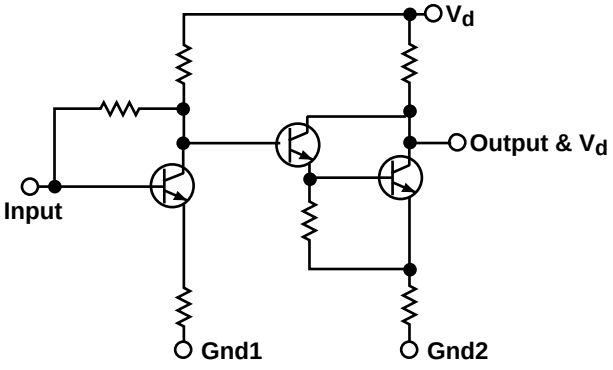


Pin Connections and Package Marking



Note: Package marking provides orientation and identification.

Simplified Schematic



Description

Agilent's INA-31063 is a Silicon RFIC amplifier that has excellent gain and isolation for applications to 2.5 GHz. Packaged in an ultra-miniature SOT-363 package, it requires half the board space of a SOT-143 package.

The INA-31063 uses a unique circuit topology that provides broadband gain and 50 Ω input and 200 Ω output impedance. With more than 35 dB of isolation to 2.5 GHz makes it an excellent candidate for LO buffer applications.

The INA-31063 is fabricated using HP's 30 GHz f_{MAX} ISOSAT™ Silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, and polyimide intermetal dielectric and scratch protection to achieve superior performance, uniformity, and reliability.

Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_d	Device Voltage, output to ground	V	6.0
P_{in}	CW RF Input Power	dBm	+7.0
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
θ_{jc} = 170°C/W

Notes:
1. Operation of this device above any one of these limits may cause permanent damage.
2. T_C = 25°C (T_C is defined to be the temperature at the package pins where contact is made to the circuit board)

INA-31063 Electrical Specifications, T_C = 25°C, Z_O = 50 Ω, V_d = 3 V

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.	Std. Dev.[4]
$\|S_{21}\|^2$	Gain in 50 Ω system	f = 0.9 GHz f = 1.9 GHz f = 2.4 GHz	dB	13.0[3]	14.0 15.1 15.0		0.44
NF_{50}	Noise Figure	f = 1.9 GHz	dB		6.1		0.25
P_{1dB}	Output Power at 1 dB Gain Compression	f = 0.9 GHz f = 1.9 GHz f = 2.4 GHz	dBm		-1.8 -2.1 -3.5		
IP_3	Output Third Order Intercept Point	f = 0.9 GHz f = 1.9 GHz f = 2.4 GHz	dBm		9.1 8.5 6.8		
$VSWR_{in}$	Input VSWR	f = 0.1 – 2.4 GHz			1.35:1		
$VSWR_{out}$	Output VSWR	f = 0.1 – 2.4 GHz			3.5:1		
I_d	Device Current		mA		11.0	13.5[3]	0.47

Notes:
3. Guaranteed specifications are 100% tested in production.
4. Standard deviation number is based on measurement of a large number of parts from three non-consecutive wafer lots during the initial characterization of this product, and is intended to be used as an estimate for distribution of the typical specification.

INA-31063 Typical Performance, T_C = 25°C, Z_O = 50 Ω, V_d = 3 V

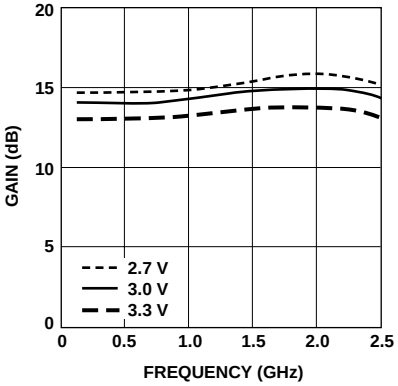


Figure 1. Gain vs. Frequency and Voltage measured in a 50 Ω system.

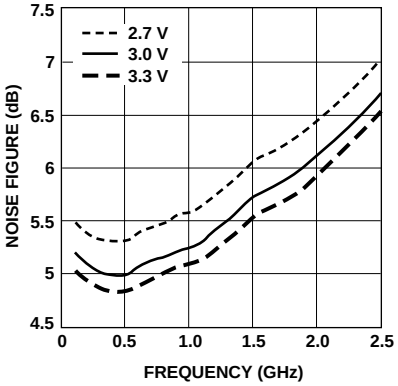


Figure 2. Noise Figure vs. Frequency and Voltage.

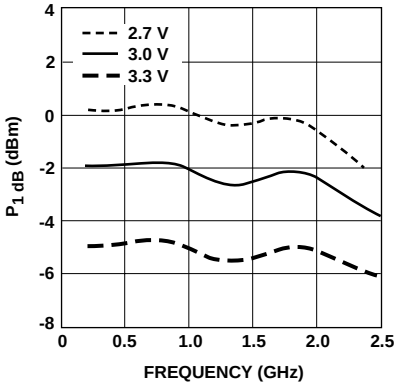


Figure 3. Output Power for 1 dB Gain Compression vs. Frequency and Voltage.

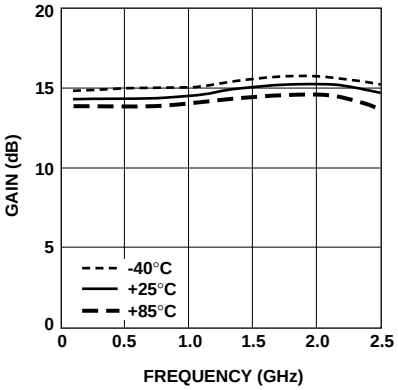


Figure 4. Gain vs. Frequency and Temperature measured in a 50 Ω system.

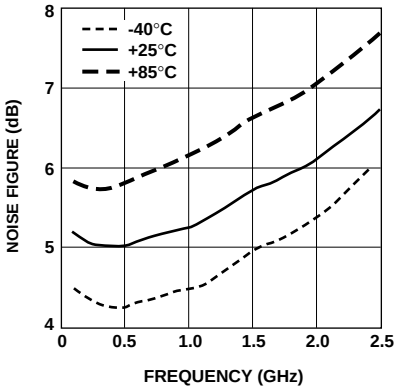


Figure 5. Noise Figure vs. Frequency and Temperature.

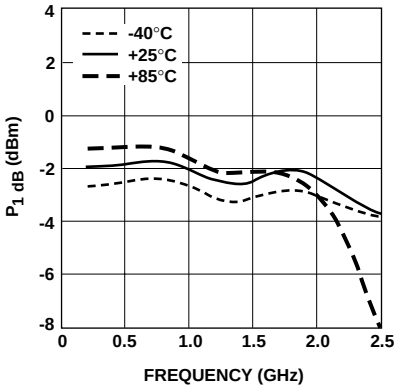


Figure 6. Output Power for 1 dB Gain Compression vs. Frequency and Temperature.

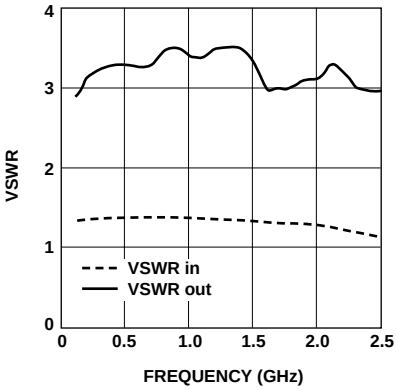


Figure 7. Input and Output VSWR vs. Frequency.

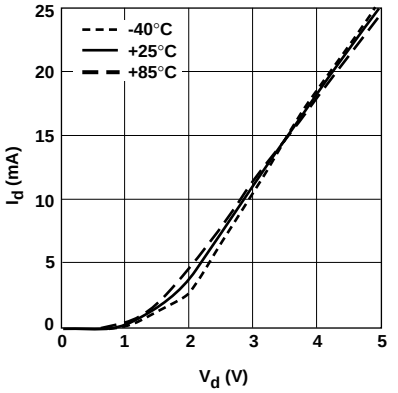


Figure 8. Supply Current vs. Voltage and Temperature.

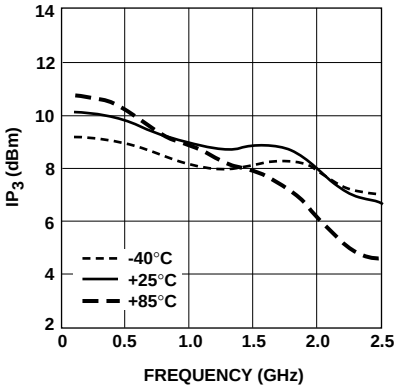


Figure 9. Third Order Intercept Point, IP_3 vs. Frequency and Temperature.

INA-31063 Typical Scattering Parameters[5], T_C = 25°C, Z_O = 50 Ω, V_d = 3.0 V

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang	K Factor
0.1	0.14	171	13.6	4.81	-5	-32.5	0.024	10	0.49	-3	3.45
0.2	0.15	167	13.7	4.84	-11	-37.1	0.014	11	0.52	-4	5.37
0.3	0.14	164	13.7	4.83	-15	-36.0	0.016	-3	0.51	-4	4.79
0.4	0.15	163	13.7	4.86	-20	-37.6	0.013	-39	0.54	-3	5.60
0.5	0.15	152	13.8	4.88	-26	-39.8	0.010	-6	0.53	-5	7.31
0.6	0.14	152	13.8	4.88	-30	-37.1	0.014	-18	0.51	-5	5.38
0.7	0.14	151	13.9	4.93	-35	-38.6	0.012	-35	0.53	-5	6.02
0.8	0.15	147	14.0	4.99	-40	-41.3	0.009	-46	0.55	-8	7.66
0.9	0.14	143	14.0	5.04	-45	-45.5	0.005	-35	0.56	-11	13.54
1.0	0.14	138	14.1	5.06	-51	-45.2	0.005	-4	0.55	-14	13.71
1.1	0.14	137	14.2	5.12	-56	-44.1	0.006	-6	0.54	-17	11.32
1.2	0.13	136	14.3	5.20	-61	-45.3	0.005	-16	0.55	-19	13.20
1.3	0.13	132	14.4	5.26	-67	-47.3	0.004	20	0.55	-24	16.34
1.4	0.13	129	14.5	5.33	-73	-46.8	0.005	40	0.55	-28	12.92
1.5	0.13	125	14.6	5.34	-80	-41.9	0.008	58	0.53	-35	8.32
1.6	0.12	128	14.6	5.36	-85	-41.5	0.008	30	0.49	-36	8.84
1.7	0.12	130	14.8	5.49	-91	-44.3	0.006	27	0.50	-37	11.23
1.8	0.12	130	14.9	5.57	-97	-45.0	0.006	31	0.50	-40	11.18
1.9	0.12	130	15.1	5.69	-104	-46.4	0.005	53	0.51	-44	12.80
2.0	0.11	128	15.2	5.77	-111	-45.8	0.005	61	0.52	-48	12.59
2.1	0.10	129	15.3	5.83	-119	-44.7	0.006	74	0.53	-54	10.20
2.2	0.08	130	15.3	5.79	-127	-43.4	0.007	78	0.52	-62	8.94
2.3	0.07	134	15.1	5.71	-135	-42.4	0.008	79	0.50	-68	8.22
2.4	0.05	144	15.0	5.63	-143	-41.7	0.008	76	0.49	-73	8.42
2.5	0.04	166	14.8	5.50	-152	-41.8	0.008	74	0.49	-80	8.64
2.6	0.04	-176	14.5	5.29	-160	-42.2	0.008	76	0.47	-87	9.24
2.7	0.05	-159	14.1	5.06	-167	-43.2	0.007	77	0.44	-93	11.43
2.8	0.06	-151	13.7	4.84	-174	-43.1	0.007	85	0.40	-97	12.34
2.9	0.08	-149	13.3	4.62	178	-43.3	0.007	86	0.39	-100	13.10
3.0	0.10	-150	12.8	4.36	172	-44.2	0.006	96	0.36	-105	16.46
3.1	0.13	-152	12.3	4.11	165	-44.0	0.006	105	0.34	-108	17.71
3.2	0.15	-153	11.8	3.89	159	-43.0	0.007	115	0.32	-109	16.22
3.3	0.17	-155	11.3	3.65	153	-42.0	0.008	118	0.30	-111	15.17
3.4	0.19	-158	10.7	3.42	147	-42.2	0.008	125	0.29	-113	16.23
3.5	0.21	-160	10.1	3.20	142	-41.3	0.009	139	0.27	-115	15.49
3.6	0.22	-161	9.6	3.02	137	-38.9	0.011	143	0.25	-114	13.50
3.7	0.24	-163	9.1	2.84	132	-38.0	0.013	144	0.24	-114	12.09
3.8	0.25	-165	8.5	2.66	128	-37.3	0.014	151	0.23	-115	12.00
3.9	0.25	-167	8.0	2.51	124	-35.5	0.017	155	0.21	-113	10.55
4.0	0.26	-169	7.5	2.37	120	-34.2	0.019	153	0.21	-111	9.98
4.1	0.27	-172	7.0	2.24	116	-33.2	0.022	153	0.20	-109	9.10
4.2	0.27	-175	6.5	2.12	112	-32.4	0.024	154	0.20	-108	8.83
4.3	0.28	-178	6.1	2.01	109	-31.3	0.027	154	0.19	-105	8.26
4.4	0.29	180	5.6	1.90	105	-30.5	0.030	154	0.19	-103	7.82
4.5	0.29	177	5.1	1.81	102	-29.7	0.033	153	0.19	-101	7.47
4.6	0.30	174	4.7	1.72	98	-28.9	0.036	152	0.19	-99	7.17
4.7	0.31	171	4.3	1.63	95	-28.3	0.039	151	0.19	-98	6.94
4.8	0.32	169	3.8	1.55	92	-27.7	0.041	151	0.19	-97	6.89
4.9	0.33	166	3.4	1.48	89	-27.0	0.045	151	0.19	-95	6.54
5.0	0.33	164	3.0	1.41	87	-26.2	0.049	150	0.19	-93	6.30

Note:

5. Reference plane per Figure 19 in Applications Information section.

INA-31063 Applications Information

Introduction

The INA-31063 is a +3 volt silicon RFIC amplifier that is designed with a two stage internal network to provide a broadband gain and 50 Ω input and 200 Ω output impedance. With a $P_{-1\ dB}$ compressed output power of -3 dBm and high isolation of 40 dB, the INA-31063 is well suited for LO buffer amplifier applications in mobile communication systems.

The 200 Ω output impedance of the amplifier allows easy connections to additional RFICs and some filters.

In addition to use in buffer applications in the cellular market, the INA-31063 will find many applications in battery operated wireless communication systems.

Operating Details

The INA-31063 is a voltage biased device that operates from a +3 volt power supply with a typical current drain of 11 mA. All bias regulation circuitry is integrated into the RFIC. Figure 10 shows a typical implementation of the INA-31063. The supply voltage for the INA-31063 must be applied to two terminals, the V_d pin and the RF Output pin.

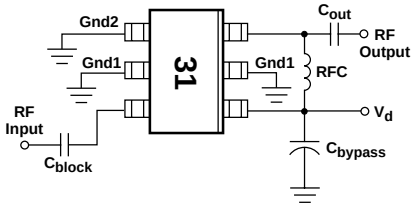


Figure 10. Basic Amplifier Application.

The V_d connection to the amplifier is RF bypassed by placing a capacitor to ground near the V_d pin of the amplifier package. The power supply connection to the RF Output pin is achieved by means of a RF choke (inductor). The value of the RF choke must be large relative to 50 Ω in order to prevent loading of the RF Output. The supply voltage end of the RF choke is bypassed to ground with a capacitor. If the physical layout permits, this can be the same bypass capacitor that is used at the V_d terminal of the amplifier. Blocking capacitors are normally placed in series with the RF Input and the RF Output to isolate the DC voltages on these pins from circuits adjacent to the amplifier. The values for the blocking and bypass capacitors are selected to provide a reactance at the lowest frequency of operation that is small relative to 50 Ω. Since the gain of the INA-31063 extends down to DC, the frequency response of the amplifier is limited only by the values of the capacitors and choke.

RF Layout

An example for the RF layout for the INA-31063 is shown in Figure 11.

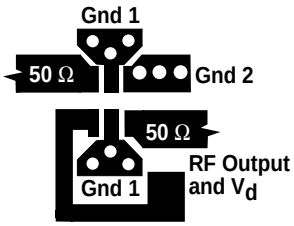


Figure 11. RF Layout

This example uses a microstripline design (solid groundplane on the backside of the circuit board). The circuit board material is 0.031-inch thick FR4. Plated through holes (vias) are used to bring the ground to the top side of the circuit where needed. The performance of INA-31063 is sensitive to ground path inductance. The two-stage design creates the possibility of a feedback loop being formed through the ground returns of the stages, Gnd 1 and Gnd 2.

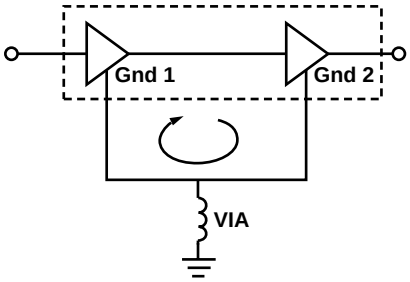


Figure 12. INA-31063 Potential Ground Loop.

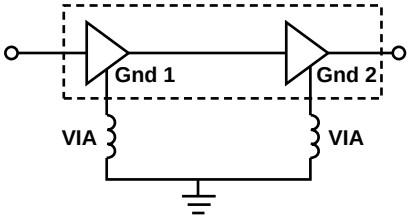


Figure 13. INA-31063 Suggested Layout.

At least one ground via should be placed adjacent to each ground pin to assure good RF grounding. Multiple vias are used to reduce the inductance of the path to ground and should be placed as close to the package terminals as practical.

The effects of the potential ground loop shown in Figure 12 may be observed as a “peaking” in the gain versus frequency response, an increase in input VSWR, or even as return gain at the input of the INA-31063.

Figure 14 shows an assembled 50 Ω amplifier. The +3 volt supply is fed directly into the V_d pin of the INA-31063 and into the RF Output pin through the RF choke (RFC). Capacitor C3 provides RF bypassing for both the V_d pin and the power supply end of the RFC. Capacitor C4 is optional and may be used to add additional bypassing for the V_d line. A well-bypassed V_d line is especially necessary in cascades of amplifier stages to prevent oscillation that may occur as a result of RF feedback through the power supply lines.

900 MHz 50 Ω Matched Example

The use of a simple impedance matching network will typically increase both gain and output power by 1.5 dB and 1.5 dBm, respectively. The values that were chosen for the two tuning elements were a 12 nF series inductor and a 1.0 pF shunt capacitor. The RF choke was a 56 nH (Coilcraft 1008CS-221, TOKO LL2012-F or equivalent). The two blocking capacitors were 100 pF and the bypass capacitor was 1000 pF.

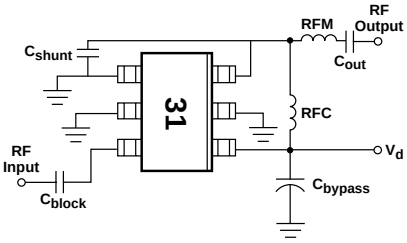


Figure 15. Impedance Matched Output Amplifier Circuit.

These values provide excellent amplifier performance at 900 MHz. Larger values for the choke and capacitors can be used to extend the lower end of the bandwidth. A convenient method for making RF connection to the demonstration board is to use a PCB mounting type of SMA connector (Johnson 142-0701881, or equivalent). These connectors can be slipped over the edge of the PCB and the center conductor soldered to the input and output lines. The ground pins of the connectors can be soldered to the ground plane on the backside of board.

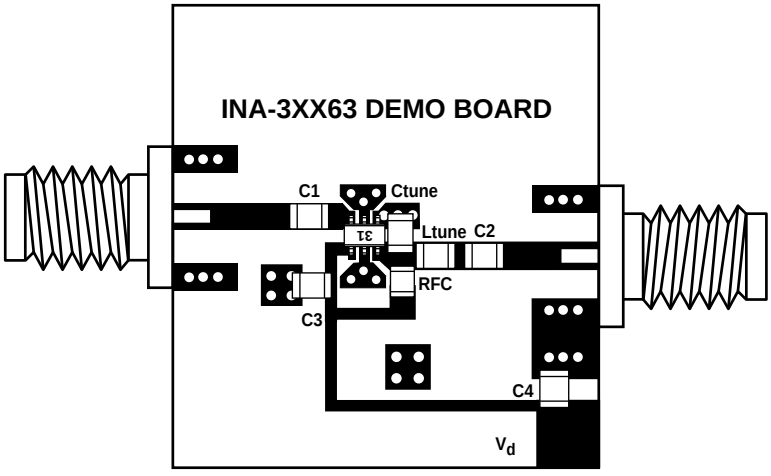


Figure 14. Assembled Amplifier.

Frequency	RFC	RFM	CSHUNT
400 MHz	120 nH	27 nH	2.7 pF
900 MHz	56 nH	12 nH	1.0 pF
1900 MHz	33 nH	4.7 nH	None
2400 MHz	27 nH	1.8 nH	None

Figure 16. Suggested Matching Elements for Common Frequency Bands.

The test results for the INA-31063 were measured on the 50 Ω input and output impedance matched amplifier described above.

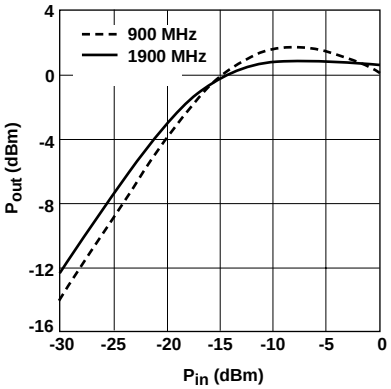


Figure 17. Measured Input Power vs. Output Power on Assembled 50 Ω Amplifier at 900 MHz and 1900 MHz.

An important specification when selecting a LO buffer amplifier is reverse isolation under P_{1dB} input conditions. Figure 18 shows the measured reverse isolation with -10 dBm applied to the input of the device.

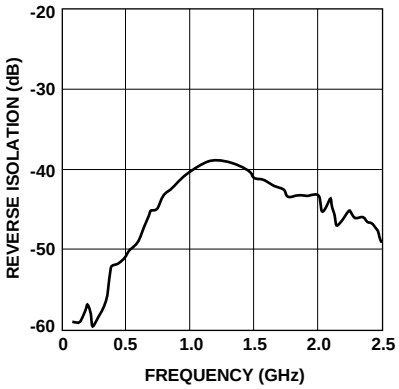


Figure 18. Measured Isolation.

PCB Materials

Typical choices for PCB material for low cost wireless applications are FR-4 or G-10 with a thickness of 0.025 (0.636 mm) or 0.031 inches (0.787 mm). A thickness of 0.062 inches (1.574 mm) is the maximum that is recommended for use with this particular device. The use of a thicker board material increases the inductance of the plated through vias used for RF grounding and may deteriorate circuit performance. Adequate grounding is needed not only to obtain maximum amplifier performance but also to reduce any possibility of instability.

Phase Reference Planes

The positions of the reference planes used to measure S-Parameters for this device are shown in Figure 19. As seen in the illustration, the reference planes are located at the point where the package leads contact the test circuit.

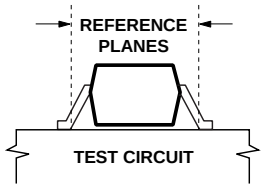


Figure 19. Phase Reference Planes.

SOT-363 PCB Layout

The INA-31063 is packaged in the miniature SOT-363 (SC-70) surface mount package. A PCB pad layout for the SOT-363 package is shown in Figure 20 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding pad parasitics that could impair the high frequency performance of the INA-31063 The layout that is shown with a nominal SOT-363 package footprint superimposed on the PCB pads for reference.

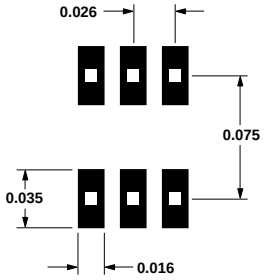


Figure 20. PCB Pad Layout for INA-31063 (dimensions in inches).

Statistical Parameters

Several categories of parameters appear within this data sheet. Parameters may be described with values that are either "minimum or maximum," "typical," or "standard deviations." The values for parameters are based on comprehensive product characterization data, in which automated measurements are made on a large number of parts taken from 3 non-consecutive process lots of semiconductor wafers. The data derived from product characterization tends to be normally distributed, e.g., fits the standard "bell curve." Parameters considered to be the most important to system performance are bounded by minimum or maximum values. For the INA-31063, these parameters are: Power Gain ($|S21|^2$), and the Device Current (I_d). Each of these guaranteed parameters is 100% tested. Values for most of the parameters in the table of Electrical Specifications that are described by typical data are the mathematical mean (μ), of the normal distribution taken from the characterization data. For parameters where measurements or mathematical averaging may not be practical, such as S-parameters or Noise Parameters and the performance curves, the data represents a nominal part taken from the "center" of the characterization distribution. Typical values are intended to be used as a basis for electrical design.

To assist designers in optimizing not only the immediate circuit using the INA-31063, but to also optimize and evaluate trade-offs that affect a complete wireless system, the standard deviation (σ) is provided for three of the Electrical Specifications parameters (at 25°C) in addition to the mean. The standard deviation is a measure of the variability about the mean. It will be recalled that a normal distribution is completely described by the mean and standard deviation. Standard statistics tables or calculations provide the probability of a parameter falling between any two values, usually symmetrically located about the mean. Referring to Figure 21 for example, the probability of a parameter being between ±1σ is 68.3%; between ±2σ is 95.4%; and between ±3σ is 99.7%.

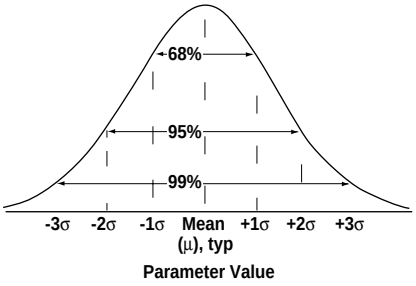


Figure 21. Normal Distribution.

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT-363 package, will reach solder reflow temperatures faster than those with a greater mass.

The INA-31063 has been qualified to the time-temperature profile shown in Figure 22. This profile is representative of an IR reflow type of surface mount assembly process. After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock.

These parameters are typical for a surface mount assembly process for the INA-31063. As a general guideline, the circuit board and components should only be exposed to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

For more information on mounting considerations for packaged microwave semiconductors, please refer to Agilent application note AN-A006.

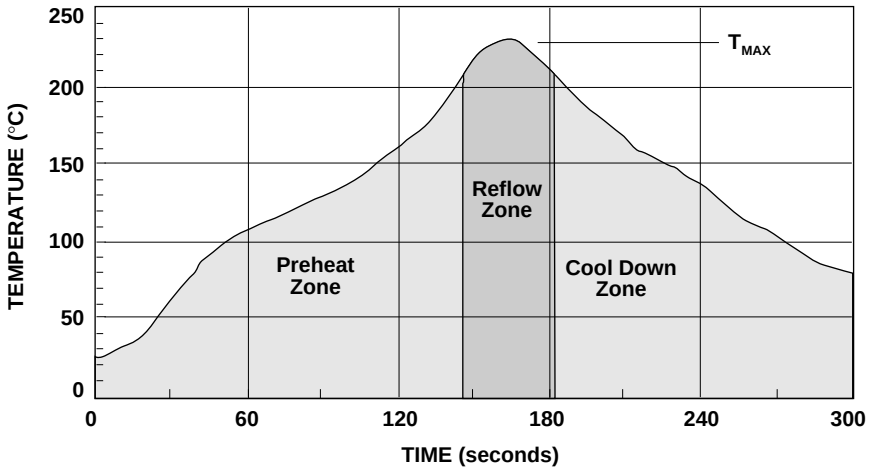


Figure 22. Surface Mount Assembly Profile.

Electrostatic Sensitivity

RFICs are electrostatic discharge (ESD) sensitive devices. Although the INA-31063 is robust in design, permanent damage may occur to these devices if they are subjected to high-energy electrostatic discharges. Electrostatic charges as high as several thousand volts (which readily accumulate on the human body and on test equipment) can discharge without degradation in performance, reliability, or failure. Electronic devices may be subjected to ESD damage in any of the following areas:

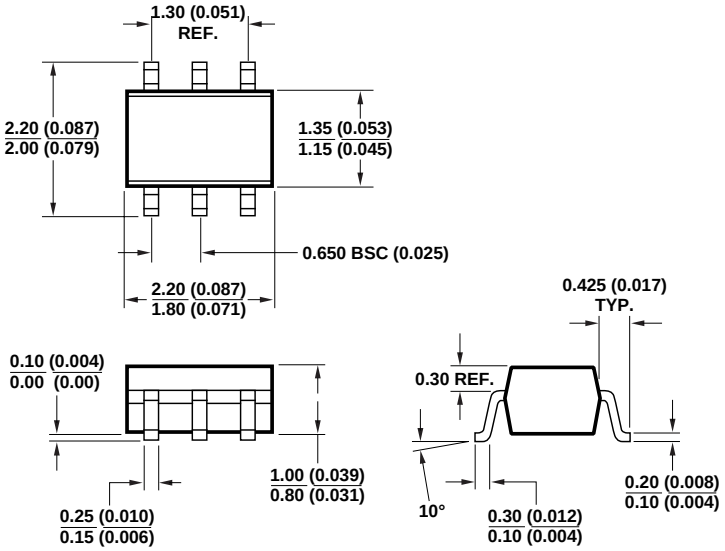
- Storage & handling
- Inspection & testing
- Assembly
- In-circuit use

The INA-31063 is an ESD Class 1 device. Therefore, proper ESD precautions are recommended when handling, inspecting, testing, assembling, and using these devices to avoid damage.

For more information on Electrostatic Discharge and Control refer to Agilent application note AN-A004R.

Package Dimensions

Outline 63 (SOT-363/SC-70)



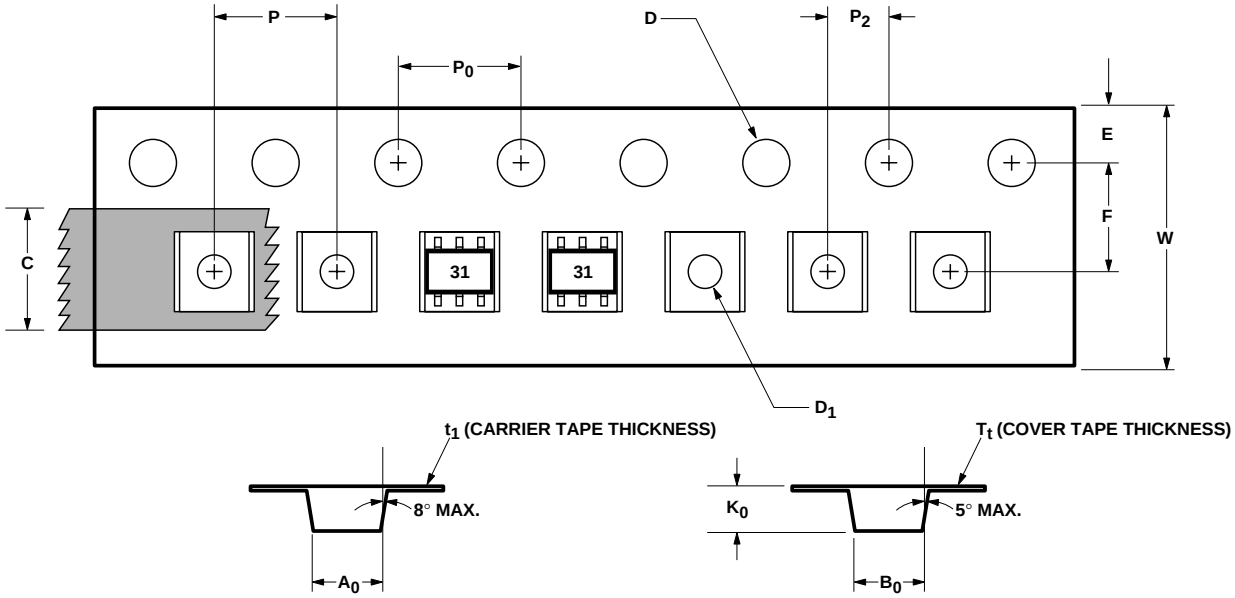
DIMENSIONS ARE IN MILLIMETERS (INCHES)

INA-31063 Part Number Ordering Information

Part Number	Devices per Container	Container
INA-31063-BLK	100	tape strip in antistatic bag
INA-31063-TR1	3,000	7" reel
INA-31063-TR2	10,000	13" reel

Tape Dimensions and Product Orientation

For Outline 63



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

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Data subject to change.

Obsoletes 5967-5770E
5968-1238E (11/99)