National Semiconductor

October 2007

CLC006
Serial Digital Cable Driver with Adjustable Outputs

General Description

National's Comlinear CLC006 is a monolithic, high-speed cable driver designed for the SMPTE 259M serial digital video data transmission standard. The CLC006 drives 75Ω transmission lines (Belden 8281 or equivalent) at data rates up to 400 Mbps. Controlled output rise and fall times (650 ps typical) minimize transition-induced jitter. The output voltage swing, typically 1.65V, set by an accurate, low-drift internal bandgap reference, delivers an 800 mV swing to back-matched and terminated 75Ω cable. Output swing is adjustable from 0.7 V_{P-P} to 2 V_{P-P} using external resistors.

The CLC006's class AB output stage consumes less power than other designs, 185 mW with both outputs terminated, and requires no external bias resistors. The differential inputs accept a wide range of digital signals from 200 mV_{P-P} to ECL levels within the specified common-mode limits. All this make the CLC006 an excellent general purpose high speed driver for digital applications.

The CLC006 is powered from a single +5V or −5.2V supply and comes in an 8-pin SOIC package.

Key Specifications

- 650 ps rise and fall times
- Data rates to 400 Mbps
- 200 mV differential input
- Low residual jitter (25 ps_{pp})

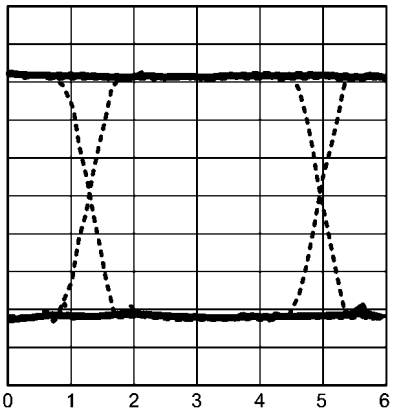
Features

- No external pull-down resistors
- Adjustable output amplitude
- Differential input and output
- Low power dissipation
- Single +5V or −5.2V supply
- Replaces GS9008 in most applications

Applications

- Digital routers and distribution amplifiers
- Coaxial cable driver for digital transmission line
- Twisted pair driver
- Serial digital video interfaces for the commercial and broadcast industry
- SMPTE, Sonet/SDH, and ATM compatible driver
- Buffer applications

270 Mbps Eye Pattern



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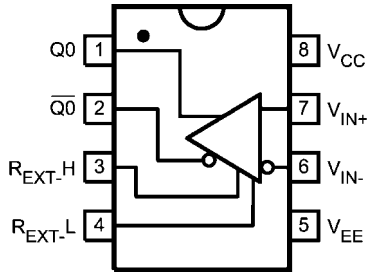
Connection Diagram (8-Pin SOIC)



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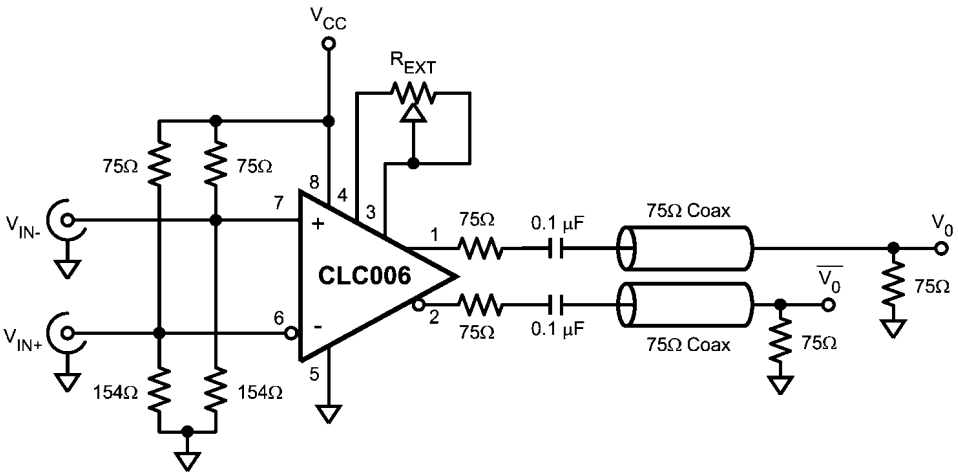
Order Number CLC006BM
See NS Package Number M08A

Typical Application



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	6V
Output Current	30 mA
Maximum Junction Temperature	+125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10 Seconds)	+300°C
ESD Rating (Human Body Model)	1000V
Package Thermal Resistance	
θ_{JA} 8–pin SOIC	+160°C/W
θ_{JC} 8–pin SOIC	+105°C/W
Reliability Information MTTF	254 Mhr

Recommended Operating Conditions

Supply Voltage Range (V_{CC} – V_{EE})	+4.5V to +5.5V

Electrical Characteristics

(V_{CC} = 0V, V_{EE} = −5V; unless otherwise specified).

Parameter	Condition	Typ +25°C	Min/Max +25°C	Min/Max 0°C to +70°C	Min/Max −40°C to +85°C	Units
STATIC DC PERFORMANCE						
Supply Current, Loaded	150Ω @ 270 Mbps (Note 5)	37	—	—	—	mA
Supply Current, Unloaded	(Note 3)	34	28/45	26/47	26/47	mA
Output HIGH Voltage (V_{OH})	(Note 3)	−1.7	−2.0/1.4	−2.0/1.4	−2.0/1.4	V
Output LOW Voltage (V_{OL})	(Note 3)	−3.3	−3.6/3.0	−3.6/3.0	−3.6/3.0	V
Input Bias Current		10	30	50	50	µA
Output Swing	R_{EXT} = ∞(Note 3)	1.65	1.55/1.75	1.53/1.77	1.51/1.79	V
Output Swing	R_{EXT} = 10 kΩ	1.30	—	—	—	V
Common Mode Input Range Upper Limit		−0.7	−0.8	−0.8	−0.8	V
Common Mode Input Range Lower Limit		−2.6	−2.5	−2.5	−2.5	V
Minimum Differential Input Swing		200	200	200	200	mV
Power Supply Rejection Ratio (Note 3)		26	20	20	20	dB
AC PERFORMANCE						
Output Rise and Fall Time	(Notes 3, 4, 5)	650	425/825	400/850	400/850	ps
Overshoot		5				%
Propagation Delay		1.0				ns
Duty Cycle Distortion		50				ps
Residual Jitter		25	—	—	—	ps_{pp}
MISCELLANEOUS PERFORMANCE						
Input Capacitance		1.0				pF
Output Resistance		10				Ω
Output Inductance		6				nH

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Note 3: Spec is 100% tested at +25°C

Note 4: Measured between the 20% and 80% levels of the waveform.

Note 5: Measured with both outputs driving 150Ω, AC coupled at 270 Mbps.

Operation

INPUT INTERFACING

The CLC006 has high impedance, emitter-follower buffered, differential inputs. Single-ended signals may also be input. Transmission lines supplying input signals must be properly terminated close to the CLC006. Either A.C. or D.C. coupling as in *Figure 2* or *Figure 3* may be used. *Figures 2, 4* and *Figure 5* show how Thevenin-equivalent resistor networks are used to provide input termination and biasing. The input D.C. common-mode voltage range is 0.8V to 2.5V below the positive power supply (V_{CC}). Input signals plus bias should be kept within the specified common-mode range. For an 800 mV_{P-P} input signal, typical input bias levels range from 1.2V to 2.1V below the positive supply.

Load Type	Resistor to V_{CC} (R1)	Resistor to V_{EE} (R2)
ECL, 50Ω, 5V, V_T=2V	82.5Ω	124Ω
ECL, 50Ω, 5.2V, V_T=2V	80.6Ω	133Ω
ECL, 75Ω, 5V, V_T=2V	124Ω	187Ω
ECL, 75Ω, 5.2V, V_T=2V	121Ω	196Ω
800 mV_{P-P}, 50Ω, 5V, V_T=1.6V	75.0Ω	154Ω
800 mV_{P-P}, 75Ω, 5V, V_T=1.6V	110Ω	232Ω
800 mV_{P-P}, 2.2KΩ, 5Ω, V_T=1.6V	3240Ω	6810Ω

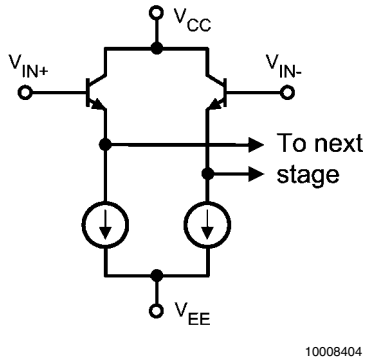


FIGURE 1. Input Stage

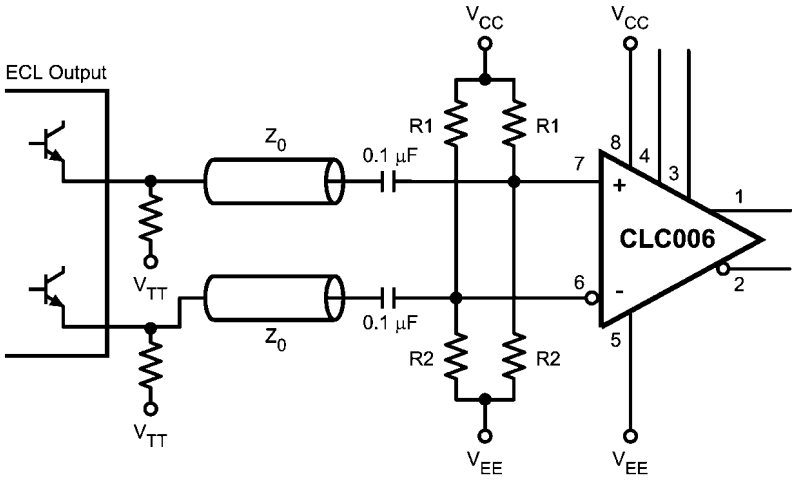


FIGURE 2. AC Coupled Input

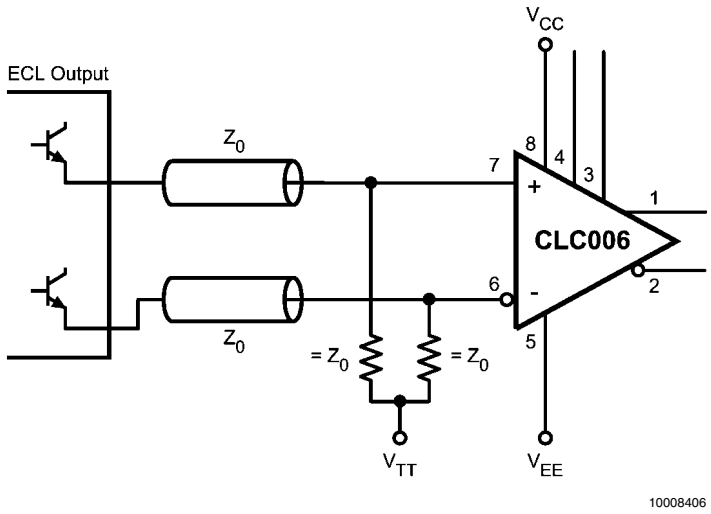


FIGURE 3. DC Coupled Input

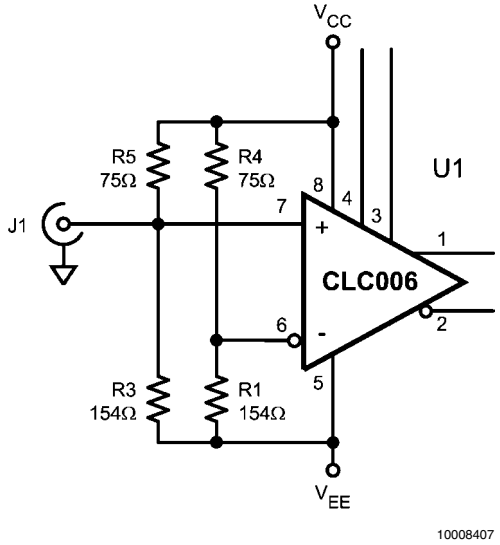


FIGURE 4. Single Ended 50Ω ECL input

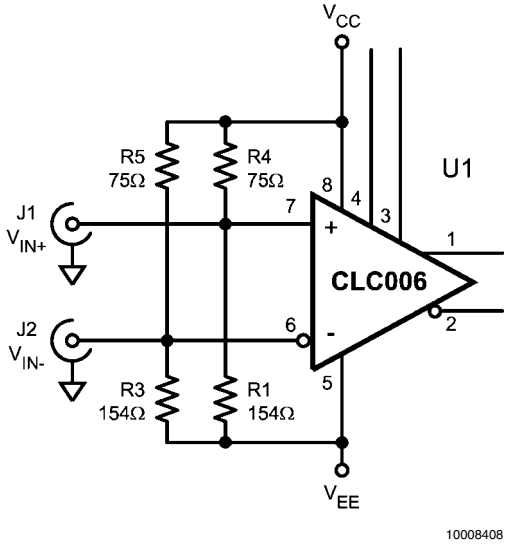


FIGURE 5. Differential 50Ω ECL Input

OUTPUT INTERFACING

The CLC006's class AB output stage, *Figure 6*, requires no standing current in the output transistors and therefore requires no biasing or pull-down resistors. Advantages of this arrangement are lower power dissipation and fewer external components. The output may be either D.C. or A.C. coupled to the load. A bandgap voltage reference sets output voltage levels which are compatible with F100K and 10K ECL when correctly terminated. The outputs do not have the same output voltage temperature coefficient as 10K. Therefore, noise margins will be reduced over the full temperature range when driving 10K ECL. Noise margins will not be affected when interfacing to F100K since F100K is fully voltage and temperature compensated.

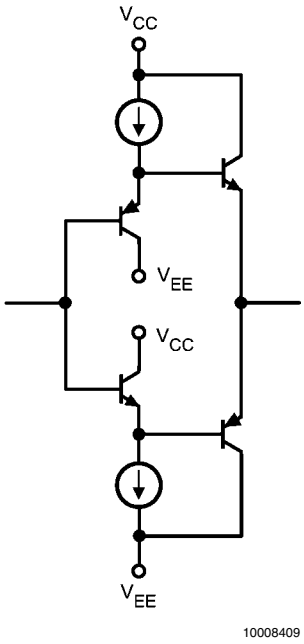


FIGURE 6. Output Stage

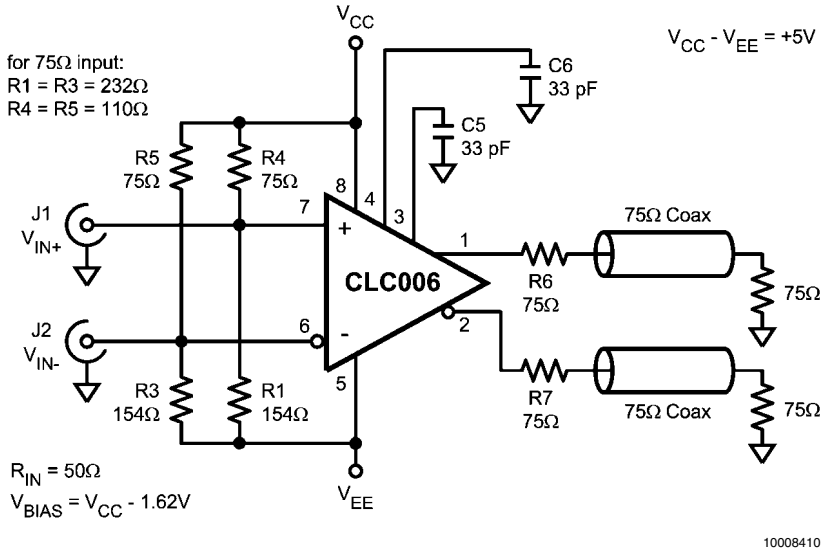


FIGURE 7. Differential Input DC Coupled Output

OUTPUT AMPLITUDE ADJUSTMENT

The high and low output levels of the CLC006 are set by a circuit shown simplified in *Figure 8*. Output high and low levels may be set independently with external resistor networks connected between R_{EXT-H} (pin 3), R_{EXT-L} (pin 4) and the power supplies. The resistor networks affect the high and low output levels by changing the internally generated bias voltages, V_H and V_L. The nominal high and low output levels are V_{CC}–1.7V and V_{CC}–3.3V, respectively, when the pins R_{EXT-H} and R_{EXT-L} are left unconnected. Though the internal components which determine output voltage levels have accurate ratios, their absolute values may be controlled only within about ±15% of nominal. Even so, without external adjustment, output voltages are well controlled. A final design should accommodate the variation in externally set output voltages due to the CLC006's part-to-part and external component tolerances.

Output voltage swing may be reduced with the circuit shown in *Figure 9*. A single resistance chosen with the aid of the graph, *Figure 10*, is connected between pins 3 and 4. Output voltage swing may be increased with the circuit of *Figure 11*. *Figure 12* is used to estimate a value for resistor R. Note that both of these circuits and the accompanying graphs assume that the CLC006 is loaded with the standard 150Ω. Be aware

that output loading will affect the output swing and the high and low levels. It may be necessary to empirically select resistances used to set output levels when the D.C. loading on the CLC006 differs appreciably from 150Ω.

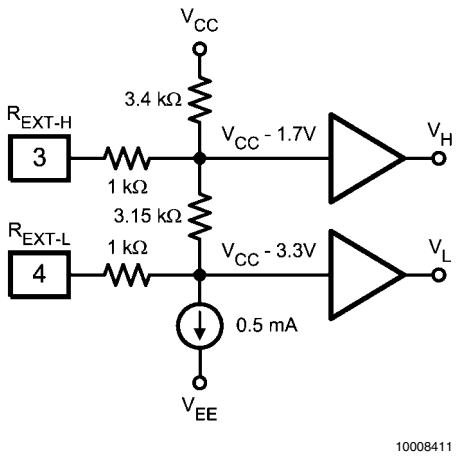


FIGURE 8. Equivalent Bias Generation Circuit

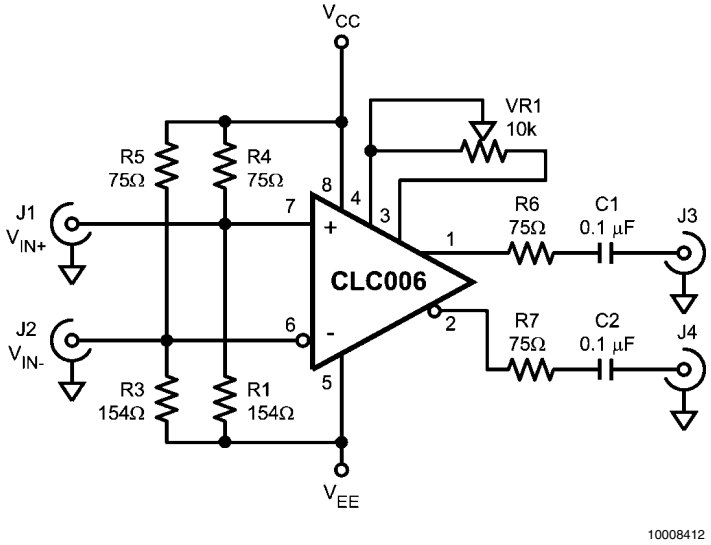


FIGURE 9. Differential Input Reduced Output

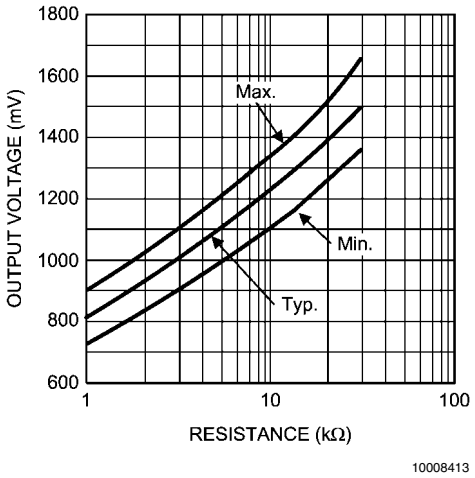


FIGURE 10. Resistance Pins 3 to 4 vs Output Voltage Reduced Output @ 150Ω Load

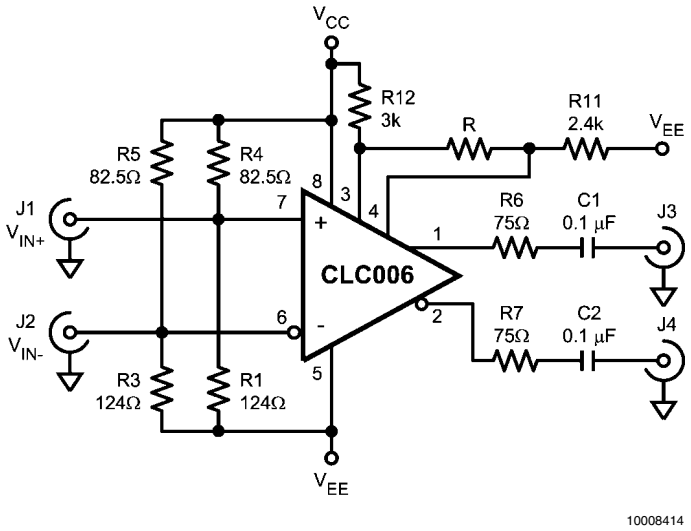


FIGURE 11. Differential Input Increased Output

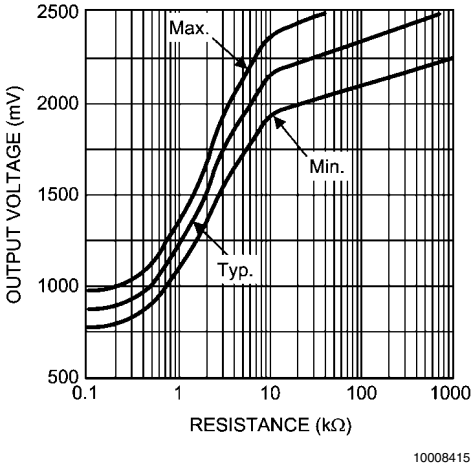


FIGURE 12. Resistance Pins 3 to 4 vs Output Voltage Increased Output @ 150Ω Load

OUTPUT RISE AND FALL TIMES

Output load capacitance can significantly affect output rise and fall times. The effect of load capacitance, stray or otherwise, may be reduced by placing the output back-match resistor close to the output pin and by minimizing all interconnecting trace lengths. *Figure 13* shows the effect on risetime of parallel load capacitance across a 150Ω load.

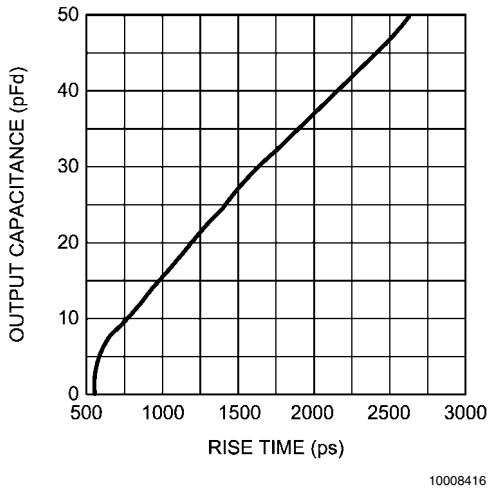


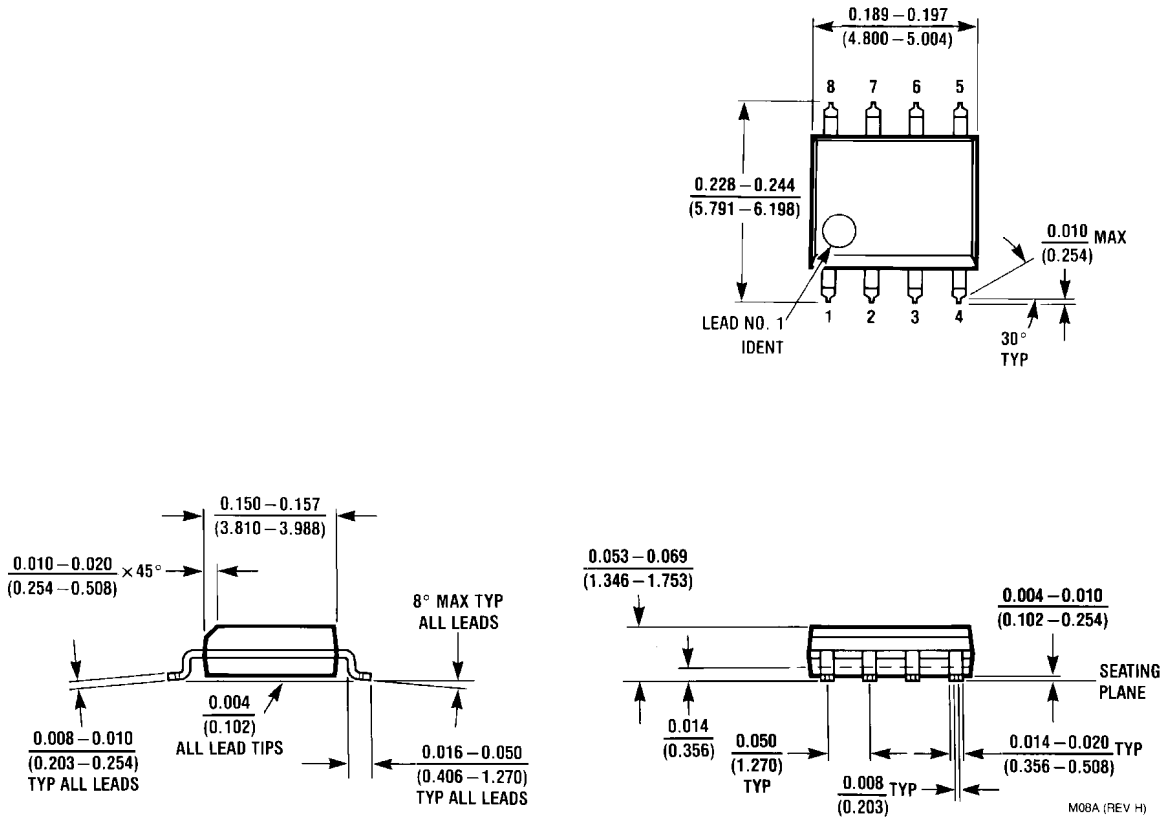
FIGURE 13. Rise Time vs C_L

PCB Layout Recommendations

Printed circuit board layout affects the performance of the CLC006. The following guidelines will aid in achieving satisfactory device performance.

- Use a ground plane or power/ground plane sandwich design for optimum performance.
- Bypass device power with a 0.01 µF monolithic ceramic capacitor in parallel with a 6.8 µF tantalum electrolytic capacitor located no more than 0.1" (2.5 mm) from the device power pins.
- Provide short, symmetrical ground return paths for:
  - inputs,
  - supply bypass capacitors and
  - the output load.
- Provide short, grounded guard traces located
  - under the centerline of the package,
  - 0.1" (2.5 mm) from the package pins
  - on both top and bottom of the board with connecting vias.

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number CLC006BM
NS Package Number M08A

Notes

Notes

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