

DS91D176/DS91C176

100 MHz Single Channel M-LVDS Transceivers

General Description

The DS91C176 and DS91D176 are 100 MHz single channel M-LVDS (Multipoint Low Voltage Differential Signaling) transceivers designed for applications that utilize multipoint networks (e.g. clock distribution in ATCA and uTCA based systems). M-LVDS is a new bus interface standard (TIA/EIA-899) optimized for multidrop networks. Controlled edge rates, tight input receiver thresholds and increased drive strength are some of the key enhancements that make M-LVDS devices an ideal choice for distributing signals via multipoint networks.

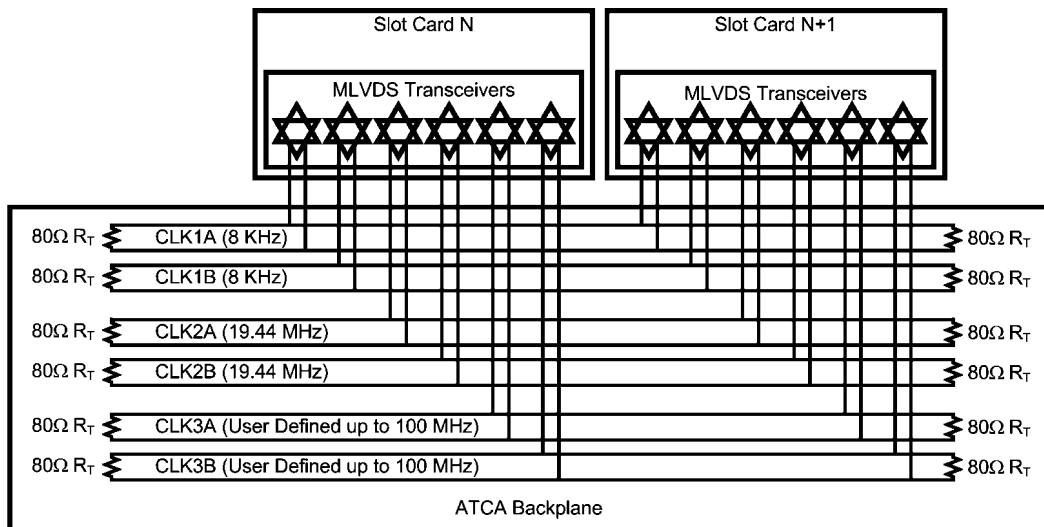
The DS91C176/DS91D176 are half-duplex transceivers that accept LVTTTL/LVCMOS signals at the driver inputs and convert them to differential M-LVDS signals. The receiver inputs accept low voltage differential signals (LVDS, B-LVDS, M-LVDS, LV-PECL and CML) and convert them to 3V LVCMOS

signals. The DS91D176 has a M-LVDS type 1 receiver input with no offset. The DS91C176 has an M-LVDS type 2 receiver which enable failsafe functionality.

Features

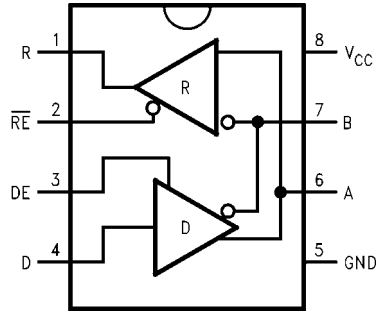
- DC to 100+ MHz / 200+ Mbps low power, low EMI operation
- Optimal for ATCA, uTCA clock distribution networks
- Meets or exceeds TIA/EIA-899 M-LVDS Standard
- Wide Input Common Mode Voltage for Increased Noise Immunity
- DS91D176 has type 1 receiver input
- DS91C176 has type 2 receiver with fail-safe
- Industrial temperature range
- Space saving SOIC-8 package

Typical Application in an ATCA Clock Distribution Network



20024630

Connection and Logic Diagram



20024601

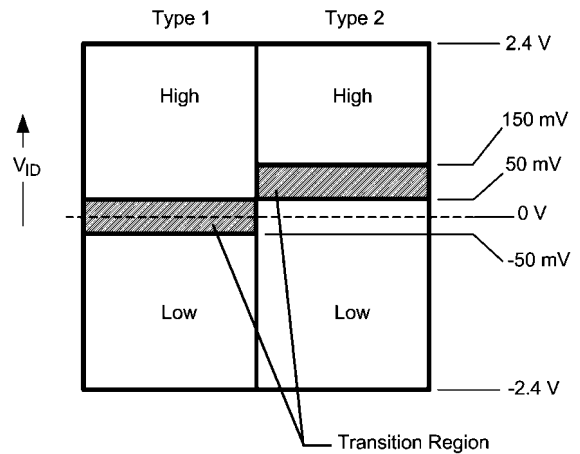
Top View
Order Number DS91D176TMA, DS91C176TMA
See NS Package Number M08A

Ordering Information

Order Number	Receiver Input	Function	Package Type
DS91D176TMA	type 1	Data (0V threshold receiver)	SOIC/M08A
DS91C176TMA	type 2	Control (100 mV offset fail-safe receiver)	SOIC/M08A

M-LVDS Receiver Types

The EIA/TIA-899 M-LVDS standard specifies two different types of receiver input stages. A type 1 receiver has a conventional threshold that is centered at the midpoint of the input amplitude, $V_{ID}/2$. A type 2 receiver has a built in offset that is 100mV greater than $V_{ID}/2$. The type 2 receiver offset acts as a failsafe circuit where open or short circuits at the input will always result in the output stage being driven to a low logic state.



20024640

FIGURE 1. M-LVDS Receiver Input Thresholds

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	-0.3V to +4V
Control Input Voltages	-0.3V to ($V_{CC} + 0.3V$)
Driver Input Voltage	-0.3V to ($V_{CC} + 0.3V$)
Driver Output Voltages	-1.8V to +4.1V
Receiver Input Voltages	-1.8V to +4.1V
Receiver Output Voltage	-0.3V to ($V_{CC} + 0.3V$)
Maximum Package Power Dissipation at +25°C	
SOIC Package	833 mW
Derate SOIC Package	6.67 mW/°C above +25°C
Thermal Resistance (4-Layer, 2 oz. Cu, JEDEC)	
θ_{JA}	150°C/W
θ_{JC}	63°C/W
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to +150°C

Lead Temperature (Soldering, 4 seconds)	260°C
ESD Ratings: (HBM 1.5k Ω , 100pF) (EIAJ 0 Ω , 200pF) (CDM 0 Ω , 0pF)	≥ 8 kV ≥ 250 V ≥ 1000 V

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage, V_{CC}	3.0	3.3	3.6	V
Voltage at Any Bus Terminal (Separate or Common-Mode)	-1.4		+3.8	V
Differential Input Voltage V_{ID}			2.4	V
LVTTL Input Voltage High V_{IH}	2.0		V_{CC}	V
LVTTL Input Voltage Low V_{IL}	0		0.8	V
Operating Free Air Temperature T_A	-40	+25	+85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2, Note 3, Note 4, Note 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
M-LVDS Driver							
$ V_{AB} $	Differential output voltage magnitude	$R_L = 50\Omega$, $C_L = 5pF$	480		650	mV	
ΔV_{AB}	Change in differential output voltage magnitude between logic states	Figure 2 and Figure 4	-50	0	+50	mV	
$V_{OS(SS)}$	Steady-state common-mode output voltage	$R_L = 50\Omega$, $C_L = 5pF$	0.3	1.8	2.1	V	
$ \Delta V_{OS(SS)} $	Change in steady-state common-mode output voltage between logic states	Figure 2 and Figure 3	0		+50	mV	
$V_{OS(PP)}$	Peak-to-peak common-mode output voltage	($V_{OS(PP)}$ @ 500KHz clock)		135		mV	
$V_{A(OC)}$	Maximum steady-state open-circuit output voltage	Figure 5	0		2.4	V	
$V_{B(OC)}$	Maximum steady-state open-circuit output voltage		0		2.4	V	
$V_{P(H)}$	Voltage overshoot, low-to-high level output	$R_L = 50\Omega$, $C_L = 5pF$, $C_D = 0.5pF$			$1.2V_{SS}$	V	
$V_{P(L)}$	Voltage overshoot, high-to-low level output	Figure 7 and Figure 8 (Note 9)	-0.2 V_S			V	
I_{IH}	High-level input current (LVTTL inputs)	$V_{IH} = 2.0V$	-15		15	μA	
I_{IL}	Low-level input current (LVTTL inputs)	$V_{IL} = 0.8V$	-15		15	μA	
V_{IKL}	Input Clamp Voltage (LVTTL inputs)	$I_{IN} = -18mA$	-1.5			V	
I_{OS}	Differential short-circuit output current	Figure 6	-43		43	mA	
M-LVDS Receiver							
V_{IT+}	Positive-going differential input voltage threshold	See Function Tables	Type 1		20	50	mV
			Type 2		94	150	mV
V_{IT-}	Negative-going differential input voltage threshold	See Function Tables	Type 1	-50	20		mV
			Type 2	50	94		mV
V_{OH}	High-level output voltage (LVTTL output)	$I_{OH} = -8mA$	2.4	2.7		V	
V_{OL}	Low-level output voltage (LVTTL output)	$I_{OL} = 8mA$		0.28	0.4	V	
I_{OZ}	TRI-STATE output current	$V_O = 0V$ or $3.6V$	-10		10	μA	
I_{OSR}	Short-circuit receiver output current (LVTTL output)	$V_O = 0V$		-48	-90	mA	
M-LVDS Bus (Input and Output) Pins							
I_A	Transceiver input/output current	$V_A = 3.8V$, $V_B = 1.2V$			32	μA	
		$V_A = 0V$ or $2.4V$, $V_B = 1.2V$	-20		+20	μA	
		$V_A = -1.4V$, $V_B = 1.2V$	-32			μA	

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_B	Transceiver input/output current	$V_B = 3.8V, V_A = 1.2V$			32	μA
		$V_B = 0V \text{ or } 2.4V, V_A = 1.2V$	-20		+20	μA
		$V_B = -1.4V, V_A = 1.2V$	-32			μA
I_{AB}	Transceiver input/output differential current ($I_A - I_B$)	$V_A = V_B, -1.4V \leq V \leq 3.8V$	-4		+4	μA
$I_{A(OFF)}$	Transceiver input/output power-off current	$V_A = 3.8V, V_B = 1.2V,$ $DE = V_{CC}$ $0V \leq V_{CC} \leq 1.5V$			32	μA
		$V_A = 0V \text{ or } 2.4V, V_B = 1.2V,$ $DE = V_{CC}$ $0V \leq V_{CC} \leq 1.5V$	-20		+20	μA
		$V_A = -1.4V, V_B = 1.2V,$ $DE = V_{CC}$ $0V \leq V_{CC} \leq 1.5V$	-32			μA
$I_{B(OFF)}$	Transceiver input/output power-off current	$V_B = 3.8V, V_A = 1.2V,$ $DE = V_{CC}$ $0V \leq V_{CC} \leq 1.5V$			32	μA
		$V_B = 0V \text{ or } 2.4V, V_A = 1.2V,$ $DE = V_{CC}$ $0V \leq V_{CC} \leq 1.5V$	-20		+20	μA
		$V_B = -1.4V, V_A = 1.2V,$ $DE = V_{CC}$ $0V \leq V_{CC} \leq 1.5V$	-32			μA
$I_{AB(OFF)}$	Transceiver input/output power-off differential current ($I_{A(OFF)} - I_{B(OFF)}$)	$V_A = V_B, -1.4V \leq V \leq 3.8V,$ $DE = V_{CC}$ $0V \leq V_{CC} \leq 1.5V$	-4		+4	μA
C_A	Transceiver input/output capacitance	$V_{CC} = \text{OPEN}$		9		pF
C_B	Transceiver input/output capacitance			9		pF
C_{AB}	Transceiver input/output differential capacitance			5.7		pF
$C_{A/B}$	Transceiver input/output capacitance balance (C_A/C_B)			1.0		
SUPPLY CURRENT (V_{CC})						
I_{CCD}	Driver Supply Current	$R_L = 50\Omega, DE = V_{CC}, \overline{RE} = V_{CC}$		20	29.5	mA
I_{CCZ}	TRI-STATE Supply Current	$DE = \text{GND}, \overline{RE} = V_{CC}$		6	9.0	mA
I_{CCR}	Receiver Supply Current	$DE = \text{GND}, \overline{RE} = \text{GND}$		14	18.5	mA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 3, Note 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AC SPECIFICATION						
t_{PLH}	Differential Propagation Delay Low to High	$R_L = 50\Omega, C_L = 5\text{ pF},$ $C_D = 0.5\text{ pF}$ Figure 7 and Figure 8	1.3	3.4	5.0	ns
t_{PHL}	Differential Propagation Delay High to Low		1.3	3.1	5.0	ns
$t_{SKD1} (t_{sk(p)})$	Pulse Skew $ t_{PLHD} - t_{PHLD} $ (Note 5, Note 9)			300	420	ps
t_{SKD3}	Part-to-Part Skew (Note 6, Note 9)				1.3	ns
$t_{TLH} (t_r)$	Rise Time (Note 9)		1.0	1.8	3.0	ns
$t_{THL} (t_f)$	Fall Time (Note 9)		1.0	1.8	3.0	ns
t_{PZH}	Enable Time (Z to Active High)	$R_L = 50\Omega, C_L = 5\text{ pF},$ $C_D = 0.5\text{ pF}$ Figure 9 and Figure 10			8	ns
t_{PZL}	Enable Time (Z to Active Low)				8	ns
t_{PLZ}	Disable Time (Active Low to Z)				8	ns
t_{PHZ}	Disable Time (Active High to Z)				8	ns
t_{JIT}	Random Jitter, RJ (Note 9)	100 MHz Clock Pattern (Note 7)		2.5	5.5	psrms
f_{MAX}	Maximum Data Rate		200			Mbps
RECEIVER AC SPECIFICATION						
t_{PLH}	Propagation Delay Low to High	$C_L = 15\text{ pF}$ Figures 11, 12 and Figure 13	2.0	4.7	7.5	ns
t_{PHL}	Propagation Delay High to Low		2.0	5.3	7.5	ns
$t_{SKD1} (t_{sk(p)})$	Pulse Skew $ t_{PLHD} - t_{PHLD} $ (Note 5, Note 9)			0.6	1.7	ns
t_{SKD3}	Part-to-Part Skew (Note 6, Note 9)				1.3	ns
$t_{TLH} (t_r)$	Rise Time (Note 9)		0.5	1.2	2.5	ns
$t_{THL} (t_f)$	Fall Time (Note 9)		0.5	1.2	2.5	ns
t_{PZH}	Enable Time (Z to Active High)	$R_L = 500\Omega, C_L = 15\text{ pF}$ Figure 14 and Figure 15			10	ns
t_{PZL}	Enable Time (Z to Active Low)				10	ns
t_{PLZ}	Disable Time (Active Low to Z)				10	ns
t_{PHZ}	Disable Time (Active High to Z)				10	ns
f_{MAX}	Maximum Data Rate		200			Mbps

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for $V_{CC} = 3.3V$ and $T_A = 25^\circ C$.

Note 4: The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this datasheet.

Note 5: t_{SKD1} , $|t_{PLHD} - t_{PHLD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

Note 6: t_{SKD3} , Part-to-Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within $5^\circ C$ of each other within the operating temperature range.

Note 7: Stimulus and fixture Jitter has been subtracted.

Note 8: C_L includes fixture capacitance and C_D includes probe capacitance.

Note 9: Not production tested. Guaranteed by a statistical analysis on a sample basis at the time of characterization.

Test Circuits and Waveforms

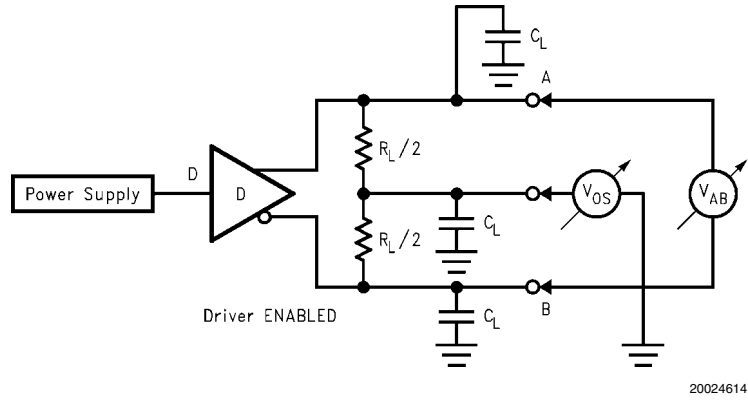


FIGURE 2. Differential Driver Test Circuit

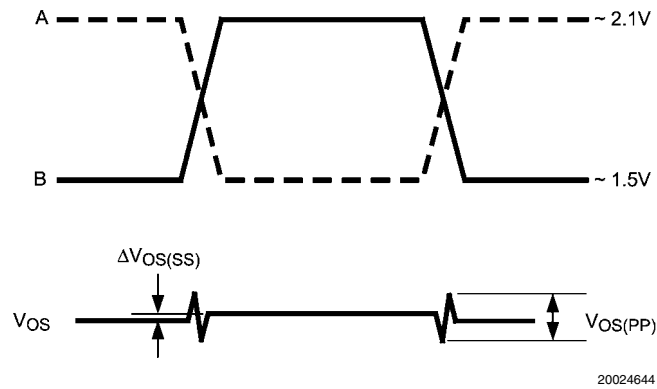


FIGURE 3. Differential Driver Waveforms

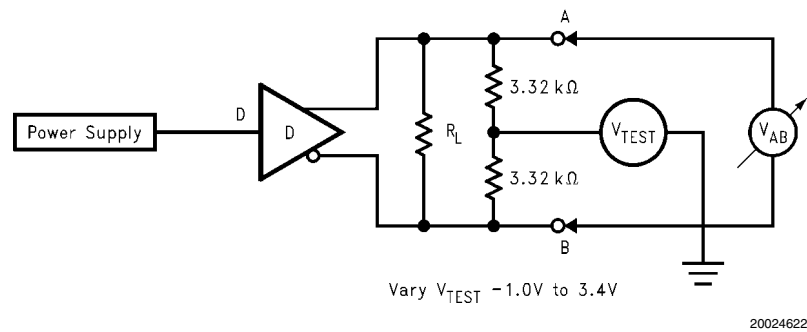
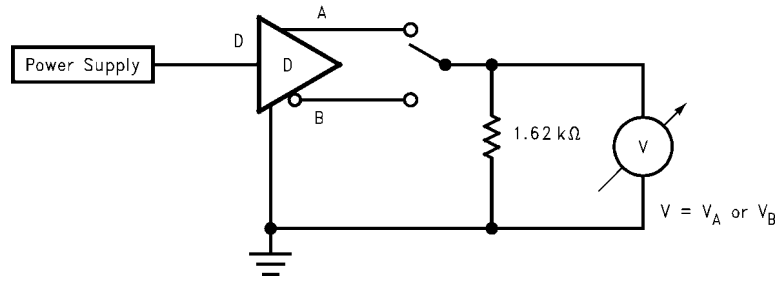
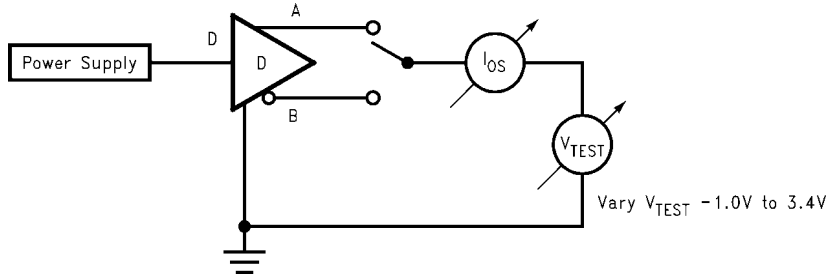


FIGURE 4. Differential Driver Full Load Test Circuit



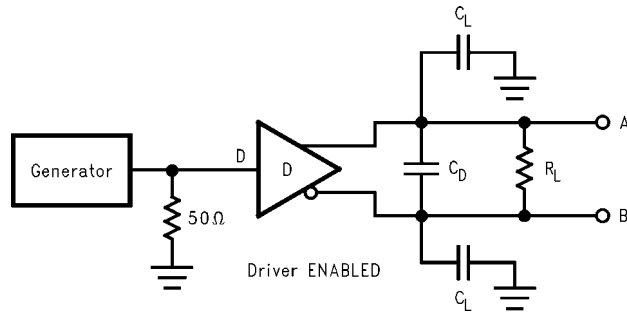
20024612

FIGURE 5. Differential Driver DC Open Test Circuit



20024625

FIGURE 6. Differential Driver Short-Circuit Test Circuit



20024616

FIGURE 7. Driver Propagation Delay and Transition Time Test Circuit

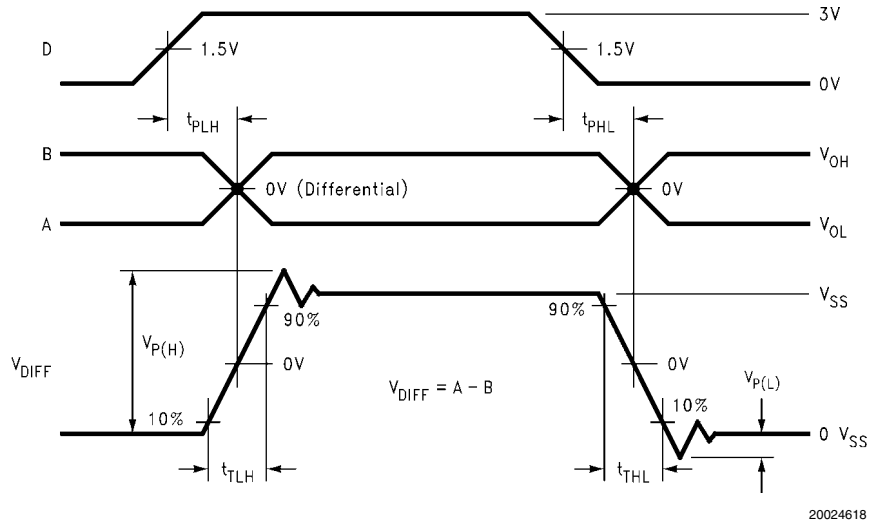


FIGURE 8. Driver Propagation Delays and Transition Time Waveforms

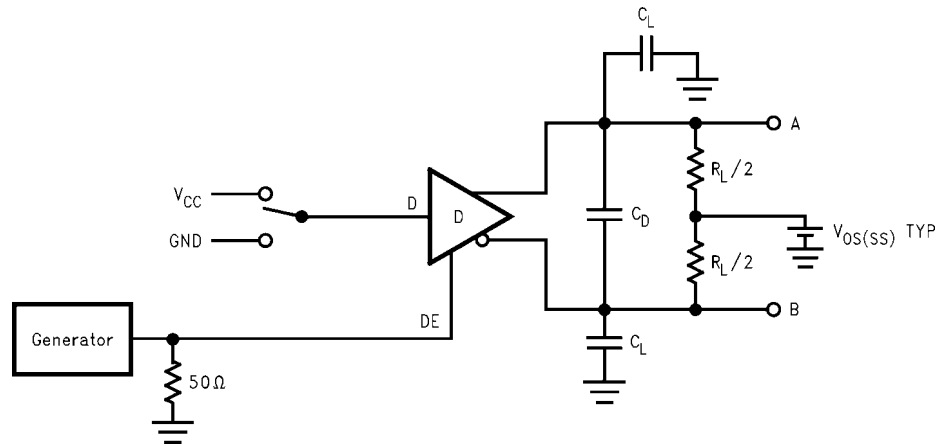


FIGURE 9. Driver TRI-STATE Delay Test Circuit

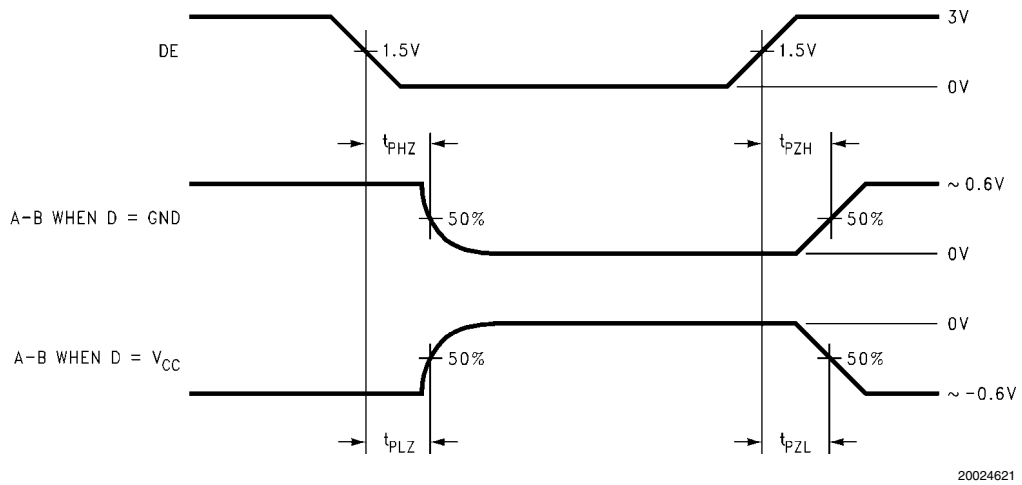
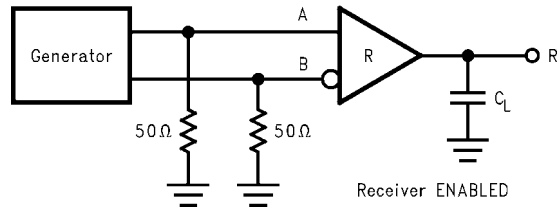
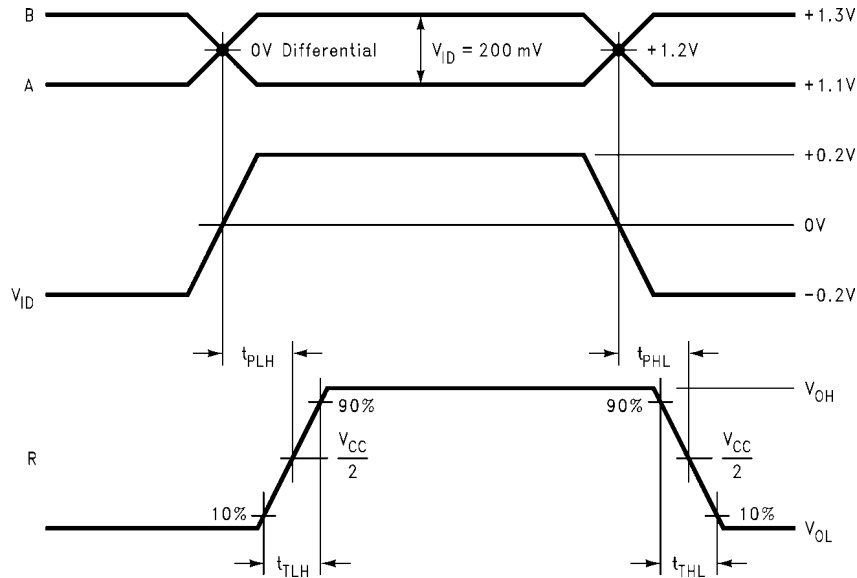


FIGURE 10. Driver TRI-STATE Delay Waveforms



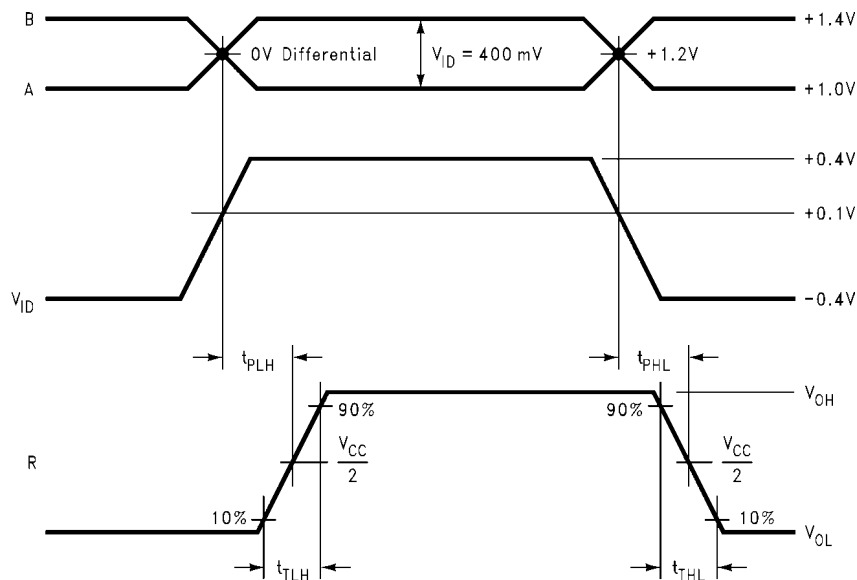
20024615

FIGURE 11. Receiver Propagation Delay and Transition Time Test Circuit



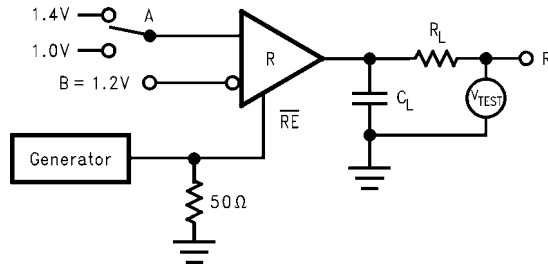
20024617

FIGURE 12. Type 1 Receiver Propagation Delay and Transition Time Waveforms



20024623

FIGURE 13. Type 2 Receiver Propagation Delay and Transition Time Waveforms



20024613

FIGURE 14. Receiver TRI-STATE Delay Test Circuit

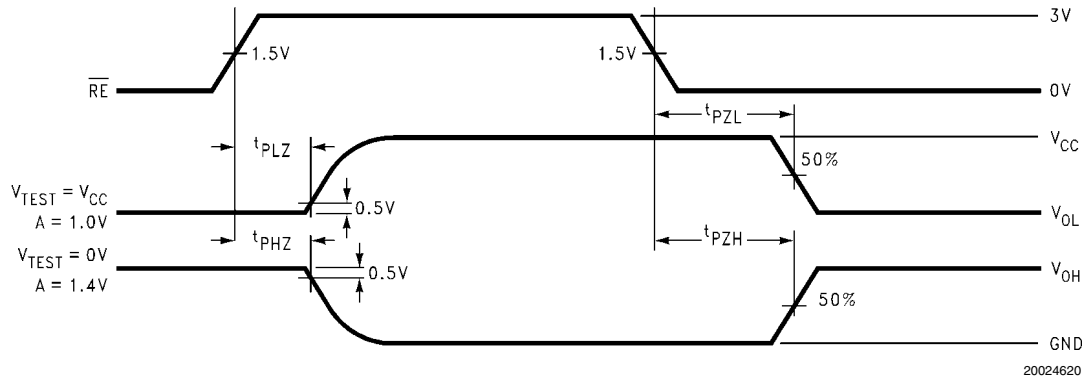


FIGURE 15. Receiver TRI-STATE Delay Waveforms

Function Tables

DS91D176/DS91C176 Transmitting

Inputs			Outputs	
\overline{RE}	DE	D	B	A
X	2.0V	2.0V	L	H
X	2.0V	0.8V	H	L
X	0.8V	X	Z	Z

X — Don't care condition
Z — High impedance state

DS91D176 Receiving

Inputs			Output
\overline{RE}	DE	A - B	R
0.8V	0.8V	$\geq +0.05V$	H
0.8V	0.8V	$\leq -0.05V$	L
0.8V	0.8V	0V	X
2.0V	0.8V	X	Z

X — Don't care condition
Z — High impedance state

DS91C176 Receiving

Inputs			Output
\overline{RE}	DE	A - B	R
0.8V	0.8V	$\geq +0.15V$	H
0.8V	0.8V	$\leq +0.05V$	L
0.8V	0.8V	0V	L
2.0V	0.8V	X	Z

X — Don't care condition
Z — High impedance state

DS91D176 Receiver Input Threshold Test Voltages

Applied Voltages		Resulting Differential Input Voltage	Resulting Common-Mode Input Voltage	Receiver Output
V_{IA}	V_{IB}	V_{ID}	V_{IC}	R
2.400V	0.000V	2.400V	1.200V	H
0.000V	2.400V	-2.400V	1.200V	L
3.800V	3.750V	0.050V	3.775V	H
3.750V	3.800V	-0.050V	3.775V	L
-1.400V	-1.350V	-0.050V	-1.375V	H
-1.350V	-1.400V	0.050V	-1.375V	L

H — High Level
L — Low Level
Output state assumes that the receiver is enabled ($\overline{RE} = L$)

DS91C176 Receiver Input Threshold Test Voltages

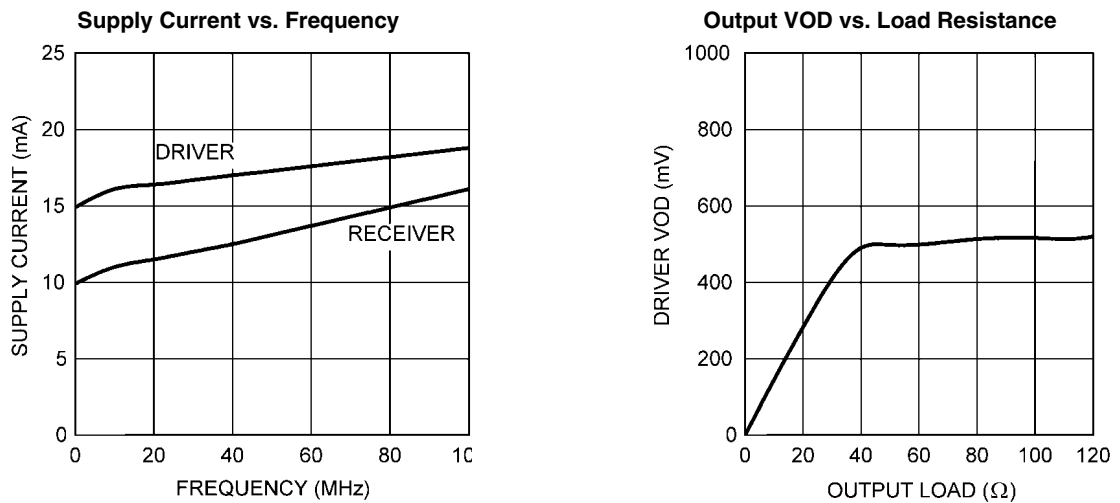
Applied Voltages		Resulting Differential Input Voltage	Resulting Common-Mode Input Voltage	Receiver Output
V_{IA}	V_{IB}	V_{ID}	V_{IC}	R
2.400V	0.000V	2.400V	1.200V	H
0.000V	2.400V	-2.400V	1.200V	L
3.800V	3.650V	0.150V	3.725V	H
3.800V	3.750V	0.050V	3.775V	L
-1.250V	-1.400V	0.150V	-1.325V	H
-1.350V	-1.400V	0.050V	-1.375V	L

H — High Level
L — Low Level
Output state assumes that the receiver is enabled ($\overline{RE} = L$)

Pin Descriptions

Pin No.	Name	Description
1	R	Receiver output pin
2	\overline{RE}	Receiver enable pin: When \overline{RE} is high, the receiver is disabled. When \overline{RE} is low or open, the receiver is enabled.
3	DE	Driver enable pin: When DE is low, the driver is disabled. When DE is high, the driver is enabled.
4	D	Driver input pin
5	GND	Ground pin
6	A	Non-inverting driver output pin/Non-inverting receiver input pin
7	B	Inverting driver output pin/Inverting receiver input pin
8	V_{CC}	Power supply pin, $+3.3V \pm 0.3V$

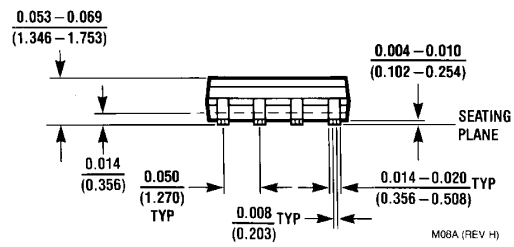
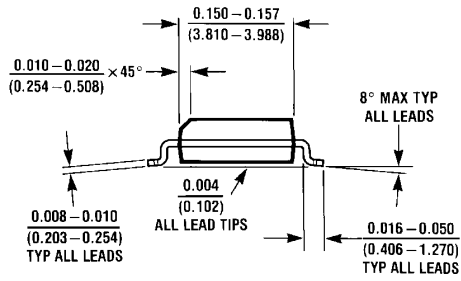
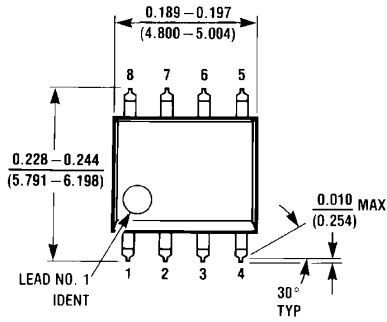
Typical Performance Characteristics



Supply Current measured using a clock pattern with driver terminated to 50ohms. $V_{CC} = 3.3V$, $T_A = +25^\circ C$
 $V_{CC} = 3.3V$, $T_A = +25^\circ C$.

FIGURE 16. DS91D176/DS91C176 Typical Performance Characteristics

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number DS91D176TMA, DS91C176TMA
See NS package Number M08A

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
Audio	www.national.com/audio	App Notes	www.national.com/appnotes
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/lido	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempensors	SolarMagic™	www.national.com/solarmagic
Wireless (PLL/VCO)	www.national.com/wireless	PowerWise® Design University	www.national.com/training

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2009 National Semiconductor Corporation

For the most current product information visit us at www.national.com



National Semiconductor Americas Technical Support Center
Email: support@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Technical Support Center
Email: europe.support@nsc.com

National Semiconductor Asia Pacific Technical Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Technical Support Center
Email: jpn.feedback@nsc.com