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Specification
 4 x 40 Daystar Nova LCD Module
 with
 Parallel Data Input Option and Fiber Optic Backlight
 Model 03875-21-0114

REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

REVISION STATUS


PROJ. NO. 411	CONTRACT		 INDUSTRIAL ELECTRONIC ENGINEERS, INC. VAN NUYS, CALIFORNIA		
	DRAWN R. January 3-19-93	PARALLEL DATA INPUT 4 X 40 LCD MODULE WITH FIBER OPTIC BACKLIGHT			
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1.0 GENERAL INFORMATION

1.1 Introduction

This specification describes the parallel interface Daystar Nova model 03875–21–0114, a 4–line supertwisted liquid crystal display (LCD) with 40 characters per line.

Model Number Designation System

<u>03875</u>	–	<u>21</u>	–	<u>0</u>		<u>1</u>		<u>1</u>		<u>4</u>
Transflective STN LCD w/EL Backlight		4x40 Format		Reserved		1 = Parallel Data Input * 2 = Serial Data Input		1 = +5 V _{DC} Backlight Power		5 = White Color

* Parallel standard, Serial optional

1.2 Application

Daystar Nova modules provide alphanumeric information which is easily readable in high ambient light or in darkness with Fiber Optic (FO) backlight activated. The low power requirements of the modules make them suitable for portable battery operated equipment. The wide operating temperature range (–30° to +80°C) is ideal for most outdoor applications. The choice of a preferential viewing hemisphere is not necessary because of the excellent wide angle viewing characteristics of the new Super Bi–refracting Effect (SBE) liquid crystal cell used in this display.

For applications where the display is remotely located up to 50 feet from the host processor, the serial data input option should be used. The serial model is described in IEE specification S3875–21–0214.

1.3 Description

The Daystar Nova module is a self–contained 1/16 multiplexed unit. A simple parallel interface is provided and can be configured as either 4 or 8 bits. The on–board microprocessor controls the display, multiplexing and character decoding. The temperature compensation circuitry guarantees that the viewing characteristics are optimized for all temperatures.

The SBE liquid crystal cell used in this display has a golden–green background with dark blue–black characters.

The on–board character generator ROM generates 192 types of alphanumeric, numeric, katakana characters and symbols. In addition, a character generator RAM allows the user to define eight additional characters.

A variety of high level functions allow the programmer to operate the display with simple and straightforward software routines. One such feature automatically increments the character display position after each character is written.

A single +5 Volt nominal power supply is required for operation of the LCD module. The unit operates from 4.50 Volts to 5.50 Volts. The typical power requirement for the module is 75mW.

The module weighs 8.9 oz. (252 grams).

2.0 LOGICAL STRUCTURE AND FUNCTION

2.1 LCD Module

Figure 1 illustrates the major components of the serial option Daystar Nova module. The module provides means for an external viewing angle adjustment potentiometer (V_{BIAS} Adj.) at Pin 4, and connections for optional RESET and self–test switches at Pins 3 and 5. The external viewing angle adjustment potentiometer should be connected to the same +5 Volt supply as the display module. RESET and TEST pull down to ground to activate the function. All three inputs may be left open if not used. The V_{BIAS} test point is used at the factory to preset the viewing angle. The LCD Controllers are microprocessor units (MPU) designed specifically to control all multiplexing and character decoding functions for the LCD display.

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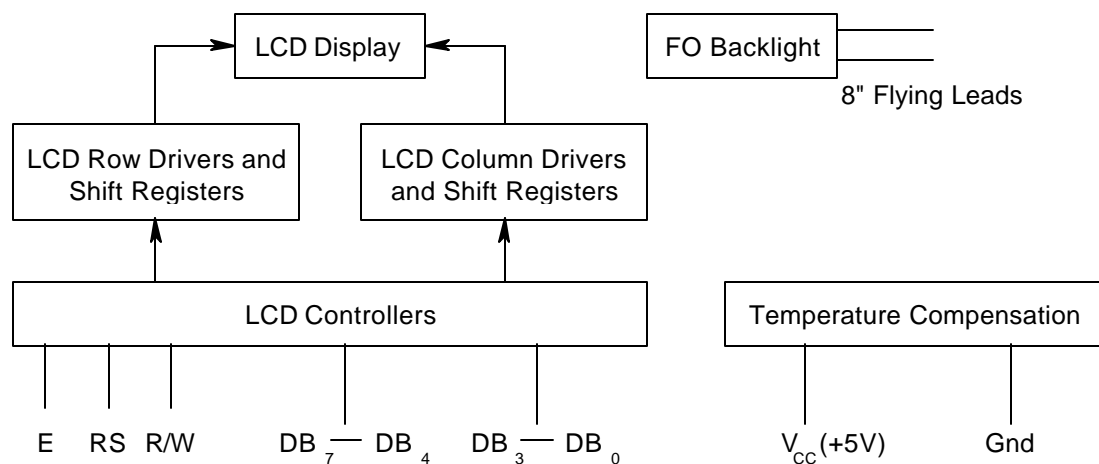


Figure 1 Module Block Diagram

2.1.1 Signal Description

Signal Name	Number Of Lines	Input/Output	Connected
RS	1	I	MPU1/MPU2
R/W	1	I	MPU1/MPU2
E	1	I	MPU1
E	1	I	MPU2
DB ₄ -DB ₇	4	I/O	MPU1/MPU2
DB ₀ -DB ₃	4	I/O	MPU1/MPU2
V _{CC}	2	-	Power
GND	7	-	-

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2.2 LCD Controller

The LCD Controller includes all of the circuitry necessary to take parallel input data and create the necessary control functions and characters. The block diagram of the controller is shown in Figure 2 below. The remaining subparagraphs of Section 2 describe the major function blocks.

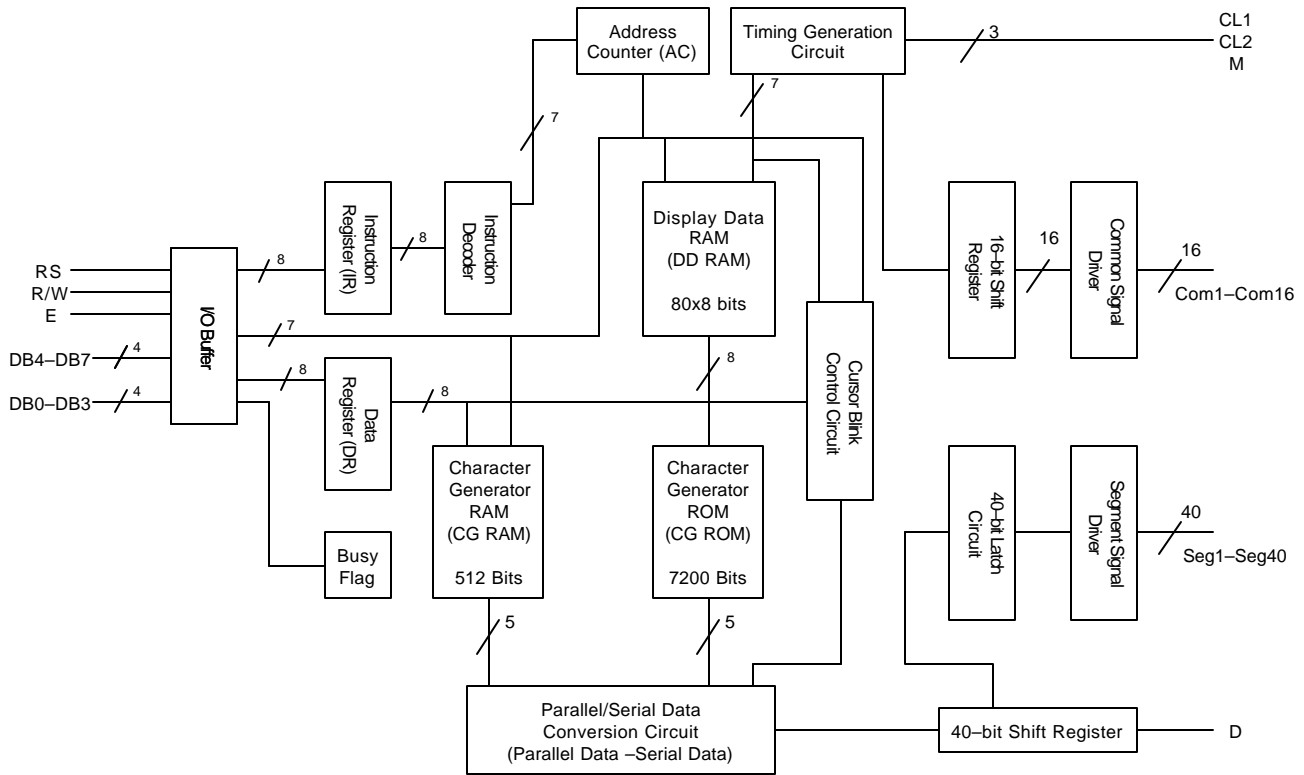


Figure 2 LCD Controller Block Diagram

2.2.1 Instruction Register (IR)

The IR stores instruction codes such as display clear and cursor shift, and address information of the display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written from the MPU, but not read.

2.2.2 Data Register (DR)

The DR temporarily stores data to be written into or read from the DD RAM or the CG RAM.

2.2.3 Busy Flag

When the Busy Flag is a "1", the module is in an internal operating mode and ignores any additional instructions (Refer to Read Busy Flag and Address instruction).

2.2.4 Address Counter (AC)

The AC determines the address of the DD RAM or CG RAM in which new data is stored. After writing into (or reading from) the DD RAM or CG RAM, the AC is incremented or decremented as defined by the Increment/Decrement bit (Refer to Entry Mode Set instruction).

2.2.5 Display Data RAM (DD RAM)

The DD RAM contains 80 X 8 bits and represents 80 characters. The relationship between the DD RAM address and position of the characters in the display can be controlled by the user (Refer to Entry Mode Set and

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Cursor or Display Shift instructions).

2.2.6 Character Generator ROM (CG ROM)

The CG ROM generates character patterns of 5 X 7 dots from 8 bit character codes. The 192 5 X 7 dot matrix characters are illustrated in Figure 3.

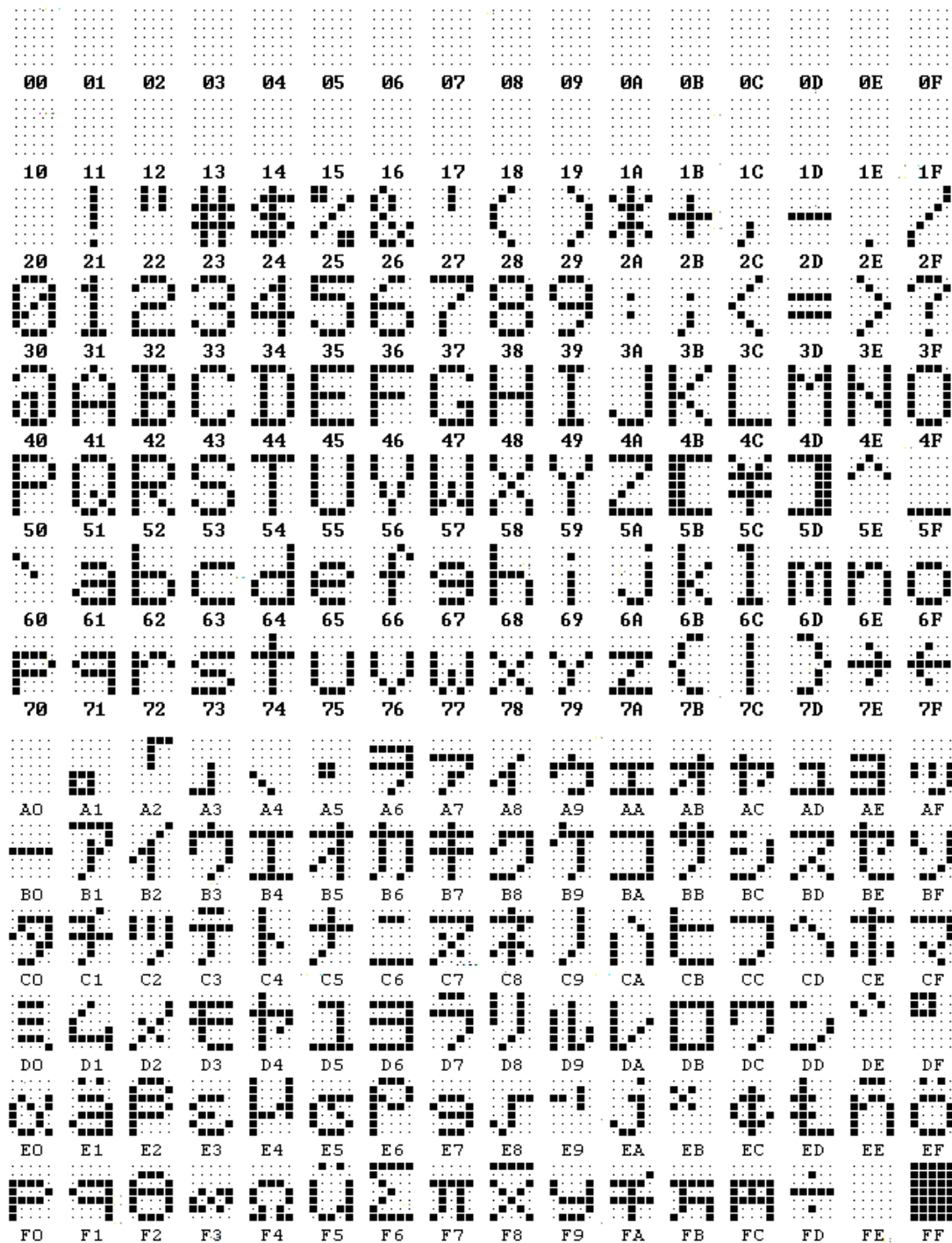


Figure 3 Correspondence Between Character Codes and Character Patterns

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Note: Addresses 00h through 0Fh are reserved for CG RAM Addressing. Addresses 10h through 1Fh and 80h through 9Fh are not used.

2.2.7 Character Generator RAM (CG RAM)

The CG RAM allows the user to define 8 types of 5 X 7 character patterns. Figure 4 shows the relationship between CG RAM addresses and data patterns (Refer to Set CG RAM Address and Write to CG or DD RAM instructions).

Character Codes (DD RAM Data)								CG RAM Address						Character Patterns (CG RAM Data)																																																																																															
7	6	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0																																																																																								
←Higher Order Bits				Lower Order Bits→				←Higher Order Bits				Lower Order Bits→				←Higher Order Bits				Lower Order Bits→																																																																																									
														<table border="0"> <tr> <td>*</td><td>*</td><td>*</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td> <td rowspan="8">Character Pattern Example ←Cursor</td> </tr> <tr> <td></td><td></td><td></td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td> </tr> <tr> <td></td><td></td><td></td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td> </tr> <tr> <td></td><td></td><td></td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td> </tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>*</td><td>0</td><td>0</td><td>0</td> <td>1</td><td>0</td><td>1</td><td>0</td><td>0</td> </tr> <tr> <td></td><td></td><td></td><td>1</td><td>0</td><td>1</td><td></td><td></td> <td>1</td><td>0</td><td>0</td><td>1</td><td>0</td> </tr> <tr> <td></td><td></td><td></td><td>1</td><td>1</td><td>0</td><td></td><td></td> <td>1</td><td>0</td><td>0</td><td>0</td><td>1</td> </tr> <tr> <td></td><td></td><td></td><td>1</td><td>1</td><td>1</td><td></td><td></td> <td>*</td><td>*</td><td>*</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> </table>								*	*	*	1	1	1	1	0	Character Pattern Example ←Cursor				1	0	0	0	1				1	0	0	0	1				1	1	1	1	0	0	0	0	0	*	0	0	0	1	0	1	0	0				1	0	1			1	0	0	1	0				1	1	0			1	0	0	0	1				1	1	1			*	*	*	0	0	0	0	0
*	*	*	1	1	1	1	0	Character Pattern Example ←Cursor																																																																																																					
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			1	1	1				*	*	*	0	0	0	0	0																																																																																													

Figure 4 Relationship Between CG RAM Address, Character Codes (DD RAM) and Character Patterns (CG RAM Data)

NOTES:

- 1) The CG RAM consists of 64 bytes. Any bytes not used for character pattern information can be used for general purpose data RAM. The 5, 6 and 7 bits are never used for character pattern information and are always available for use.
- 2) The 0, 1 and 2 bits of character code correspond to the 3, 4 and 5 bits of the CG RAM address.
- 3) The 0, 1 and 2 bits of the CG RAM address specify the row of the character pattern.
- 4) The 8th row of the character pattern corresponds to the cursor character pattern. If any bit in the row is "1", then the corresponding cursor bit is a "1" regardless of cursor position. (For most applications, the data should be "0" in this row, which allows for normal cursor operation on the character.)
- 5) Since bit 3 is a "don't care", two character codes represent the same special character. For example, a character code of 07 (hexadecimal) selects the same character pattern as 0F (hexadecimal).

2.2.8 Parallel/Serial Data Conversion Circuitry, Timing Generator Circuitry

These blocks control the interface to the LCD drivers.

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3.0 OPERATION

3.1 Instruction Set

Instruction	Code										Description	Execution Time (Max)
	RS	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM to 0	1.64 ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAN counter to 0. If the display has been shifted, characters are returned to their initial positions. DD RAM contents remain unchanged.	1.64 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets shift register direction and cursor movement direction which occur during data read and write operations	40µs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Turns ON/OFF the entire display (D), cursor) and cursor blink attribute (B).	40µs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor or shifts entire display one position. DD RAM contents are unchanged.	40µs
Function Set	0	0	0	0	1	DL	1	0	*	*	Sets Interface Data Length.	40µs
Set CG RAM Address	0	0	0	1							Sets CG RAM address. CG RAM data is sent or received after this is set.	40µs
Set DD RAM Address	0	0	1								Sets DD RAM address. DD RAM data is sent or received after this is set.	40µs
Read Busy Flag and Address	0	1	BF								Reads Busy Flag (BF) and Address Counter	0µs
Write Data to CG or DD RAM	1	0									Writes data into CG RAM or DD RAM.	40µs
Read Data from CG or DD RAM	1	1									Reads data from CG RAM or DD RAM.	40µs

I/D=1:	Increment	DD RAM:	Display Data RAM
I/D=0:	Decrement	CG RAM:	Character Generator RAM
S=1:	Enable Shift Operation	A _{CG}	CG RAM Address
S/C=1:	Shift Display	A _{DD}	DD RAM Address
S/C=0:	Shift Cursor		(Corresponds to cursor address)
R/L=1:	Shift Right	AC	Address Counter
R/L=0:	Shift Left		(used for both CG and DD RAM)
DL=1:	8-bit operation	*	Don't Care
DL=0:	4-bit operation		
BF=1:	Operating internally		
BF=0:	Can accept instruction		

Figure 5 LCD Controller Instruction Set

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3.2 Power Up Instructions Sequence

Upon power up, the Daystar Nova module is set to a default mode of operation. Under some power up circumstances, the default mode may be improperly set. Consequently, the following instructions should always be executed in the host systems initialization routine.

Step	Operation
1	Function Set for 8 bits
2	Repeat, Function Set for 8 bits
3	Function Set
4	Clear Display
5	Entry Mode Set
6	Display On/Off Control

STEP	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	0	1	1	*	*	*	*
2	0	0	0	0	1	1	*	*	*	*
3	0	0	0	0	1	DL	1	0	*	*
4	0	0	0	0	0	0	0	0	0	1
5	0	0	0	0	0	0	0	1	I/D	S
6	0	0	0	0	0	0	1	D	C	B

Refer to instruction set for values of DL, I/D, S, D, C and B. (* Don't care)

3.3 Instructions Affecting the Relationship of Display Position, Cursor, and DD RAM Address

The DD RAM contains the 8 bit character codes of the 40 characters displayed on the Daystar Nova LCD. The Cursor or Display Shift instruction and the Write to DD RAM and Entry Mode instructions affect the relationship between DD RAM address and display position. Figures 6 to 10 illustrate the effects of these instructions.

	00*	01	02	03	04	05	06	07	08	09	0A		22	23	24	25	26	27
MPU1	40	41	42	43	44	45	46	47	48	49	4A		62	63	64	65	66	67
	00*	01	02	03	04	05	06	07	08	09	0A		22	23	24	25	26	27
MPU2	40	41	42	43	44	45	46	47	48	49	4A		62	63	64	65	66	67

* = Cursor

Figure 6 Initial Conditions on Power Up

	01	02	03	04	05	06	07	08	09	0A	0B		23	24	25	26	27	00*
MPU1	41	42	43	44	45	46	47	48	49	4A	4B		63	64	65	66	67	40
	00*	01	02	03	04	05	06	07	08	09	0A		22	23	24	25	26	27
MPU2	40	41	42	43	44	45	46	47	48	49	4A		62	63	64	65	66	67

* = Cursor

Figure 7 Display Shift Left from Initial Conditions

	27	00*	01	02	03	04	05	06	07	08	09		21	22	23	24	25	26
--	----	-----	----	----	----	----	----	----	----	----	----	--	----	----	----	----	----	----

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MPU1	67	40	41	42	43	44	45	46	47	48	49		61	62	63	64	65	66
	00*	01	02	03	04	05	06	07	08	09	0A		22	23	24	25	26	27
MPU2	40	41	42	43	44	45	46	47	48	49	4A		62	63	64	65	66	67

* = Cursor

Figure 8 Display Shift Right from Initial Conditions

	01*	02	03	04	05	06	07	08	09	0A	0B		23	24	25	26	27	00#
MPU1	41	42	43	44	45	46	47	48	49	4A	4B		63	64	65	66	67	40
	00*	01	02	03	04	05	06	07	08	09	0A		22	23	24	25	26	27
MPU2	40	41	42	43	44	45	46	47	48	49	4A		62	63	64	65	66	67

* = Cursor

= Last Character Entered

Figure 9 Load Character with S=1, I/D=0 from Initial Conditions

	27*	00#	01	02	03	04	05	06	07	08	09		21	22	23	24	25	26
MPU1	67	40	41	42	43	44	45	46	47	48	49		61	62	63	64	65	66
	00*	01	02	03	04	05	06	07	08	09	0A		22	23	24	25	26	27
MPU2	40	41	42	43	44	45	46	47	48	49	4A		62	63	64	65	66	67

* = Cursor

= Last Character Entered

Figure 10 Load Character with S=1, I/D=1 from Initial Conditions

3.4 Instructions Affecting Custom Characters

The module allows the user to define 8 unique special characters. The pattern of the characters is stored in the CG RAM. The relationship between the CG RAM address and the character pattern is illustrated in Figure 4. The Read Data from CG RAM, Write Data to CG RAM, and Set DD RAM instructions provide for easy programmability.

4.0 ELECTRICAL SPECIFICATIONS

4.1 Absolute Maximum Rating

Power Supply Voltage (V_{CC}) -0.3 to $+6.5 V_{DC}$
Input Voltage -0.3 to $+V_{CC} +0.3 V_{DC}$

4.2 Normal Operating Rating

Power Supply Voltage (V_{CC}) $+5.0$ Volts $\pm 10\%$
Supply Current ($V_{CC} = 5 V_{DC}$) 16 mA ± 2 mA
Backlight Current ($V_{BL} = 5 V_{DC}$) 900 mA ± 50 mA

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4.3 Electrical Characteristics ($V_{CC} = 5V \pm 10\%$)

Item	Symbol	Condition	Min	Max	Unit
Input "High" Voltage	V_{IH}	2.2	V_{CC}	V	
Input "Low" Voltage	V_{IL}	-0.3	0.6	V	
Output "High" Voltage (TTL)	V_{OH1}	$I_{OH} = 0.205 \text{ mA}$	2.4	-	V
Output "Low" Voltage (TTL)	V_{OL1}	$I_{OL} = 1.200 \text{ mA}$	-	0.4	V
Output "High" Voltage (CMOS)	V_{OH2}	$I_{OH} = 0.040 \text{ mA}$	$0.9 V_{CC}$	-	V
Output "Low" Voltage (CMOS)	V_{OL2}	$I_{OL} = 0.040 \text{ mA}$	-	$0.1 V_{CC}$	V
Input Leakage Current	I_{IL}	$V_{IN} = 0 \text{ to } V_{CC}$	-	0.001	mA
Supply Current (logic)	I_{CC}		12	20	mA
Supply Current (Backlight)	I_{BL}	$V_{BL} = 5.5 V_{DC}$		1.0	A

4.4 Timing Characteristics

Write Operation (Refer to Figure 11)

Item	Symbol	Min	Max	Unit
Enable Cycle Time	t_{CYC}	1000	-	ns
Enable Pulse Width "High Level"	PW_{EH}	450	-	ns
Enable Rise/Fall Time	t_{Er}, t_{Ef}	-	25	ns
Address Set-up Time RS,R/W	t_{AS}	140	-	ns
Address Hold Time	t_{AH}	10	-	ns
Data Set-up Time	t_{DSW}	195	-	ns
Data Hold Time	t_H	10	-	ns

Read Operation (Refer to Figure 12)

Item	Symbol	Min	Max	Unit
Enable Cycle Time	t_{CYC}	1000	-	ns
Enable Pulse Width "High Level"	PW_{EH}	450	-	ns
Enable Rise/Fall Time	t_{Er}, t_{Ef}	-	25	ns
Address Set-up Time RS,R/W	t_{AS}	140	-	ns
Address Hold Time	t_{AH}	10	-	ns
Data Delay Time	t_{DDR}	-	320	ns
Data Hold Time	t_{DHR}	20	-	ns

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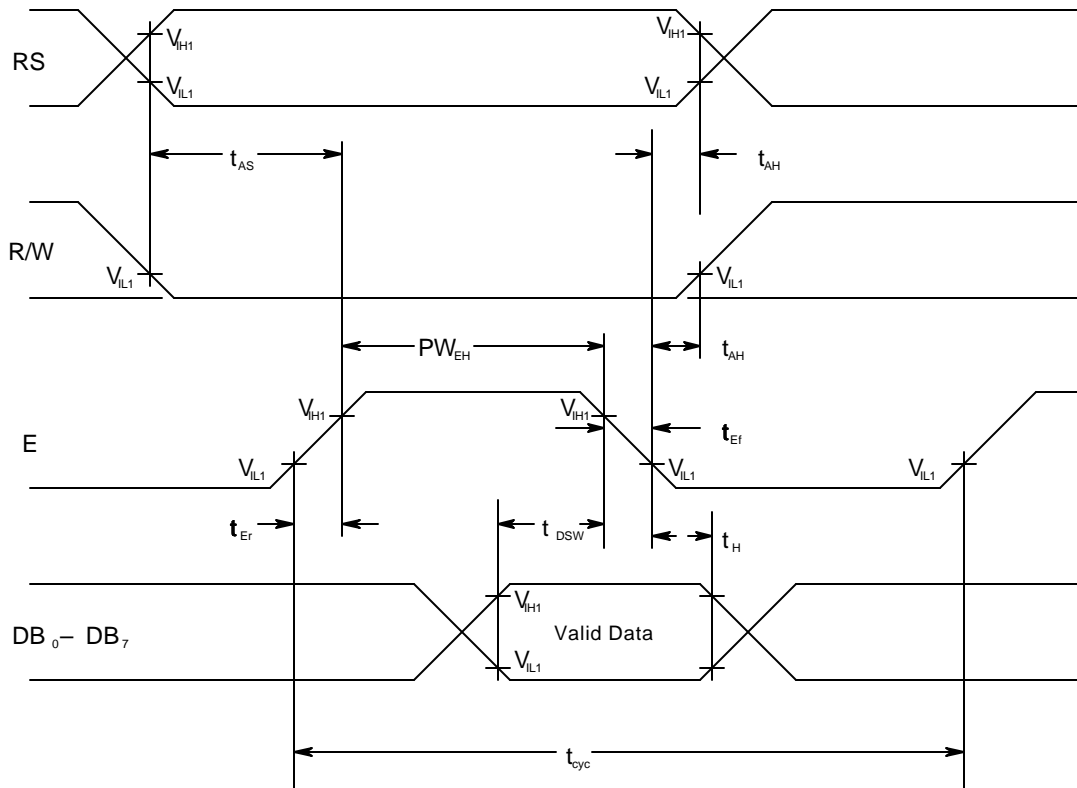


Figure 11 Interface Timing (Write)

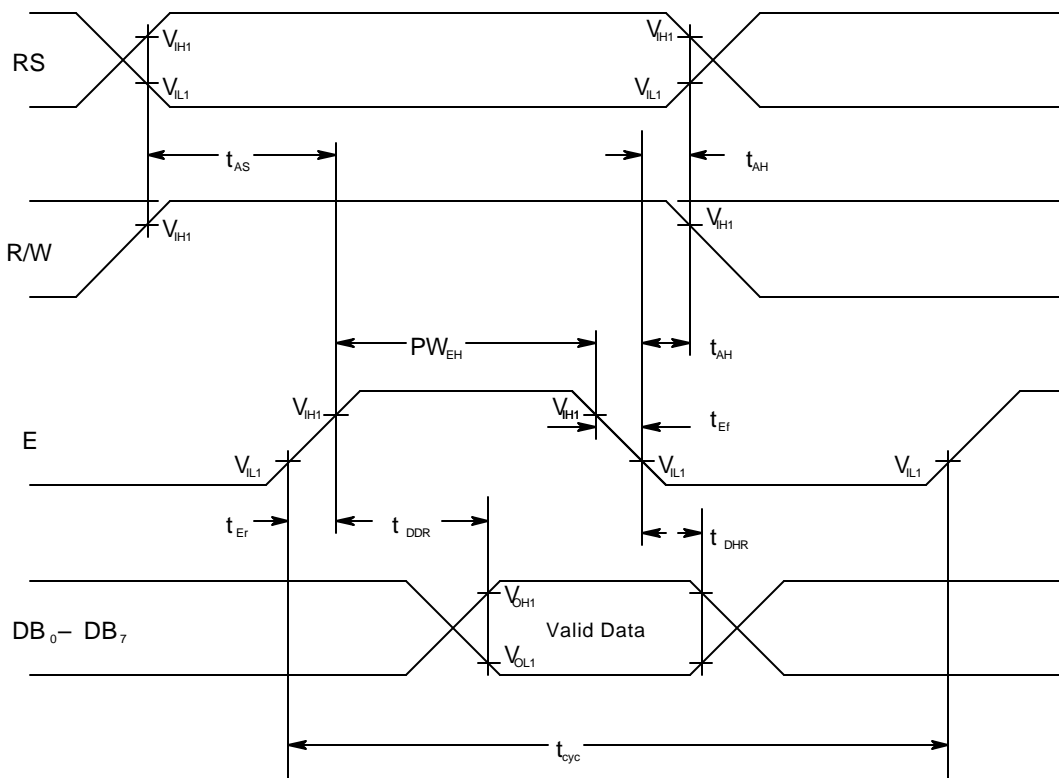


Figure 12 Interface Timing (Read)

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4.5 Timing Sequence for 8 Bit Parallel Interface

Figure 13 illustrates the typical Busy Flag check sequence for an 8 bit data interface.

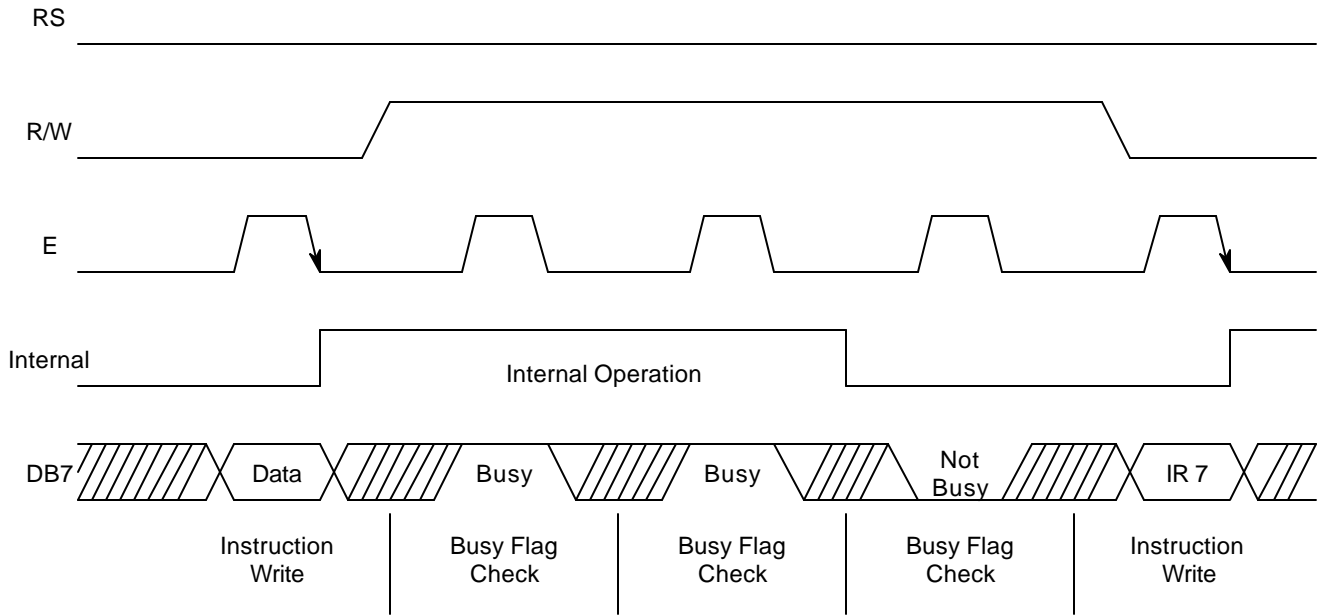


Figure 13 Busy Flag Check Sequence for 8-bit Parallel Interface

4.6 Timing Sequence for 4 Bit Parallel Interface

Figure 14 illustrates the typical Busy Flag check sequence for a 4 bit data bus interface.

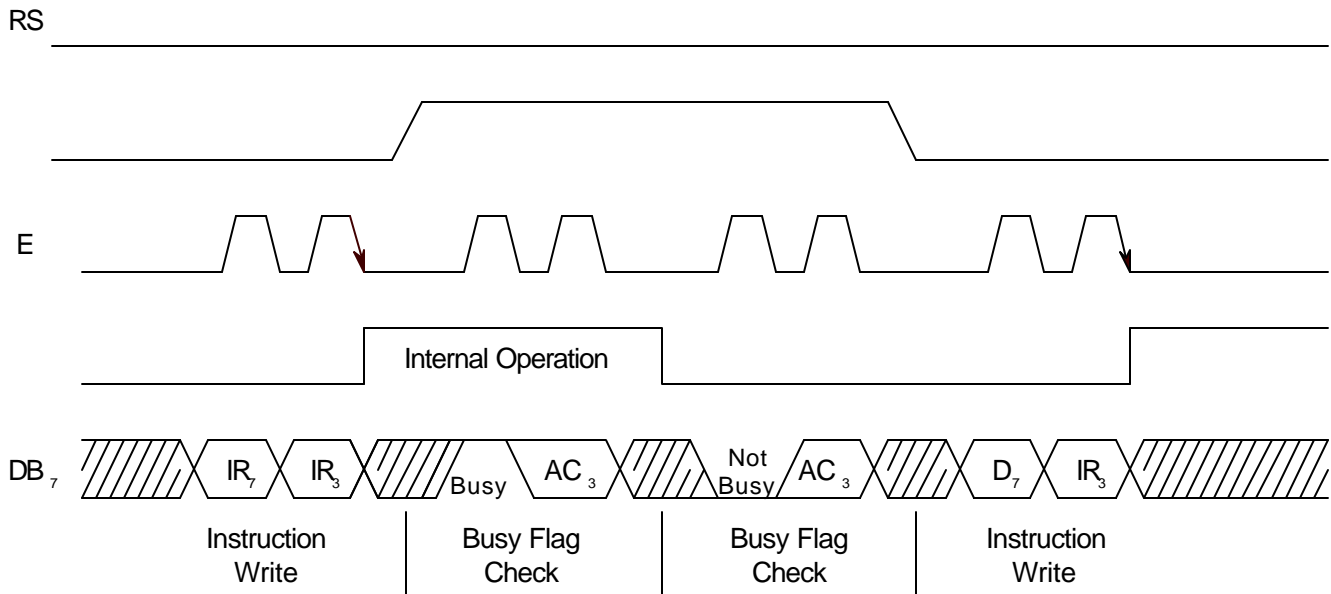


Figure 14 Busy Flag Check Sequence for 4-bit Parallel Interface

Note: IR₇, IR₃: Instruction, 7th bit & 3rd bit
 AC₃: Address Counter, 3rd bit

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4.7 Connector Pin Assignments (P1)

Pin No.	Function
1	N/C
2	V _{BIAS} (Factory Set-up Test Point)
3	N/C *
4	ADJ (Viewing Angle Adjustment)
5	R/W (Read = Logic 1)
6	Key (Pin Removed)
7	RS
8	Ground
9	Enable (E1)
10	Ground
11	DB ₀
12	Ground
13	DB ₁
14	Ground
15	DB ₂
16	Ground
17	DB ₃
18	Ground
19	DB ₄
20	Ground
21	DB ₅
22	V _{CC} (+5V _{DC} – Parallel with Pin 24)
23	DB ₆
24	V _{CC} (+5V _{DC} – Parallel with Pin 22)
25	DB ₇
26	N/C

* When the display module includes the serial data input option, Pin 3 is internally connected to provide signal E2 as an output to a second display module.

CMOS Note: Care must be taken to insure that input signals do not exceed the supply voltage or ground levels. Data cables must be as short as possible to reduce signal overshoots.

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5.0 ENVIRONMENTAL CHARACTERISTICS

5.1 Operating

Temperature:	-30 to +80°C
Humidity: (@ 40°C)	95% RH (non-condensing)
Humidity (< 40°C):	Absolute humidity must be lower the humidity of 95% RH at 40°C
Vibration:	10g at 10 to 400Hz (3 axes)
Shock:	10g (all axes)

5.2 Non-Operating

Temperature:	-40°C to +85°C
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6.0 OPTICAL SPECIFICATIONS

6.1 Optical Characteristics

Format:	Four lines of 40 characters
Character Font:	5x7 dot matrix with cursor
Character Height w/ cursor:	0.48" (12.1mm)
Character Height w/o cursor:	0.39" (9.9mm)
Character Width:	0.24" (6.1mm)
Overall Active Area:	5.70" x 2.34" (144.9mm x 59.5mm)
Peak Vertical Viewing Angle:	20° below normal plane
Viewing Mode:	Transflective, light field

Item	Symbol	Condition	Min	Typ	Max	Unit
Viewing Angle-Vertical	$\phi 1-\phi 2$	CR=2.0, $\theta=0^\circ$	100	120	-	deg.
Viewing Angle-Horizontal*	T	CR=2.0	± 45	± 55	-	deg.
Contrast ratio (Peak)**	CR	25°C	10	18	-	-
Response time (ON)**	t_r	25°C	-	100	150	mS
		-30°C	-	2000	-	mS
Response time (OFF)**	t_f	25°C	-	150	200	mS
		-30°C	-	4000	-	mS

* Measured at peak vertical angle, $\phi = -20^\circ$

** Measured at peak viewing angles:

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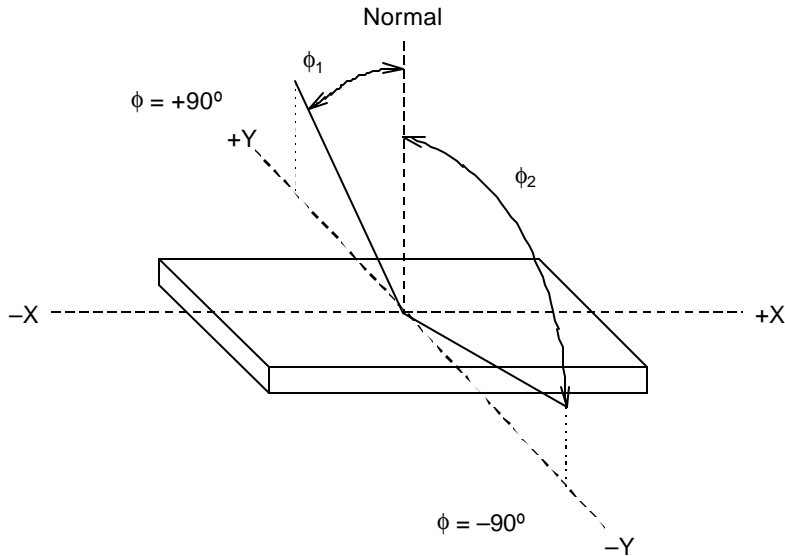


Figure 15 Definition of Vertical Viewing Angle

Definition of Horizontal Viewing Angle—top Viewing Display (for Bottom Viewing Displays $\phi = -20^\circ$ Typically)

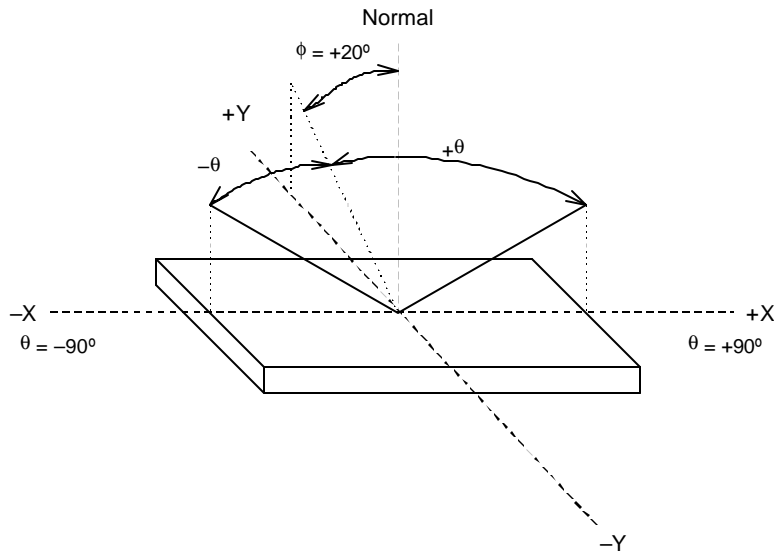


Figure 16 Definition of Horizontal Viewing Angle

Display contrast ratio is given by:

$$CR = \frac{B_2}{B_1}$$

Where: B_1 = Brightness of selected segment
 B_2 = Brightness of non-selected segment

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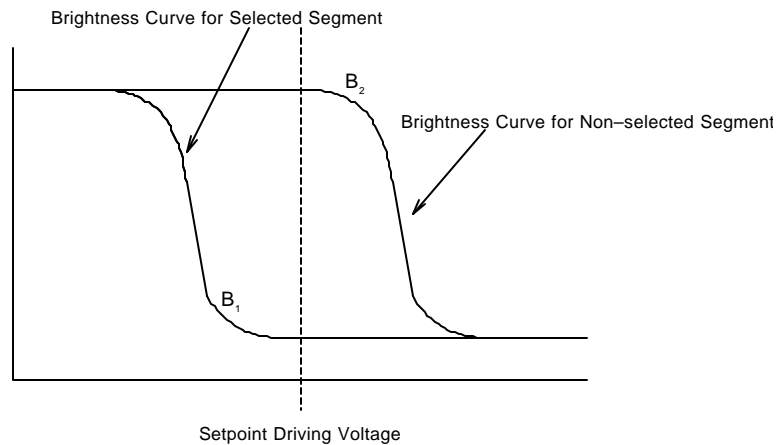


Figure 17 Definition of Contrast Ratio (CR)

Definition of optical response.

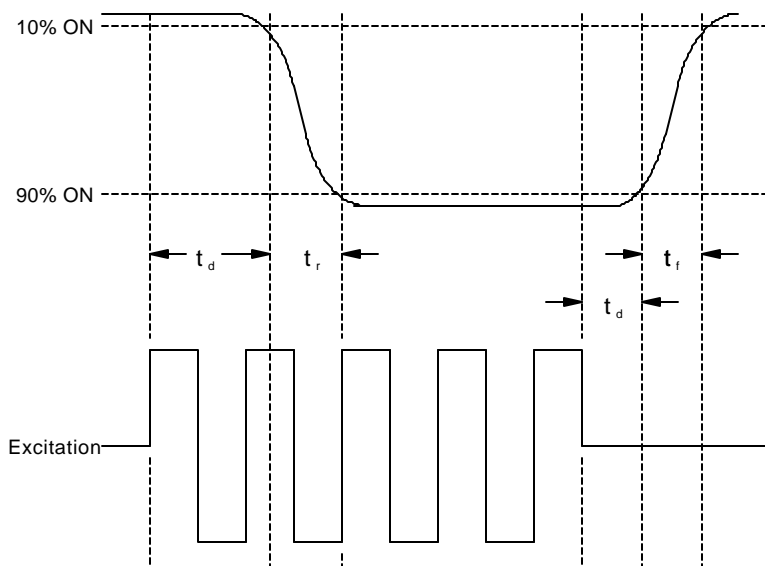


Figure 18 Definition of Optical Response

6.2 Viewing Angle Adjustment

The factory preadjusts the viewing angle of the display by setting the LCD bias voltage to 10.2 Volts using the on-board potentiometer. This is considered to be a nominal adjustment, but the user may prefer to vary this to optimize the viewing for a particular application. The bias voltage is measured between V_{CC} (pin #22) and V_{BIAS} (pin #2).

The viewing angle and contrast ratio may be externally controlled using an additional 10K ohm potentiometer. The potentiometer on the rear of the module must first be set to the maximum resistance by turning the adjustment fully counterclockwise. A 10K ohm potentiometer can then be connected between pin numbers 4 and 22 on the connector. Since the module has wide viewing angle characteristics and built-in temperature compensation of the viewing angle, the user may find that this external viewing control is unnecessary.

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7.0 FIBER OPTIC BACKLIGHT

7.1 FO Backlight Description

The module contains a light emitting flat panel constructed of plastic optical fibers which convey the light from a separately located light source. The panel is heat free, has indefinitely long life and has good brightness uniformity. The optical fibers are gathered into a bundle at the end of the flat panel and are routed to the light source.

The separately located light source is affixed to a bracket that mounts behind the display module using two of the module mounting holes (see the outline drawing, Figure 20). If the increased module depth is not acceptable, light source can be relocated elsewhere by the user within an approximate 2.5 inch radius (length of the fiber bundle) from the end of the display module. The standard light source is a halogen 5.0 Volt, 4.85 Watt lamp with 8.0 inch leads terminated by a connector to be connected by the user.

Care should be exercised in the physical location of the light source since halogen lamps operate in excess of 250°C.

Because the attenuation of the LCD cell, only 10% of the backlight luminance is emitted from the display. Thus to provide a brightly lit display, the original light source must be 10 times brighter.

7.2 Lamps Characteristics

The standard light source is a 4.85 Watt, 5.0 Volt halogen lamp. Figure 19 below shows the standard light source and two alternates which use less power. They may be satisfactory for a display in low to no ambient light and are available by special order.

Lamp Power	Rated Voltage	Relative Brightness	Rated Life (R _L)	Lamp Type
* 4.5 Watts	5.0 Volts	1.0	15k Hours	Halogen
2.5 Watts	5.0 Volts	0.6	5k Hours	Gas
1.5 Watts	12.0 Volts	0.1	15k Hours	Incandescent

Figure 19 Typical Lamp Characteristics

These sources all include a reflector as part of the lamp, which focuses the light toward the polished end of the fiber bundle.

Rated life is expressed for operation at design voltage with alternating currents under laboratory test conditions. Actual life (L_A) is very sensitive to applied voltage (V_A) as expressed by the following equation where V_R is the rated design voltage.

$$L_A = (R_L) (V_R/V_A)^{12}$$

The lamp may be powered by either AC or DC voltage. The 8.0" lamp leads are terminated in a Molex connector P/N 50-57-9402. This mates with numerous Molex headers including the following:

70553-0106, PWB Mount

70107-0036, Panel Mount

70107-0001, Wire-To-Wire

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7.3 Standard Operation

Lamp Color Temperature:	2900 – 3100 K
Display Luminance:	3.0 – 4.5 ft-L
Luminance Uniformity:	AVG 30%
Operating Temperature:	-30 to +80 C
Storage Temperature:	-40 to +85 C

8.0 INSTALLATION NOTE

To protect the front polarizer from accidental damage it is highly recommended that the LCD be mounted behind a clear glass or polycarbonate window material. It is also recommended that an air gap of at least .030" to .050" minimum be provided between the window material and the surface of the LCD to prevent the transfer of static charges to the front surface of the LCD. Supertwist LCD's may activate un-driven elements in response to a surface static charge on the front polarizer. It may take several minutes for such a surface static charge to dissipate.

9.0 ACCESSORIES

Power/Data Connector Only (26 pin)	30554-99
Keyed Power/Data Connector with cable	30554-XX
Double ended keyed Power/Data cable(26 pin)	30553-XX
Replacement Lamp-Reflector Assembly	48686-04

(XX = length in inches of cable)

(Standard cables are 18 and 36 inches)

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10.0 OUTLINE AND INSTALLATION CHARACTERISTICS

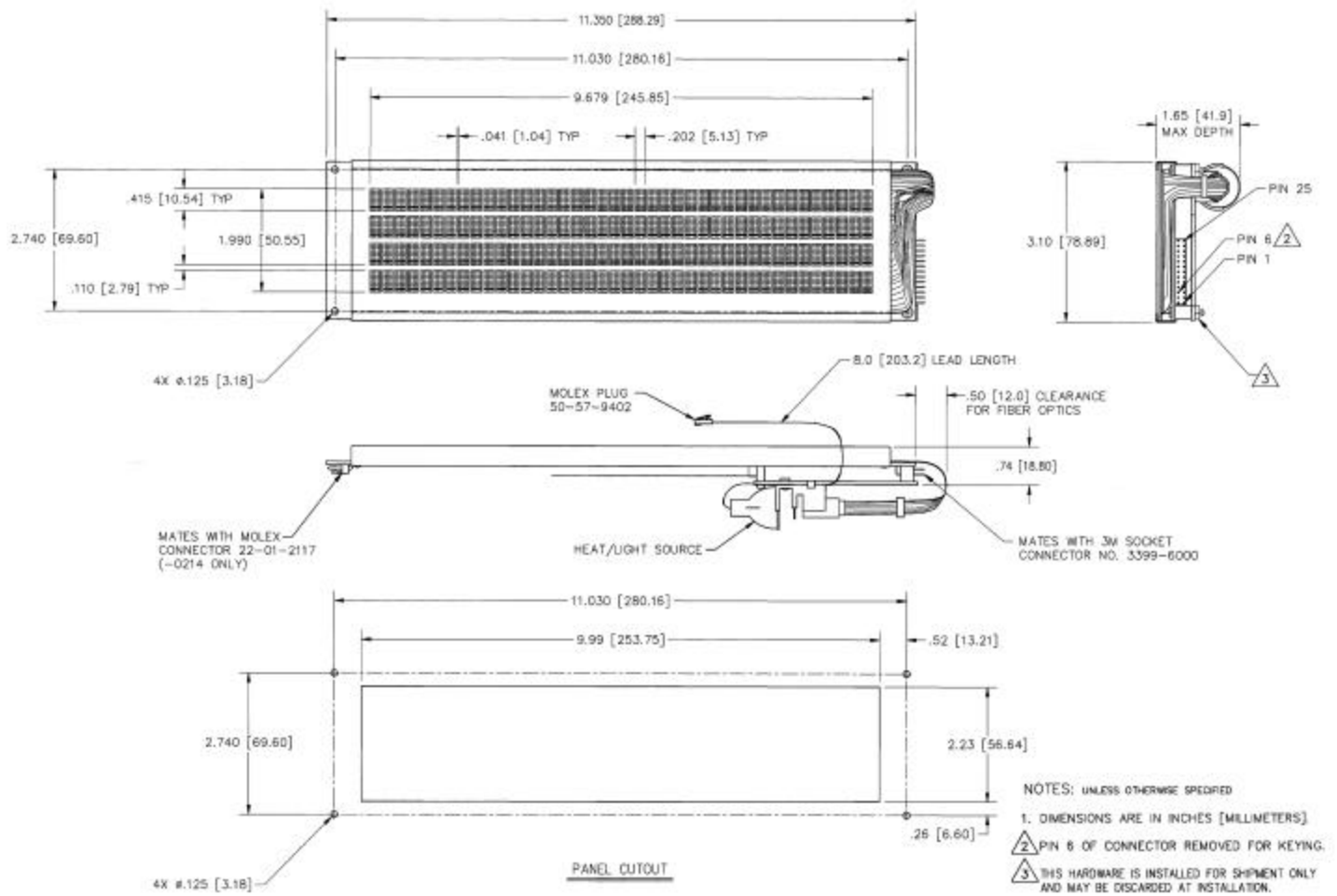


Figure 20 03875-21-0114 Outline Drawing

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