Ordering number : EN3947F

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DATA SHEET

Monolithic Digital IC

LB1836M — Low-Saturation Bidirectional Motor Driver for Low-Voltage Drive

Overview

The LB1836M is a low-saturation two-channel bidirectional motor driver IC for use in low-voltage applications. The LB1836M is a bipolar stepper-motor driver IC that is ideal for use in printers, FDDs, cameras and other portable devices.

Features

- Low voltage operation (2.5V min)
- Low saturation voltage (upper transistor + lower transistor residual voltage ; 0.40V typ at 400mA).
- Parallel connection (Upper transistor + lower transistor residual voltage ; 0.5V typ at 800mA).
- Separate logic power supply and motor power supply
- Brake function
- Spark killer diodes built in
- Thermal shutdown circuit built in
- Compact package (14-pin MFP)

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		-0.3 to +10.5	V
	V_S max		-0.3 to +10.5	V
Output supply voltage	V_{OUT}		$V_S + V_{SF}$	V
Input supply voltage	V_{IN}		-0.3 to +10	V
GND pin flow-out current	IGND	Per channel	1.0	A
Allowable power dissipation	Pd max	* Mounted on a board.	800	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* Mounted on a substrate: 30×30×1.5mm^3, glass epoxy board.

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Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		2.5 to 9.0	V
	V_S		1.8 to 9.0	V
Input “H”-level voltage	V_{IH}		1.8 to 9.0	V
Input “L”-level voltage	V_{IL}		-0.3 to +0.7	V

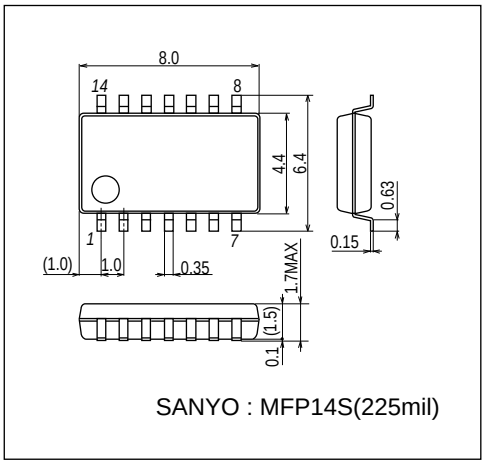
Electrical Characteristics at Ta = 25°C, V_{CC} = VS = 3V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current	$I_{CC}0$	$V_{IN}1$, 2, 3, 4 = 0V, I_{CC} + I_S		0.1	10	µA
	$I_{CC}1$	$V_{IN}1$ = 3V, $V_{IN}2$, 3, 4 = 0V, I_{CC} + I_S		14	20	mA
	$I_{CC}2$	$V_{IN}1$, 2 = 3V, $V_{IN}3$, 4 = 0V, I_{CC} + I_S		22	35	mA
Output saturation voltage (upper + lower)	$V_{OUT}1$	I_{OUT} = 200mA		0.20	0.28	V
	$V_{OUT}2$	I_{OUT} = 400mA		0.40	0.60	V
	$V_{OUT}3$	I_{OUT} = 400mA, Parallel connection		0.25	0.35	V
	$V_{OUT}4$	I_{OUT} = 800mA, Parallel connection		0.50	0.70	V
Output sustain voltage	V_O (SUS)	I_{OUT} = 400mA	9			V
Input current	I_{IN}	V_{IN} = 2V, V_{CC} = 6V			80	µA
Spark killer diode						
Reverse current	I_S (leak)	V_{CC}1, 2 = 9V			30	µA
Forward voltage	V_{SF}	I_{OUT} = 400mA			1.7	V

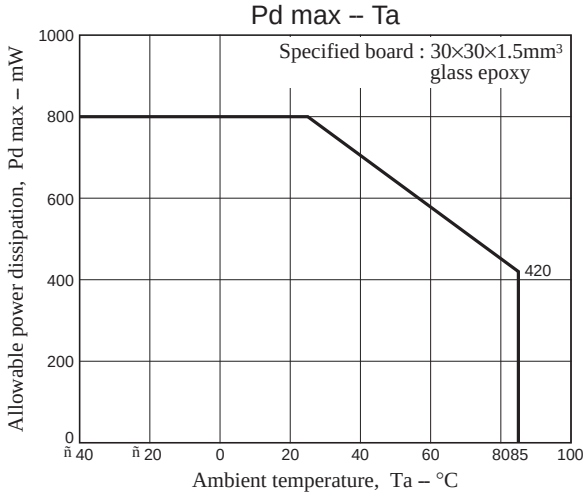
Package Dimensions

unit : mm (typ)

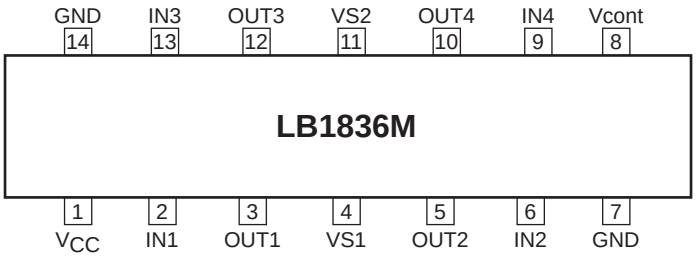
3111A



SANYO : MFP14S(225mil)



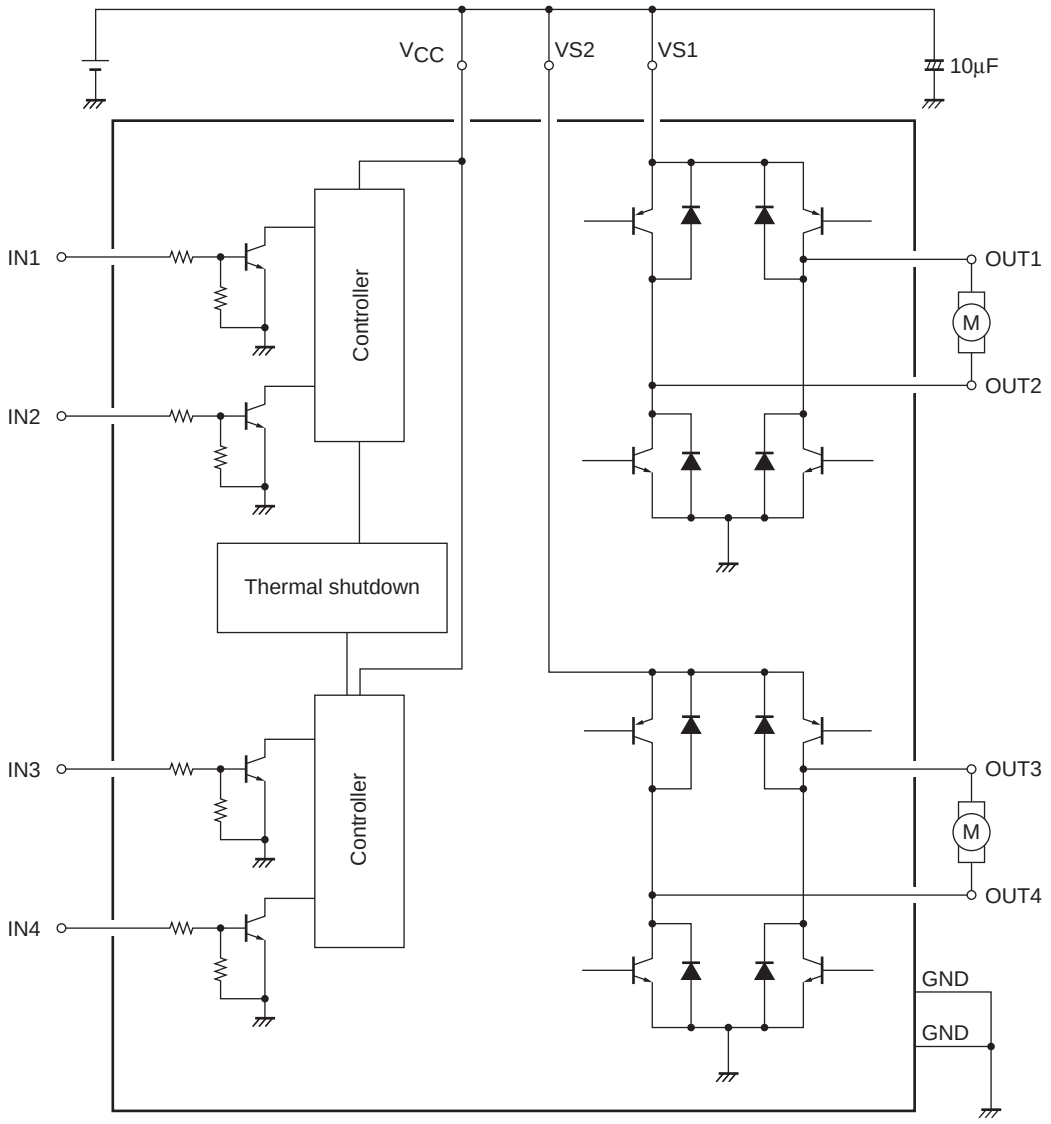
Pin Assignment



Top view

Note) Ground both GND pins.

Block Diagram



Truth Table

IN1/3	IN2/4	OUT1/3	OUT2/4	Mode
H	L	H	L	Forward
L	H	L	H	Reverse
H	H	L	L	Brake
L	L	OFF	OFF	Standby

Design Notes

If large current flows on the power supply (V_S) line and the GND line, then in some applications and layouts, misoperation due to line oscillation may result.

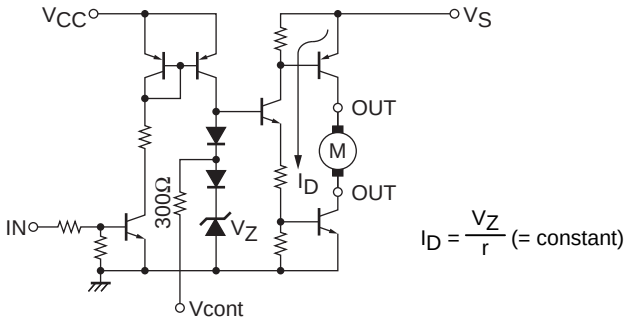
The modes during which large current flows are as follows :

- Motor surge current when the DC motor starts up or when it shifts rotation directions (forward ↔ reverse).
- Passthrough current generated within the IC when shifting rotation directions (forward ↔ reverse) or when shifting from forward/reverse rotation to braking, or vice versa.

The following points should be kept in mind regarding the pattern layout :

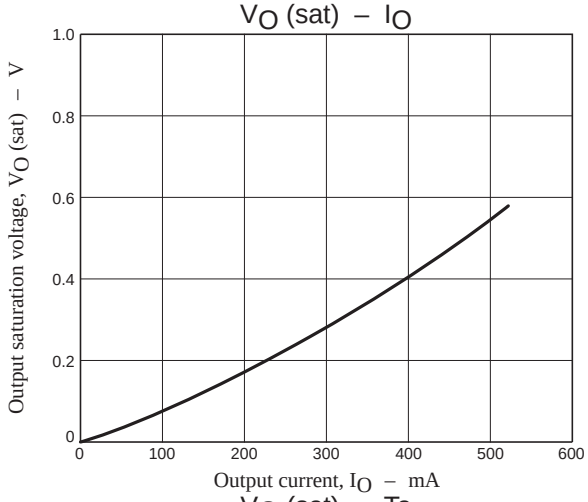
- Keep the wiring lines thick and short in order to reduce wiring inductance between the power supply (V_S) and GND.
- Insert a passthrough capacitor near the IC. (Maximum effect is obtained by inserting the passthrough capacitor between VS and the pin 7 GND at the closest distance possible.
- If the CPU and the LB1836M are mounted on separate boards and the difference between the ground potential of each board is large, install resistors of about 10kΩ in series between the CPU and the LB1836M inputs.

Vcont pin

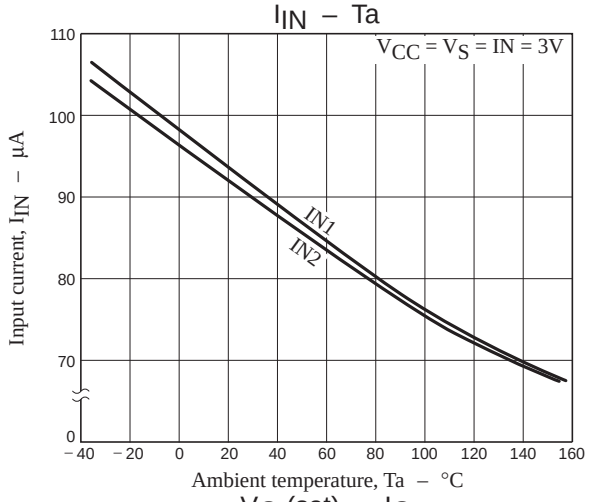


As shown in the above diagram, the Vcont pin outputs the voltage of the band gap Zener $V_Z + V_F$ (=1.93V).
In normal use, this pin is left open.
The drive current ID is varied by the Vcont voltage. However, because the band gap Zener is shared, it functions as a bridge.

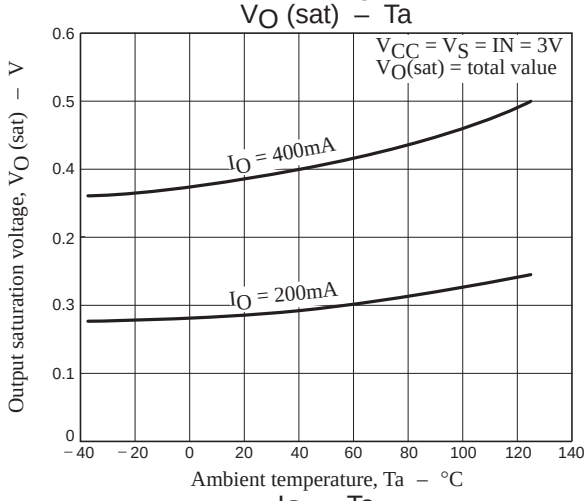
V_O (sat) – I_O



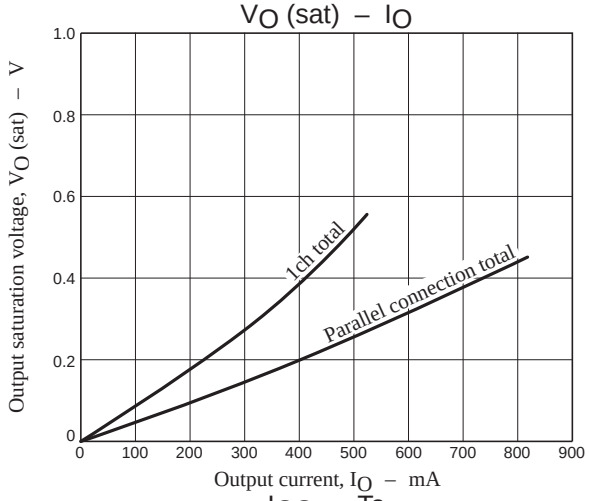
I_{IN} – Ta



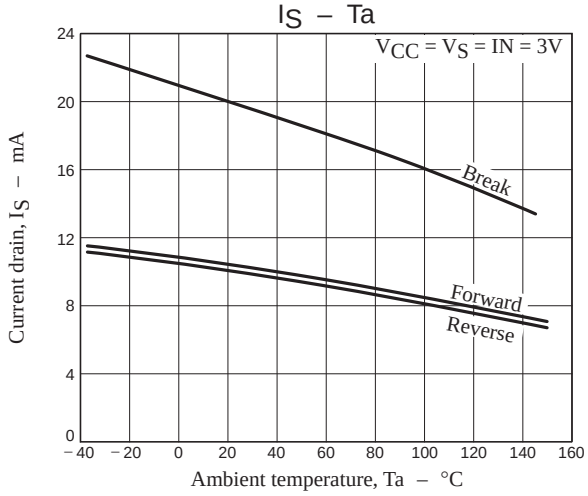
V_O (sat) – Ta



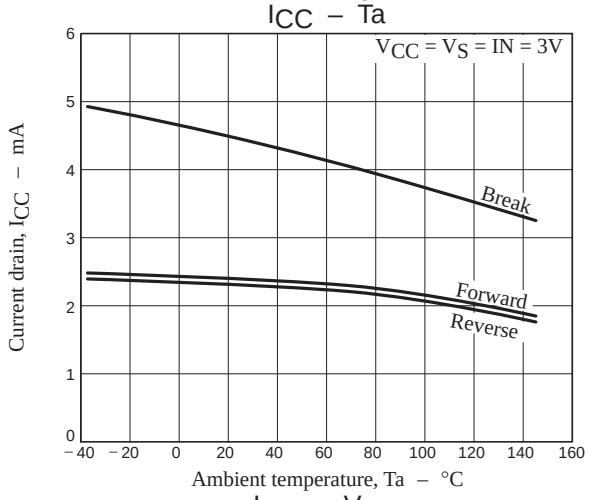
V_O (sat) – I_O



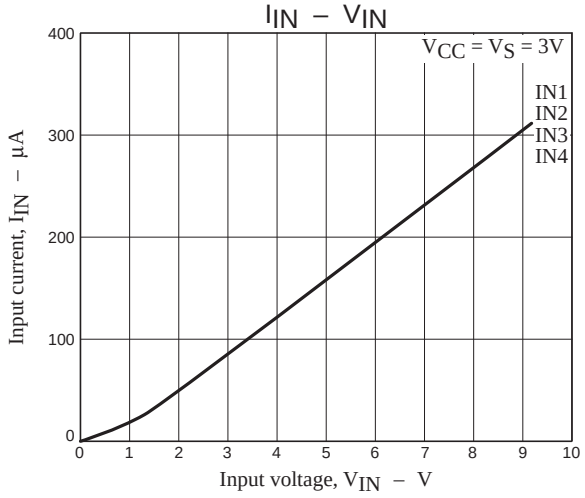
I_S – Ta



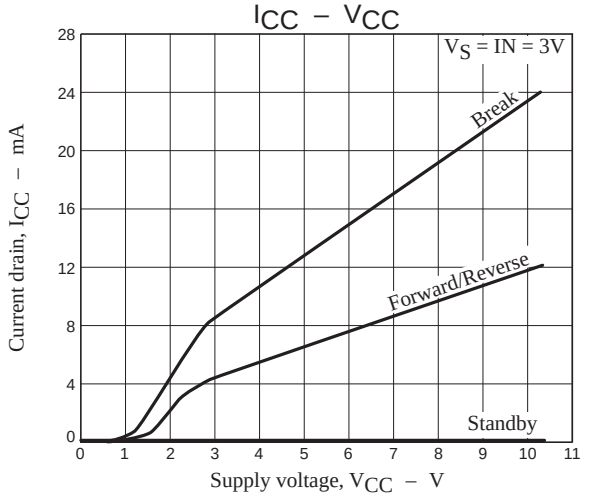
I_{CC} – Ta

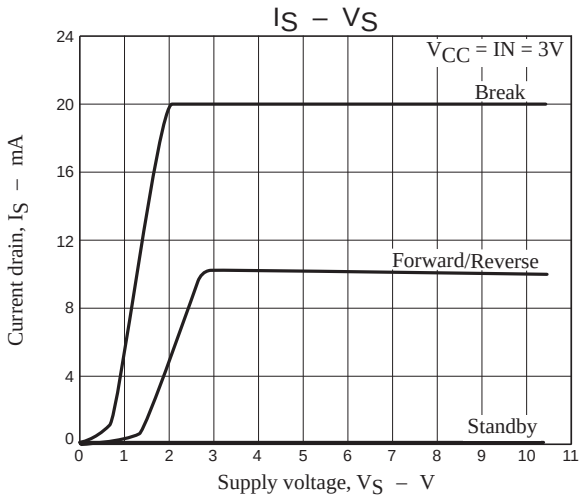


I_{IN} – V_{IN}



I_{CC} – V_{CC}





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