DATA SHEET

CBTD3384

10-bit level shifting bus switch with 5-bit output enables

Product data
Supersedes data of 2000 Aug 30
File under Integrated Circuits — ICL03

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Philips Semiconductors

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FEATURES

- 5 Ω switch connection between two ports
- TTL compatible control input and output levels
- Designed to be used in 5 V to 3.3 V level shifting applications
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, and 1000 V CDM per JESD22-C101

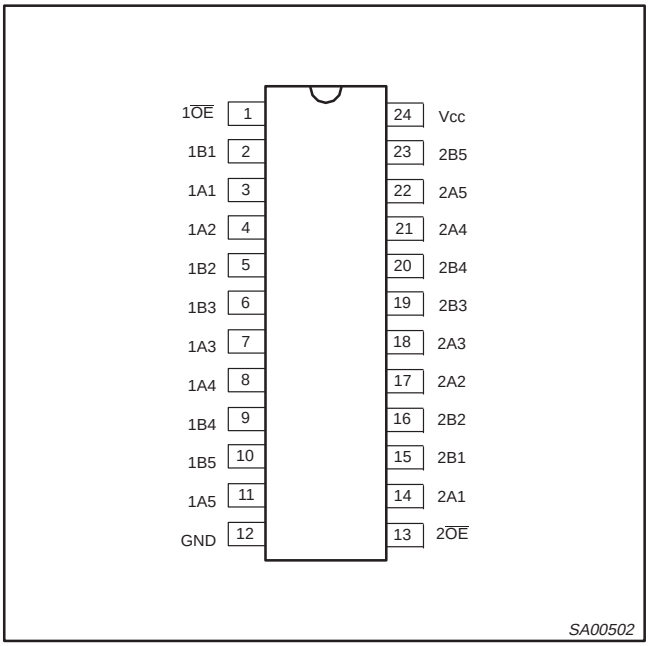
DESCRIPTION

The CBTD3384 provides ten bits of high-speed TTL-compatible level shifting bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The gate voltage of the enabled switch is lowered by a diode to allow convenient level shifting between 5 V and 3.3 V levels on either side of the CBTD3384.

The CBTD3384 device is organized as two 5-bit bus switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on and port A is connected to B. When $\overline{OE}$ is high, the switch is open and high-impedance state exists between the two ports.

The CBTD3384 is characterized for operation from –40 to +85 °C.

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{OE}$, $2\overline{OE}$	Output enables
3, 4, 7, 8, 11	1A1–1A5	Inputs
14, 17, 18, 21, 22	2A1–2A5	Inputs
2, 5, 6, 9, 10	1B1–1B5	Outputs
15, 16, 19, 20, 23	2B1–2B5	Outputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

QUICK REFERENCE DATA

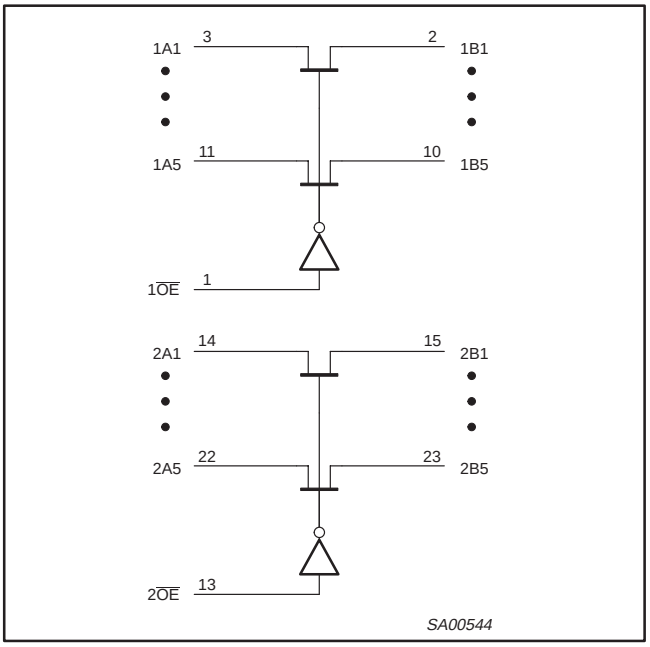
SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50 pF; V_{CC} = 5 V	250	ps
C_{IN}	Input capacitance	V_I = 0 V or V_{CC}	3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0 V or V_{CC}	6	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5 V	0.2	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
24-Pin Plastic SO	–40 to +85 °C	CBTD3384D	SOT137-1
24-Pin Plastic SSOP	–40 to +85 °C	CBTD3384DB	SOT340-1
24-Pin Plastic SSOP (QSOP)	–40 to +85 °C	CBTD3384DK	SOT556-1
24-Pin Plastic TSSOP	–40 to +85 °C	CBTD3384PW	SOT355-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS	
1$\overline{OE}$	2$\overline{OE}$	1A, 1B	2A, 2B
L	L	1A = 1B	2A= 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

H = High voltage level
L = Low voltage level
Z = High impedance “off” state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current		–50	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{SW}	DC output diode current	$V_O < 0$	±128	mA
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2.0	—	V
V_{IL}	Low-level Input voltage	—	0.8	V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			T_{amb} = –40 °C to +85 °C			
			Min	Typ[1]	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5 V; I_I = –18 mA	—	—	–1.2	V
V_{OH}	Output high pass voltage	See Figure 1	—	—	—	V
I_I	Input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V	—	—	±1	µA
I_{CC}	Quiescent supply current[2]	V_{CC} = 5.5 V; I_O = 0, V_I = V_{CC} or GND; $1\overline{OE}$=$2\overline{OE}$=GND	—	—	1.5	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5 V, one input at 3.4 V, other inputs at V_{CC} or GND	—	—	2.5	mA
C_I	Control pins	V_I= 3 V or 0	—	3.2	—	pF
$C_{I(OFF)}$	Port off capacitance	V_O = 3 V or 0, $\overline{OE}$ = V_{CC}	—	6	—	pF
r_{on}[3]	On-resistance	V_{CC} = 4.5 V; V_I = 0 V; I_I = 64 mA	—	5	7	Ω
		V_{CC} = 4.5 V; V_I = 0 V; I_I = 30 mA	—	5	7	
		V_{CC} = 4.5 V; V_I = 2.4 V; I_I = –15 mA	—	17	50	

NOTES:
1. All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C
2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND
3. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

AC CHARACTERISTICS

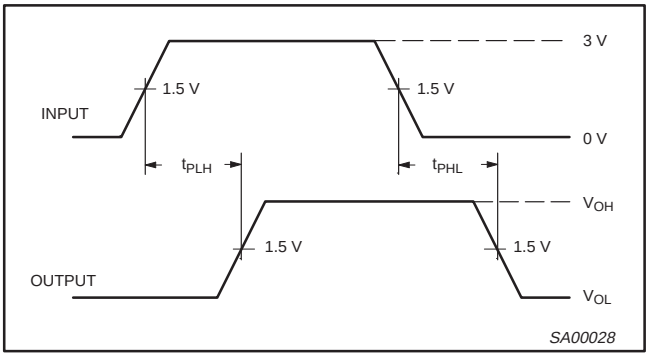
GND = 0 V; t_R = t_F = 2.5 nS; C_L = 50 pF

SYMBOL	PARAMETER DESCRIPTION	LIMITS			UNIT
		–40 °C to +85 °C V_{CC} = 5 V ± 0.5 V			
		Min	Mean	Max	
t_{pd}	Propagation delay[1]	—	—	250	ps
t_{PZH}	Output enable time to High level	2.3	4.3	7.0	ns
t_{PHZ}	Output disable time from High level	1.7	2.4	5.3	ns
t_{PZL}	Output enable time to Low level	2.3	4.9	7.5	ns
t_{PLZ}	Output disable time from Low level	1.7	4.2	5.3	ns

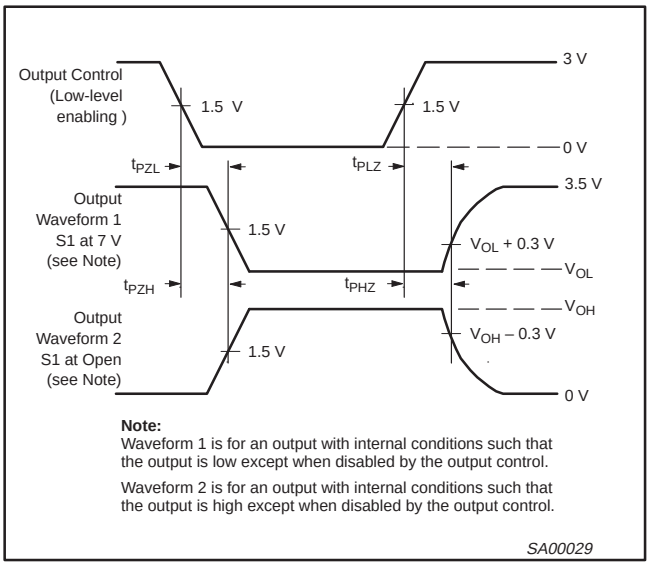
NOTE:
1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

AC WAVEFORMS

V_M = 1.5 V, V_{IN} = GND to 3.0 V

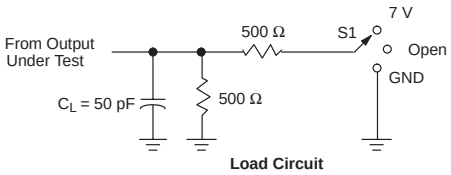


Waveform 1. Input (An) to Output (Yn) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



TEST	S1
t_{pd}	open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	open

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

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NOTES:

1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
2. The outputs are measured one at a time with one transition per measurement.

TYPICAL CHARACTERISTICS

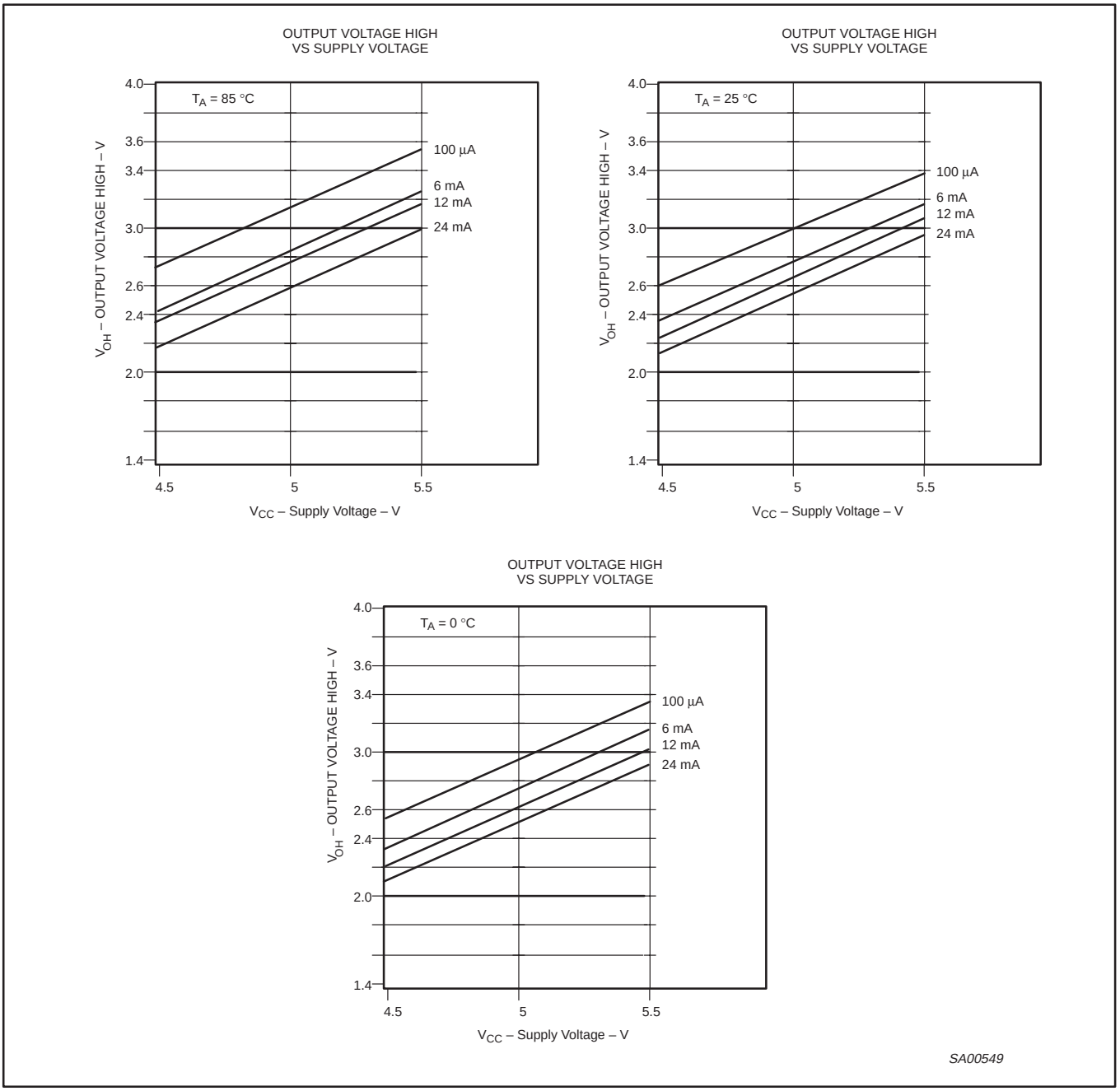
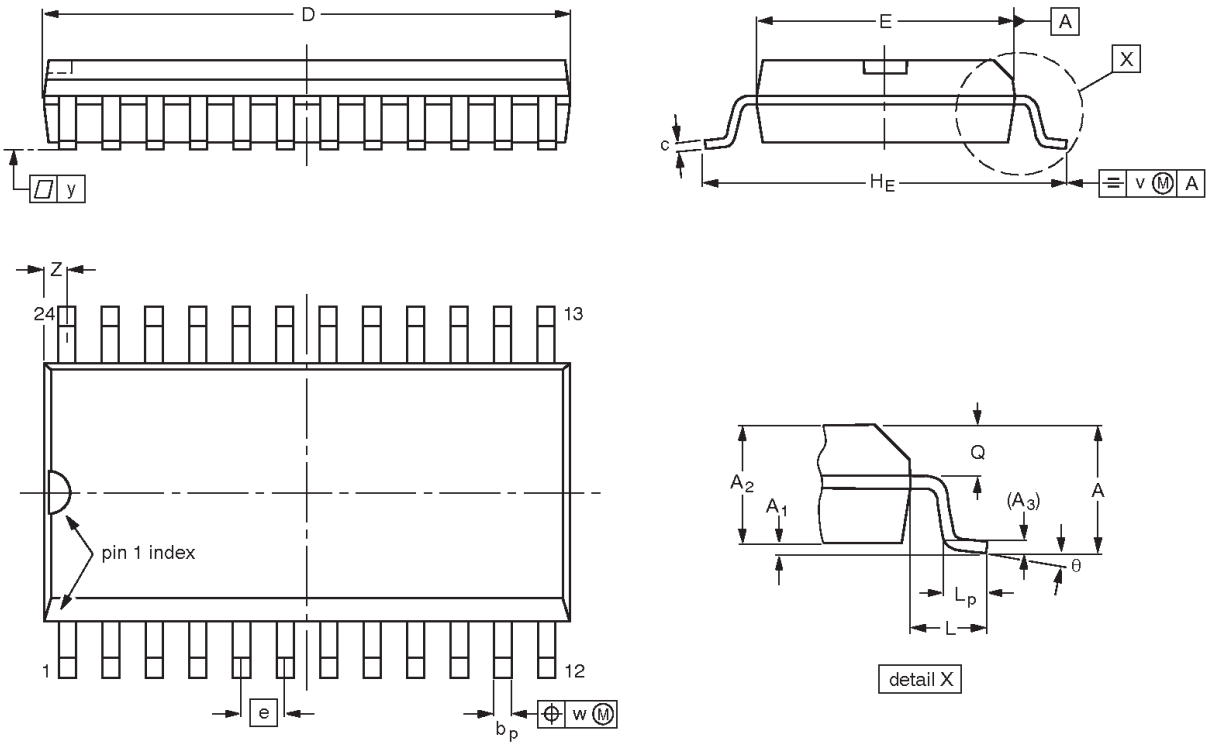


Figure 1. V_{OH} values (V_{in} = V_{CC})

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

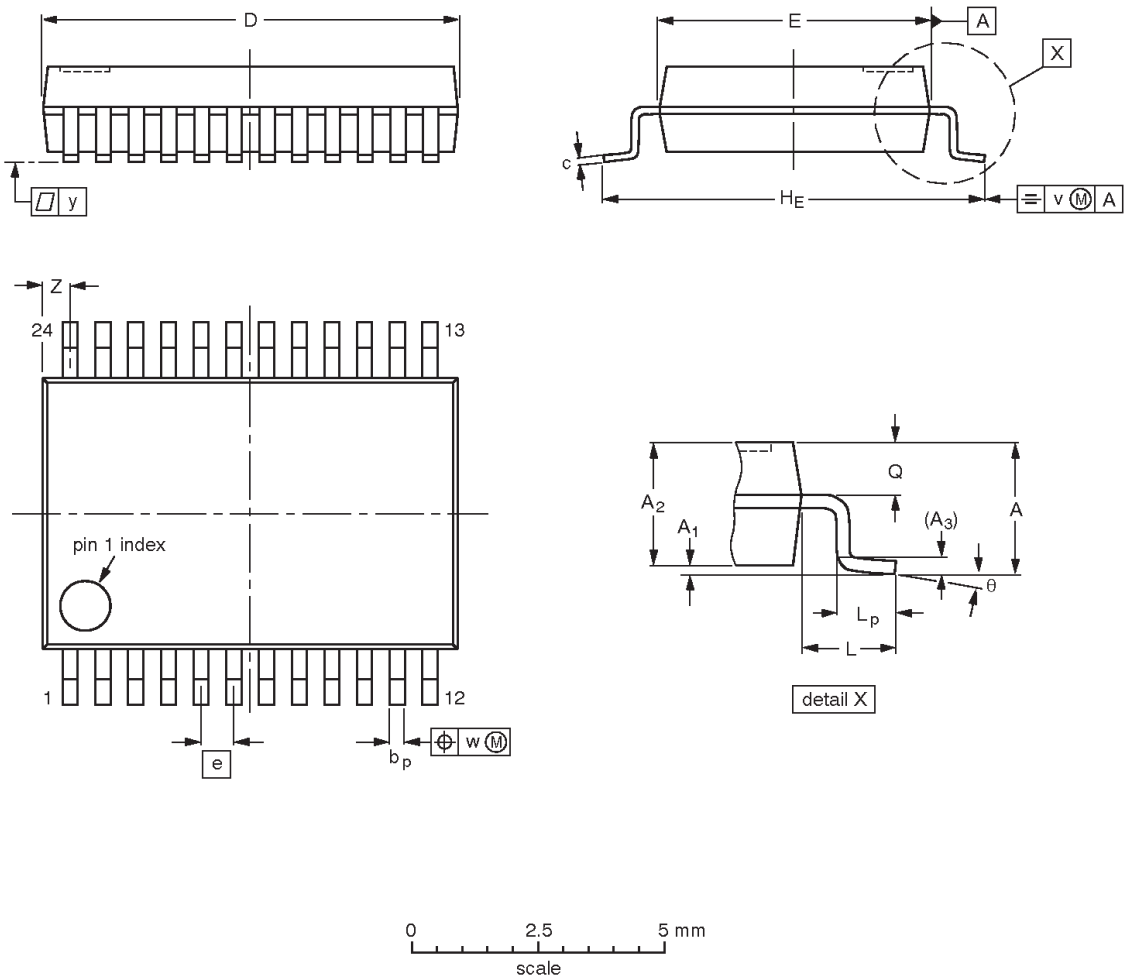
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013				~~97-05-22~~ 99-12-27

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

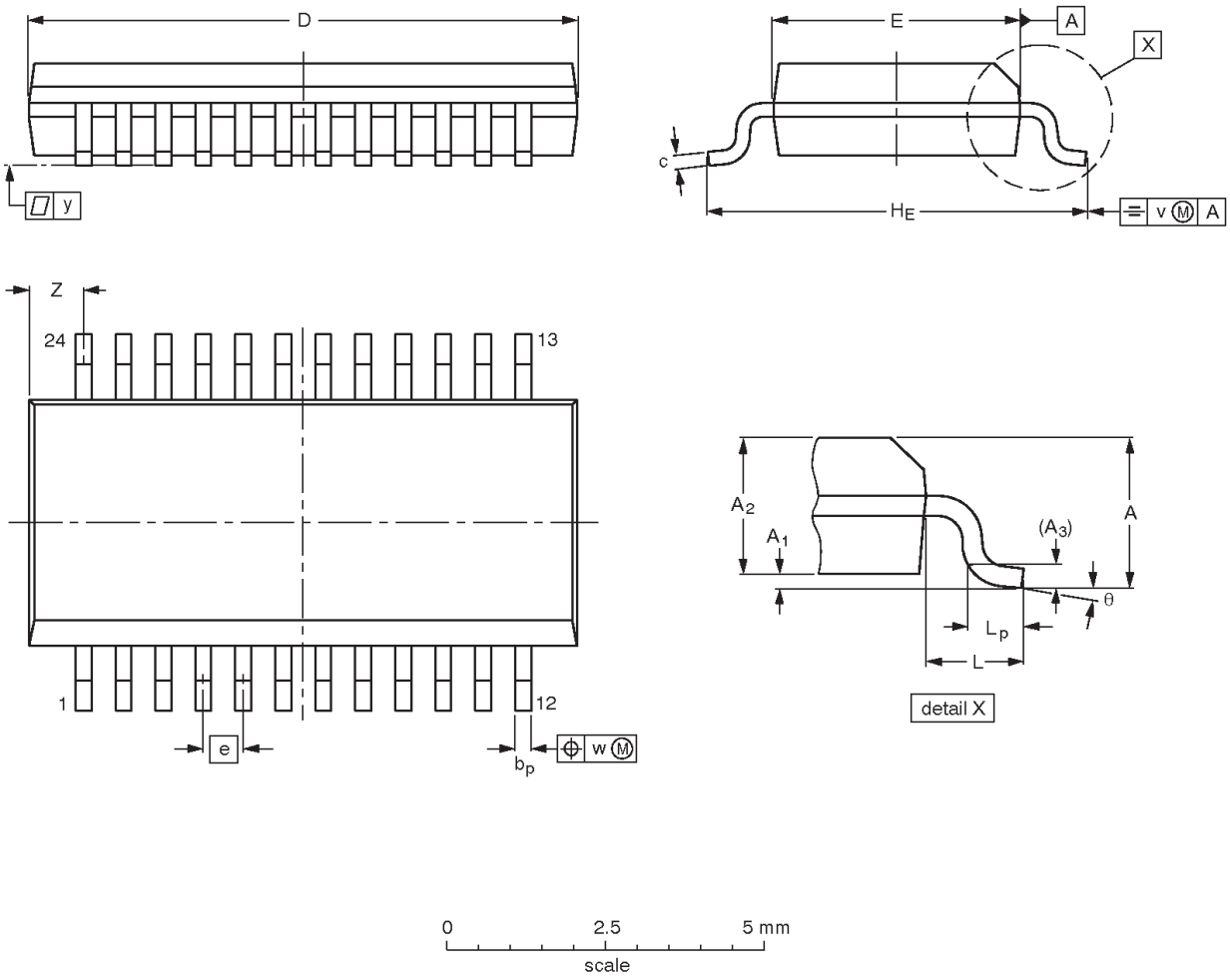
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150				~~95-02-04~~ 99-12-27

SSOP24: plastic shrink small outline package; 24 leads; body width 3.9 mm; lead pitch 0.635 mm **SOT556-1**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

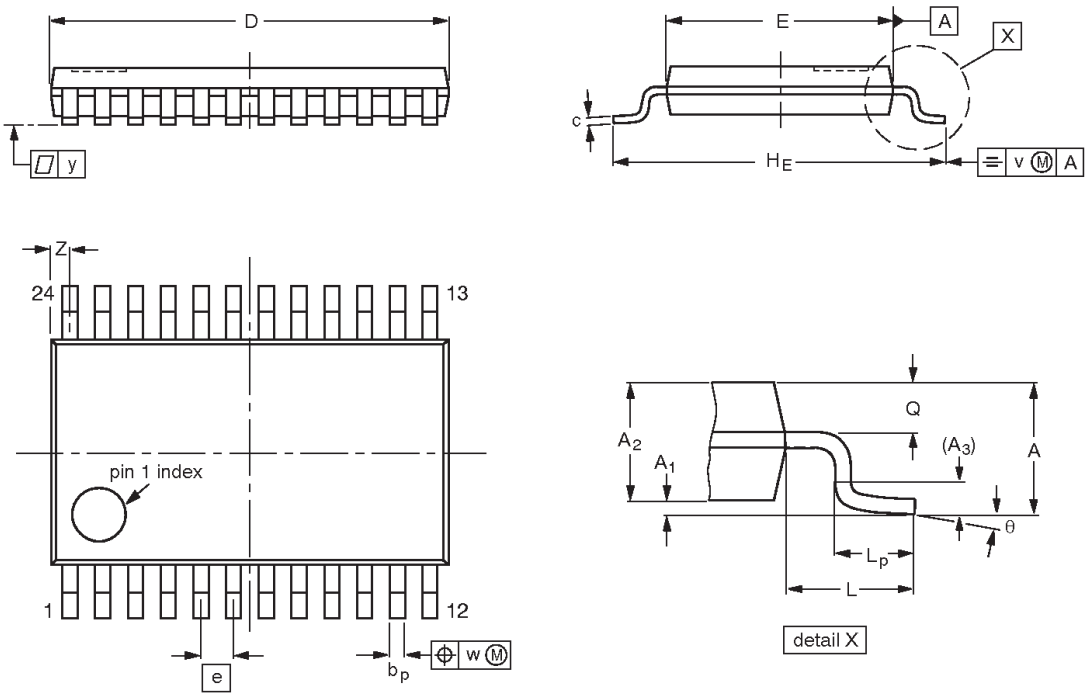
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.73	0.25 0.10	1.55 1.40	0.25	0.31 0.20	0.25 0.18	8.8 8.6	4.0 3.8	0.635	6.2 5.8	1.0	0.89 0.41	0.25	0.18	0.1	1.05 0.66	8^o 0^o
inches	0.068	0.0098 0.0040	0.061 0.055	0.010	0.012 0.008	0.0098 0.0075	0.344 0.337	0.157 0.150	0.025	0.244 0.228	0.041	0.035 0.016	0.010	0.007	0.004	0.040 0.026	8^o 0^o

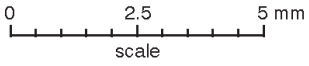
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT556-1		MO-137				~~99-05-05~~ 99-12-27

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm SOT355-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153				~~95-02-04~~ 99-12-27

NOTES

10-bit level shifting bus switch with 5-bit output enables

CBTD3384

Data sheet status

Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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